

T-46-23-15

**PRELIMINARY SPECIFICATION  
CMOS DRAM**

**KM41C1001**

**1M x 1 Bit Dynamic RAM with Nibble Mode**

**FEATURES**

- Performance range:

	t <sub>RAC</sub>	t <sub>CAC</sub>	t <sub>RC</sub>
KM41C1001-10	100ns	25ns	190ns
KM41C1001-12	120ns	30ns	220ns

- Nibble Mode Operation
- CAS-before-RAS Refresh
- RAS-only and Hidden Refresh
- TTL compatible inputs and output
- Common I/O using early write
- Single +5V ± 10% power supply
- 512 cycle/8ms refresh
- 256K x 4 fast test mode
- JEDEC standard pinout available in Plastic DIP, SOJ, ZIP packages.

**GENERAL DESCRIPTION**

The Samsung KM41C1001 is a CMOS high speed 1,048,576 x 1 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes and mini computers, graphics and high performance microprocessor systems.

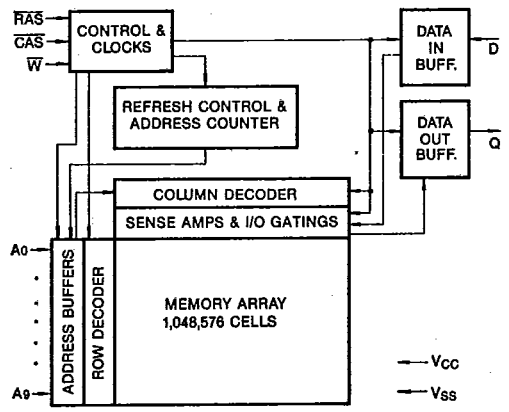
The KM41C1001 features Nibble Mode operation which allows high speed random access of up to 4-bits of data.

CAS-before-RAS Refresh capability provides on-chip auto refresh as an alternative to RAS-only Refresh. All inputs and output are fully TTL compatible.

The KM41C1001 is fabricated using Samsung's advanced CMOS process.

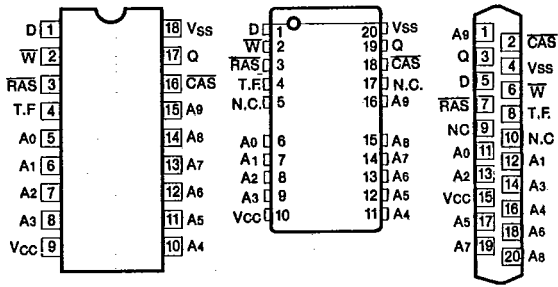
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**FUNCTIONAL BLOCK DIAGRAM**



**PIN CONFIGURATION**

- KM41C1001P
- KM41C1001J
- KM41C1001Z



Pin Name	Pin Function
A <sub>0</sub> -A <sub>9</sub>	Address Inputs
RAS	Row Address Strobe
D	Data In
Q	Data Out
CAS	Column Address Strobe
W	Read/Write Input
V <sub>cc</sub>	Power (+5V)
V <sub>ss</sub>	Ground
T.F	Test Function
N.C	No Connection