Integrated Device Technology, Inc.

256KB/512KB PIPELINED BURST FUSION™ MEMORY SECONDARY CACHE MODULES

PRELIMINARY
IDT7MPV6204
IDT7MPV6205
IDT7MPV6306
IDT7MPV6308

FEATURES

- For Intel Pentium CPU-based systems
- Low-cost, low-profile card edge module with 160 leads
- Uses FCI connector from the CELP2X80SCXXXX family
- Operates with external Pentium CPU speeds up to 66MHz
- Master and Slave module options
- Separate 5V (±5%) and 3.3V (±10%) power supplies
- Multiple GND pins and decoupling capacitors for maximum noise immunity
- Compatible with Mosys MCache™

DESCRIPTION

The IDT7MPV6204/05 and IDT7MPV6306/08 modules belong to a family of secondary caches intended for use with Intel Pentium CPU-based systems. The IDT7MPV6204/05/6306/08 use IDT's 71F432 32K x 32 pipelined Fusion Memory in plastic surface mount packages mounted on a multilayer epoxy laminate (FR-4) board. In addition, each of the modules uses a single 5V 8-bit wide SRAM for the tag. Extremely high speeds are achieved using IDT's high-reliability, low cost CMOS technology. The memory 1-T cell architecture allow IDT to pass on cost benefits where support from the appropriate core logic chipsets is present.

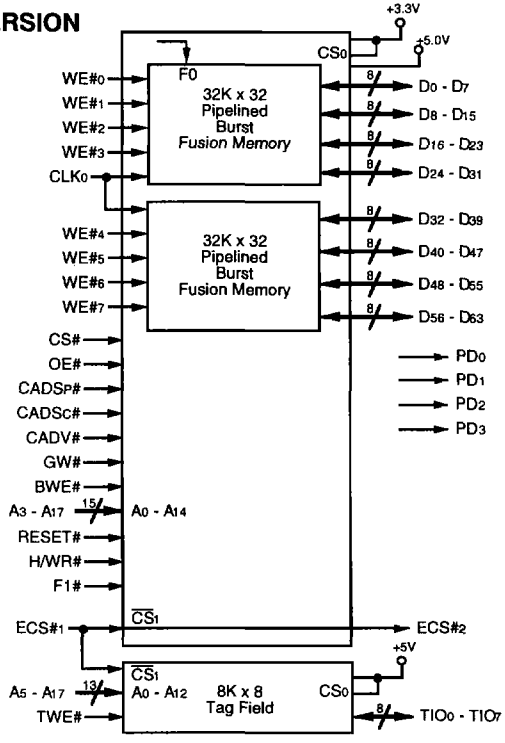
The data RAMs and a tag RAM provide an exact interface between the module and the chipset. Four PD (presence detect) input pins allow the system to determine presence of the cache.

The low profile card edge package allows 160 signal leads to be placed on a package 4.35" long, a maximum of 0.35" thick and a maximum of 1.14" tall.

All inputs and outputs are TTL-compatible and operate from separate 5V (±5%) and 3.3V (±10%) power supplies. Multiple GND pins and on-board decoupling capacitors ensure maximum protection from noise.

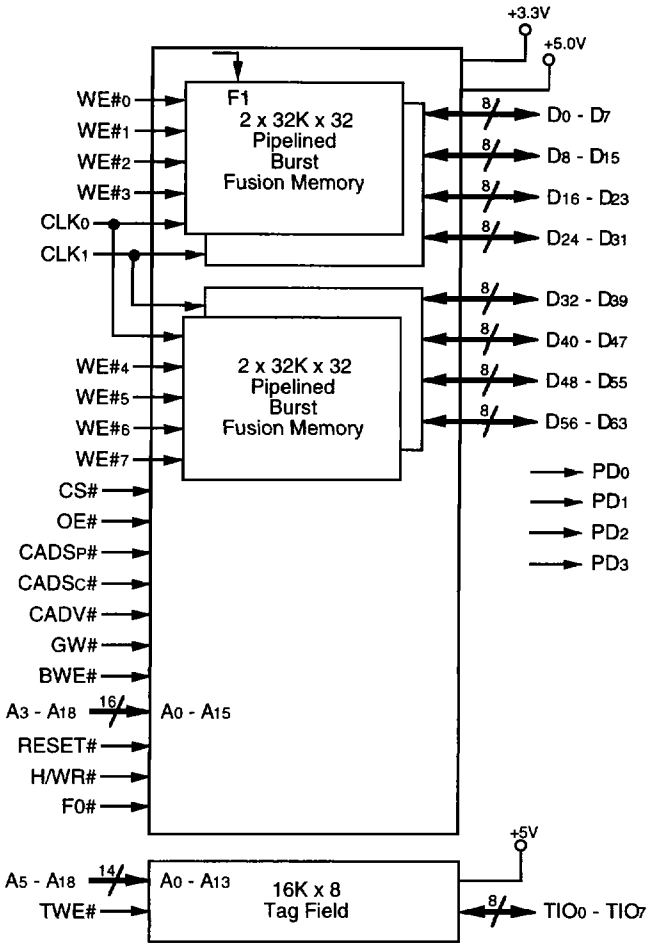
FUNCTIONAL BLOCK DIAGRAM

IDT7MPV6204/5 – 256KB VERSION



3518 drw 01

FUNCTIONAL BLOCK DIAGRAM
IDT7MPV6306/8 – 512KB VERSION



3518 drw 02

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC3}	Supply Voltage	3.0	3.3	3.6	V
V_{CC5}	Supply Voltage	4.75	5.0	5.25	V
GND	Supply Voltage	0	0	0.0	V
V_{IH}	Input High Voltage	2.2	—	V_{CC} + 0.3	V
V_{IL}	Input Low Voltage	–0.5[1]	—	0.8	V

NOTE: 3518 tbl 01

1. Power sequencing. V_{CC5} must be > V_{CC3} at all times, including during power up.
2. V_{IL} = –1.0V for pulse width less than 5ns, once per cycle.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Power Plane	Ambient Temperature	GND	Vcc
V_{CC3}	0°C to +70°C	0V	3.3V ± 10%
V_{CC5}	0°C to +70°C	0V	5.0V ± 5%

3518 tbl 02

ABSOLUTE MAXIMUM RATINGS

Symbol	Rating	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to V_{CC} + 0.5	V
V_{TERM} for V_{CC3}	Terminal Voltage with Respect to GND	–0.5 to +4.6	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–10 to +85	°C
T_{STG}	Storage Temperature	–55 to +125	°C
I_{OUT}	DC Output Current	50	mA

NOTE: 3518 tbl 03

Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

PIN CONFIGURATION

GND	81	1	GND
TIO_1	82	2	TIO_0
TIO_7	83	3	TIO_2
TIO_5	84	4	TIO_6
TIO_3	85	5	TIO_4
(1) N/C	86	6	N/C(1)
V_{CC5}	87	7	V_{CC3}
(1) N/C	88	8	TWE#
CADV#	89	9	CADSc#
GND	90	10	GND
OE#	91	11	WE#4
WE#5	92	12	WE#6
WE#7	93	13	WE#0
WE#1	94	14	WE#2
V_{CC5}	95	15	V_{CC3}
WE#3	96	16	CS#
F0	97	17	GW#
N/C	98	18	BWE#
GND	99	19	GND
RESET#	100	20	A_3
A_4	101	21	A_7
A_6	102	22	A_5
A_8	103	23	A_{11}
A_{10}	104	24	A_{16}
V_{CC5}	105	25	V_{CC3}
A_{17}	106	26	A_{18} (2)
GND	107	27	GND
A_9	108	28	A_{12}
A_{14}	109	29	A_{13}
A_{15}	110	30	CADSp#
H/WR#	111	31	ECS#1 (3)
PD_0	112	32	ECS#2 (3)
PD_2	113	33	PD_1
(4) LBO#	114	34	PD_3
GND	115	35	GND
CLK_0	116	36	CLK_1 (2)
GND	117	37	GND
D_{63}	118	38	D_{62}
V_{CC5}	119	39	V_{CC3}
D_{61}	120	40	D_{60}
D_{59}	121	41	D_{58}
D_{57}	122	42	D_{56}
GND	123	43	GND
D_{55}	124	44	D_{54}
D_{53}	125	45	D_{52}
D_{51}	126	46	D_{50}
D_{49}	127	47	D_{48}
GND	128	48	GND
D_{47}	129	49	D_{46}
D_{45}	130	50	D_{44}
D_{43}	131	51	D_{42}
V_{CC5}	132	52	V_{CC3}
D_{41}	133	53	D_{40}
D_{39}	134	54	D_{38}
D_{37}	135	55	D_{36}
GND	136	56	GND
D_{35}	137	57	D_{34}
D_{33}	138	58	D_{32}
D_{31}	139	59	D_{30}
V_{CC5}	140	60	V_{CC3}
D_{29}	141	61	D_{28}
D_{27}	142	62	D_{26}
D_{25}	143	63	D_{24}
GND	144	64	GND
D_{23}	145	65	D_{22}
D_{21}	146	66	D_{20}
D_{19}	147	67	D_{18}
V_{CC5}	148	68	V_{CC3}
D_{17}	149	69	D_{16}
D_{15}	150	70	D_{14}
D_{13}	151	71	D_{12}
GND	152	72	GND
D_{11}	153	73	D_{10}
D_9	154	74	D_8
D_7	155	75	D_6
V_{CC5}	156	76	V_{CC3}
D_5	167	77	D_4
D_3	158	78	D_2
D_1	159	79	D_0
GND	160	80	GND

LOW PROFILE CARD EDGE MODULE
TOP VIEW

NOTES: 3518 drw 03

1. These pins are reserved for 11-bit tag versions of these modules.
2. These pins are no connects for the IDT7MPV6204/05.
3. These pins are connected only for the 256KB module versions. If this module is not used as a 256KB upgrade to an existing 256KB already present in the system, then these pins should be tied to GND.
4. This version of the 7MPV6204/05/6306/08 does not have the LBO# feature. This pin is tied to a 4.7KΩ pull-up resistor.

15

PIN NAMES

$A_3 - A_{18}$	Address Inputs
$D_0 - D_{63}$	Cache Data Inputs/Outputs
$TIO_0 - TIO_7$	Tag Inputs/Outputs
OE#	Cache Data Output Enable Input
TWE#	Tag Write Enable Input
$WE\#_0 - WE\#_7$	Cache Data Write Enable Inputs
CS#	Cache Data Chip Enable Input
CADSC#	Cache Address Status Input
CADSP#	Processor Address Status Input
CADV#	Burst Address Advance
GW#	Global Write Input
BWE#	Byte Write Enable Input
ECS#1	Expansion Chip Select Input
ECS#2	Expansion Chip Select Output
$CLK_0 - CLK_1$	Clock Inputs
$PD_0 - PD_3$	Presence Detect Pins
F0	Special Function
RESET#	Host bus reset signal
H/WR#	Host bus W/R# signal
NC	No Connect
GND	Ground
V_{CC5}	5 Volt Power Supply
V_{CC3}	3.3 Volt Power Supply

3518 tbl 04

PRESENCE DETECT TABLE

PD3	PD2	PD1	PD0	Module
NC	NC	NC	NC	No cache present
NC	GND	NC	NC	IDT7MPV6204/5
GND	GND	NC	NC	IDT7MPV6306/8

3518 tbl 05

SRAM ACCESS TIMES

Module Speed	Burst[1]	Tag
66MHz	7.0ns	15ns

NOTE:
1. Burst RAMs are measured by Clock to Data Out (t_{CD}).

3518 tbl 06

CAPACITANCE (IDT7MPV6204/05,6306/08)[1, 2]

(T_A = +25°C, f = 1.0 MHz)

Symbol	Parameter	Condition	Max.	Unit
C_{IN1}	Input Capacitance (Address)	V_{IN} = 0V	20/30	pF
C_{IN2}	Input Capacitance (CA_3-CA_4)	V_{IN} = 0V	—	pF
C_{IN3}	Input Capacitance (OE#)	V_{IN} = 0V	15/25	pF
C_{IN4}	Input Capacitance (WE#, TWE#)	V_{IN} = 0V	8	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	10/20	pF

NOTES:
1. These parameters are guaranteed by design but not tested.
2. These parameters are maximum values.

3518 tbl 07

DC ELECTRICAL CHARACTERISTICS

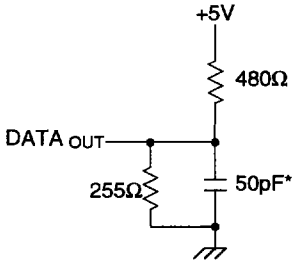
(V_{CC5} = 5.0V ± 5%, V_{CC3} = 3.3V ± 10%, T_A = 0°C to 70°C)

Symbol	Parameter	Test Condition	Min.	6204/05,6306/08 Max.	Unit
$\|I_{LI}\|$	Input Leakage Current (Address)	V_{CC} = Max, V_{IN} = GND to V_{CC}	—	30	µA
$\|I_{LI}\|$	Input Leakage Current (Data and Control)	V_{CC} = Max, V_{IN} = GND to V_{CC}	—	10	µA
$\|I_{LO}\|$	Output Leakage Current	V_{OUT} = 0V to V_{CC}, V_{CC} = Max.	—	10	µA
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min.	—	0.4	V
V_{OH}	Output HighVoltage	I_{OH}= –4mA, V_{CC} = Min.	2.4	—	V
I_{CC3}	Operating 3.3V Power Supply Current	V_{CC3} = Max., $\overline{CE} \leq V_{IL}$, f = f_{MAX}, Outputs Open	—	40	mA
I_{CC5}	Operating 5V Power Supply Current	V_{CC5} = Max., $\overline{CE} \leq V_{IL}$, f = f_{MAX}, Outputs Open	—	260	mA

AC TEST CONDITIONS – 5V POWER SUPPLY

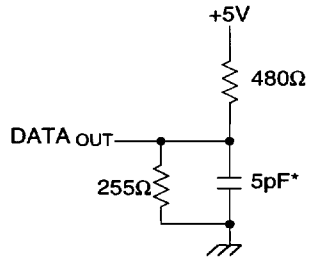
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

3518 tbl 09



*including scope and jig capacitances

Figure 1. Output Load



*including scope and jig capacitances

Figure 2. Output Load
(for t_{OHZ}, t_{CHZ}, t_{OLZ} and t_{CLZ})

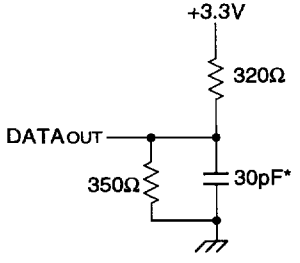
3518 drw 04

3518 drw 05

AC TEST CONDITIONS – 3.3V POWER SUPPLY

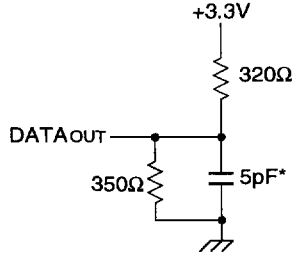
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 3 and 4

3150 tbl 10



*including scope and jig capacitances

Figure 3. Output Load



*including scope and jig capacitances

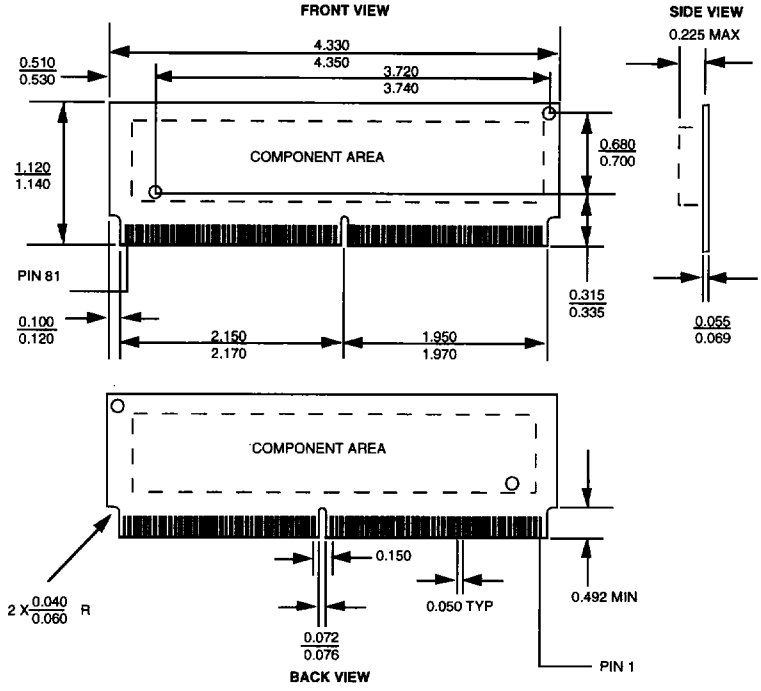
Figure 4. Output Load
(for t_{OHZ}, t_{CHZ}, t_{OLZ} and t_{CLZ})

3518 drw 06

3518 drw 07

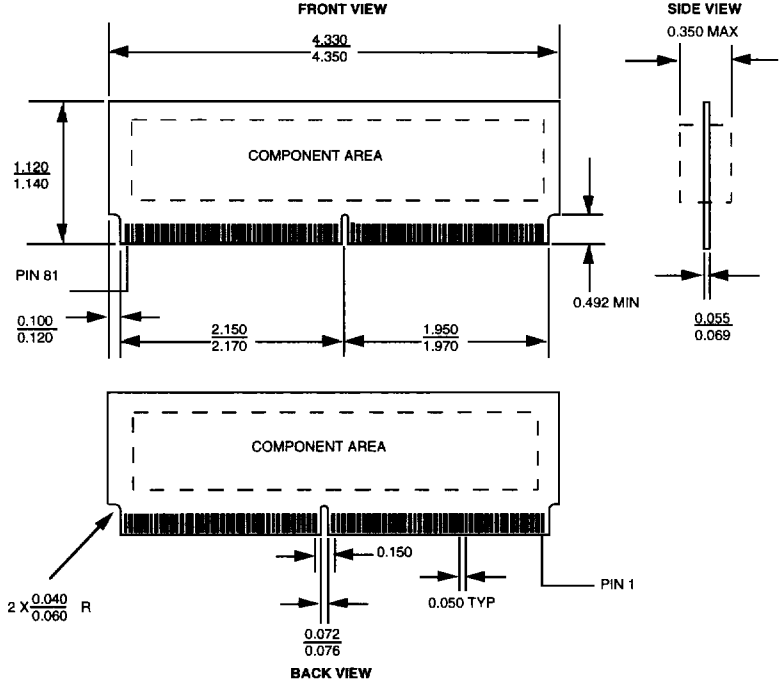
15

PACKAGE DIMENSIONS - IDT7MPV6204/5



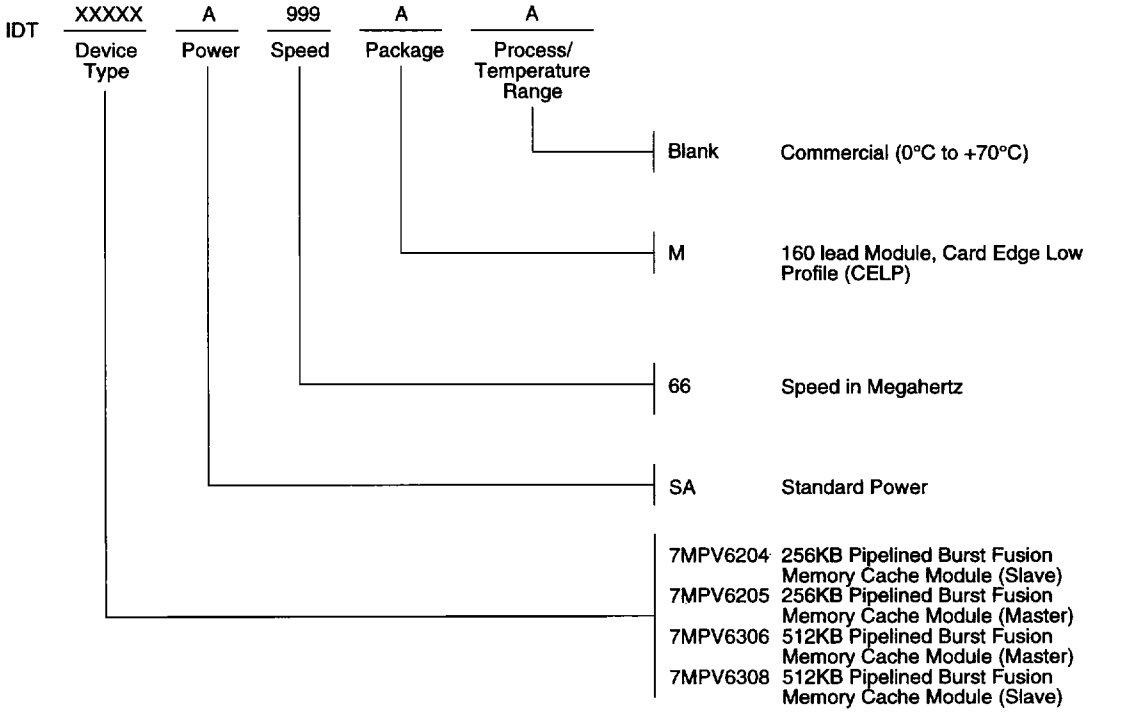
3518 drw 08

PACKAGE DIMENSIONS - IDT7MPV6306/8



3518 drw 09

ORDERING INFORMATION



3518 drw 10

15