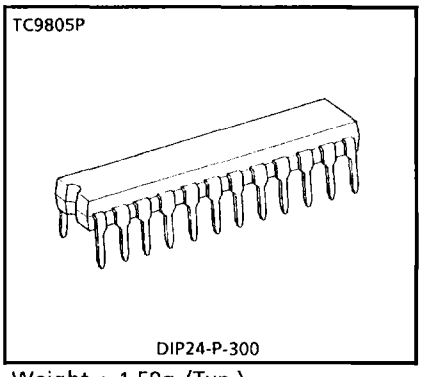
TC9805P

TENTATIVE DATA

TC9805P is a 24-pin CMOS programmable logic device (PLD) based on EEPROM cells. It has a zero-standby function. Designed using Toshiba's original technology, this device features low power dissipation and inputs that are compatible with TTL, NMOS, and CMOS output voltage levels.

It has both AND and OR arrays which the user can program like a field programmable logic array (FPLA). TC9805P consists of four blocks divided into macro cells made up of 2-bit memory cells containing D-type flip/flops (registers). Sync operation is implemented in units of blocks with up to four clocks.

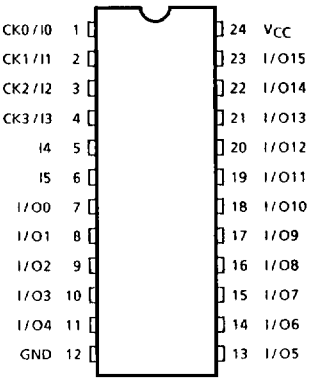


Weight : 1.50g (Typ.)

FEATURES

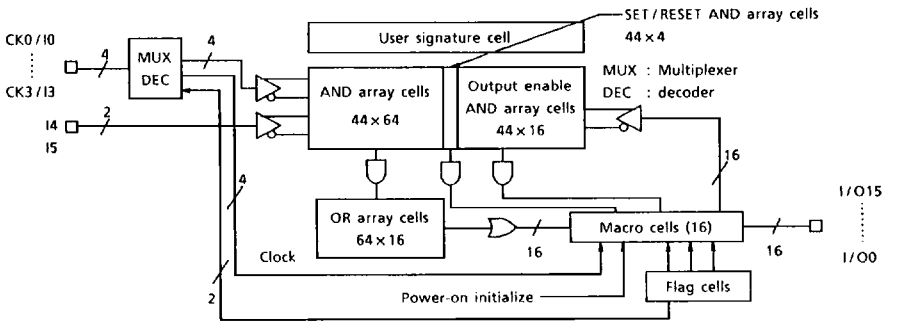
- Architecture ..... 84 AND terms
  16 OR terms
  16 macro cells with registers
  (Set/reset in async enable)
- Security cell ..... Protection of proprietary information
- Signature word ..... 84 bits for user ID code or inventory control
- High speed operation ..... t_{pd} (input-output) = 33ns (Typ.)
  t_{co} (clock-output) = 8ns (Typ.)
- Low power dissipation ..... I_{CC} (standby) = 4μA (max. @25°C)
- Wide operating voltage range ..... $V_{CC} = 5 \pm 0.25V$
- Programmable clock ..... 1-4 clock pins
- Package ..... 24-pin plastic DIP

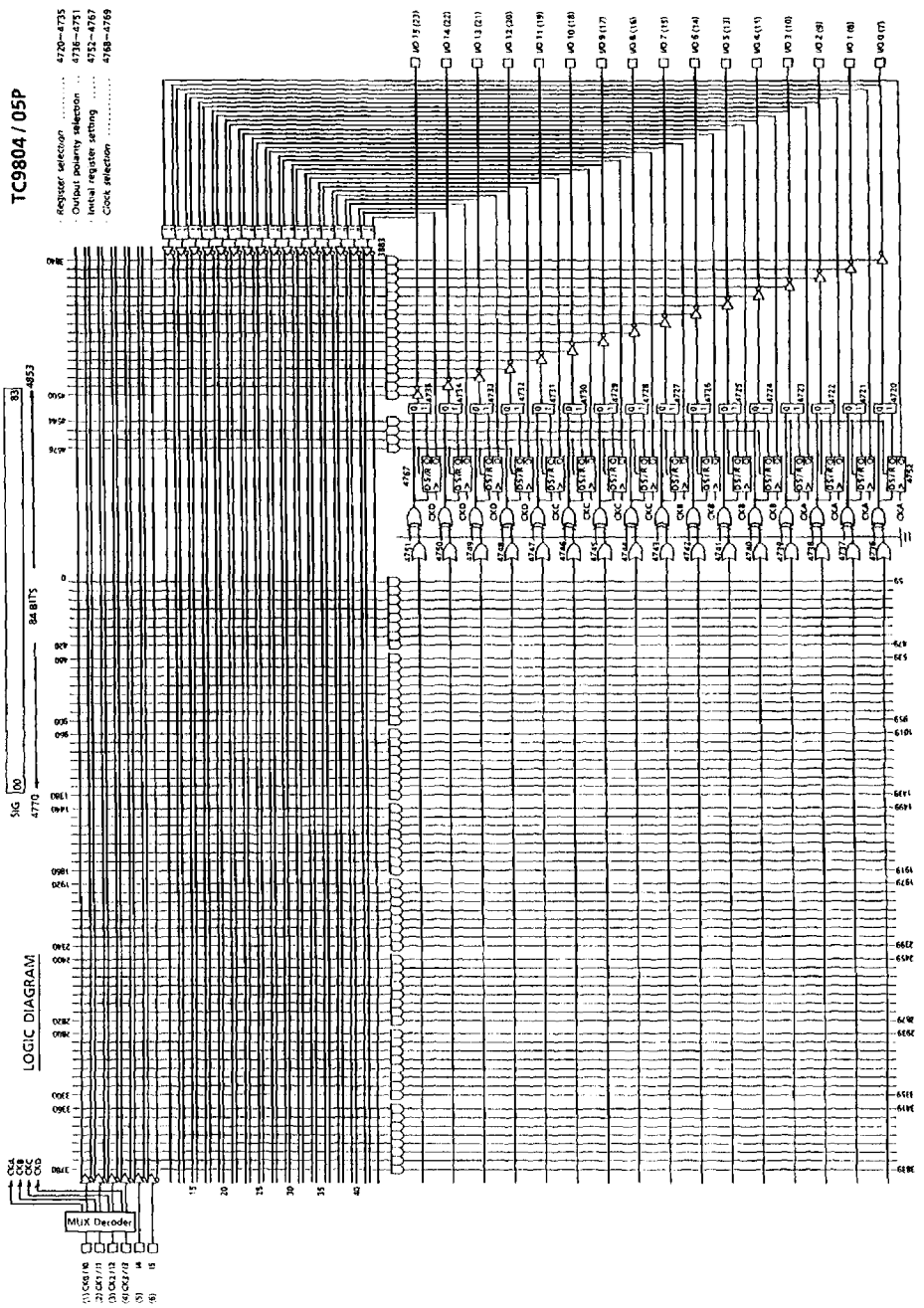
PIN NAMES & FUNCTIONS



CK0/I0~CK3/I3 ..... Clock input (when register is selected)
I4, I5 ..... Dedicated to input
I/O0~I/O15 ..... Input/Output (with register output)

FUNCTION DIAGRAM




TC9804 / 05P
LOGIC DIAGRAM
MUX Decoder
Register selection
Output polarity selection
Initial register setting
Clock selection
84 BITS

ARCHITECTURE

1. MEMORY CELLS

Programmable memory cells are divided into the following six types : AND array, OR array, output control array, flag, user signature, and register set/reset control array.
Setting program data to 1 disconnects signals to an AND/OR array : setting to 0 connects.

(1) AND array (44 x 64)

Total of 84 product terms (64 AND terms, 16 output control terms, and 4 register set/reset control terms)

(2) OR array (64 x 16)

64 AND terms input to 16 OR terms.

(3) Output control array (44 x 16)

Output from this array enables CMOS output (I/O0~I/O15).

(4) Register set/reset control array (44 x 4)

16 macro cells with D-type flip/flops are divided into four blocks. AND terms are provided with each block. Any input pin can be set to sync set/reset for a block. When the AND output of signals input to this cell array becomes high, initial states for registers are set.

(5) Flag cell

A. Output polarity selection cell ..... 16 bits

B. Register selection cell ..... 16 bits

C. Initial register setting cell ..... 16 bits

D. Security cell ..... 1 bit

E. Clock select cell ..... 2 bits

(6) User signature cell

User can program a 84-bit memory array for a variety of uses including ID codes, inventory control, and revision number.
Programming the security bit (security cell) disables access of cells other than the signature cell.

2. Macro cells

TC9805 has 16 macro cells containing D-type flip / flops (register).

(1) Output polarity of OR array

Sixteen exclusive OR gates control the output polarity of the OR array. These gates are user programmable : setting program data to 1 inputs the output signal from the OR array as inverted ; setting program data to 0, as non-inverted.

(2) Register selection

The sixteen output registers can be independently selected. Setting the program data to 1 selects an output register ; setting to 0 does not select an output register. When an output register is selected, the CK / I0 pin (pin 1) is automatically set to clock input. If an output register is not selected, pin 1~4 (like I4, I5) are set to dedicated data input. The register operates when the clock pulse goes positive. Clock division (program data) is determined according to the number of clocks and register selection.

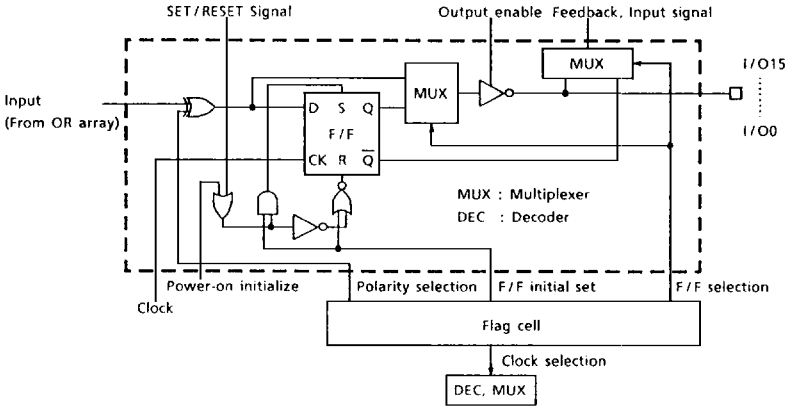
(3) Initial state of registers at power-up

The user can program reset or preset of register outputs at power-up. Setting program data to 1 presets register output ; setting to 0 resets register output. This function can only be used when registers are selected.

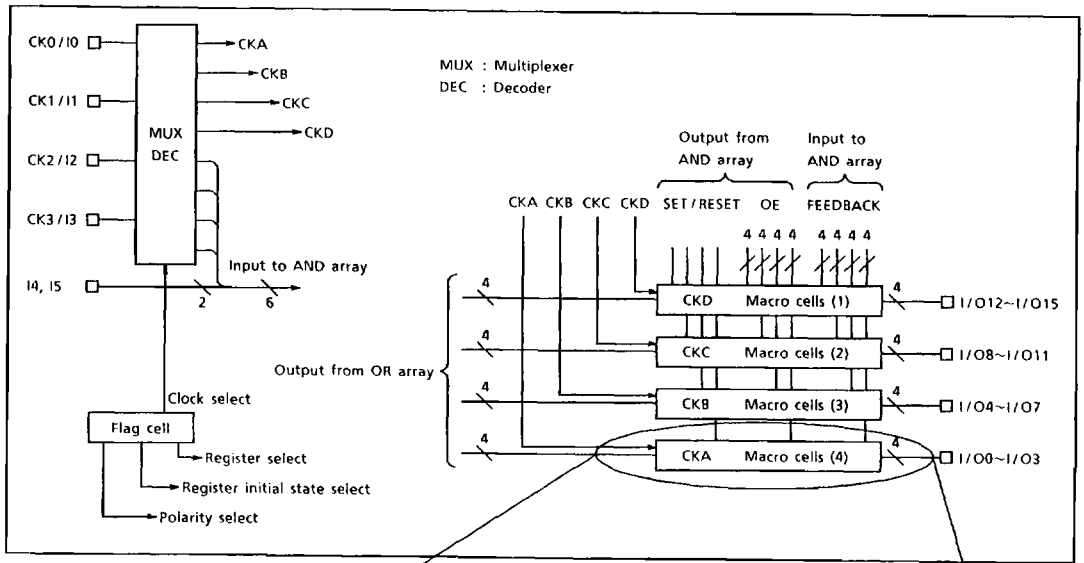
(4) Clock Select

16 macro cells with built-in output registers use a 2-bit memory cell (clock select cell) to offer three patterns of clock operation : pattern where all 16 registers are synchronized with one clock, pattern where registers are divided into two and they are in sync with two clocks, and pattern where registers are divided into four and they are in sync with four clocks.

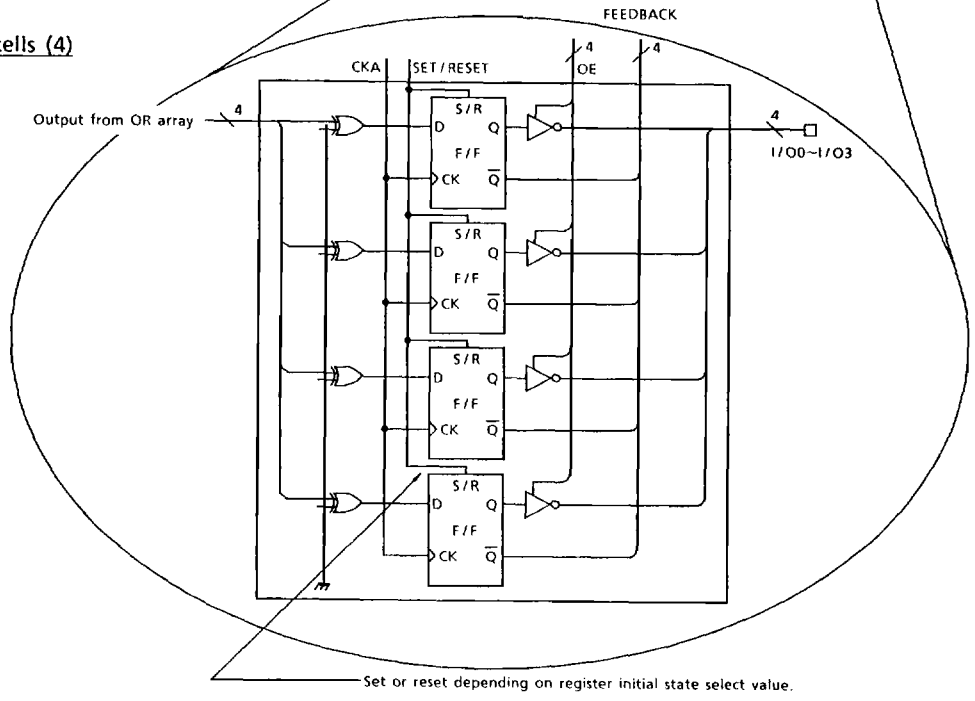
Macro cell



3. Clock Division Operation



Macro cells (4)



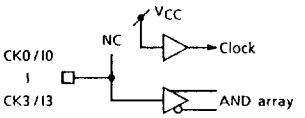
Clock division operating modes

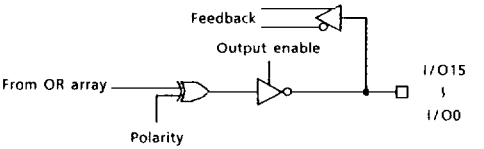
Mode	Program data	Internal clock			
		CKA	CKB	CKC	CKD
0	(0, 0)	—	—	—	—
1	(0, 1)	CK0	CK0	CK0	CK0
2	(1, 0)	CK0	CK0	CK1	CK1
3	(1, 1)	CK0	CK1	CK2	CK3

There are four clock division operating modes. Modes are selected using the clock select cell program data. The program data are determined according to the number of clocks and register selection.

(1) Mode 0

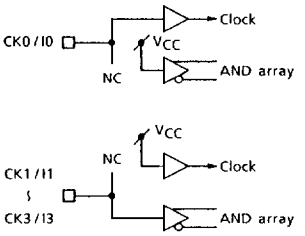
Clocks input to the CK0/I0 to CK3/I3 pins are input to AND array ; not to flip/flop.

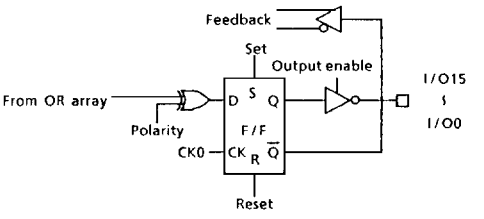




(2) Mode 1 (16-bit sync mode)

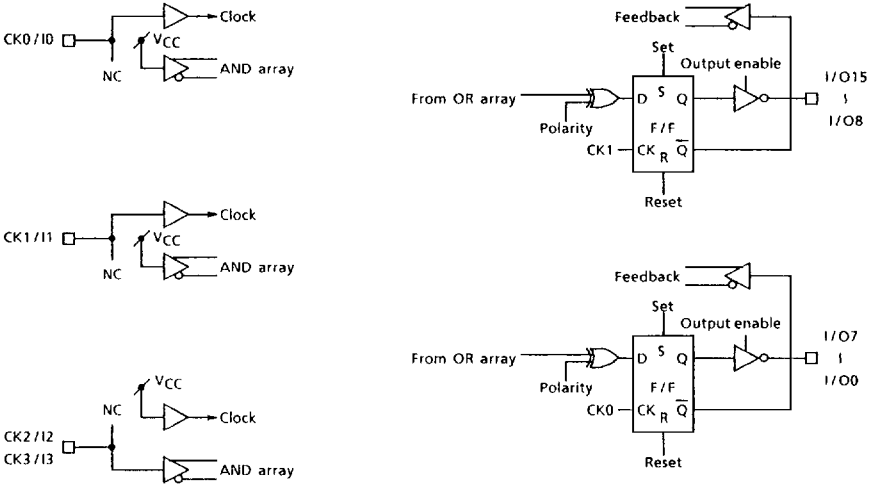
Clock input to the CK0/I0 pin is input to internal clocks, CKA, CKB, CKC, and CKD. Then the clocks are input to flip/flop of macro cells (1) to (4), resulting in maximum of 16-bit sync operation. At this time, input to pins CK1/I1 to CK3/I3 which are not used as clocks are input to the AND array.





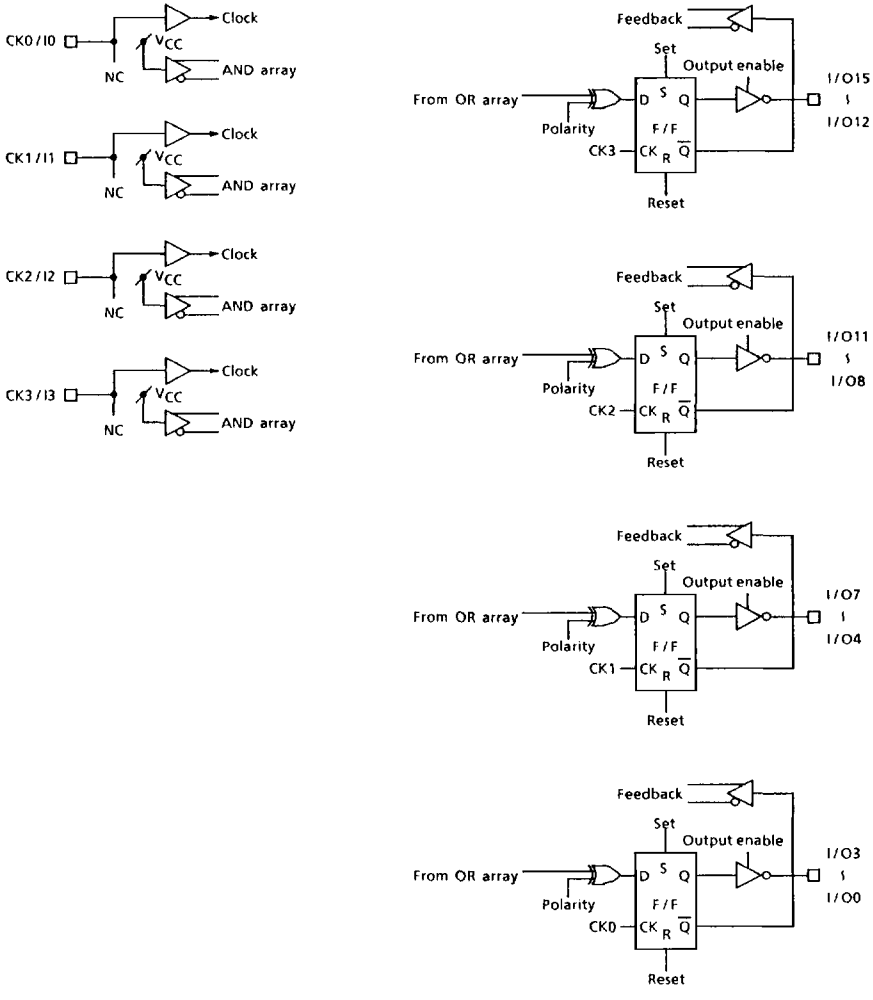
(3) Mode 2 (8-bit sync mode)

Clocks are input to the CK0/I0 and CK1/I1 pins. Clock input to the CK0/I0 pin is input to internal clocks, CKA and CKB, then input to the flip/flops of macro cells (3) and (4). Clock input to the CK1/I1 pin is input to internal clocks, CKC and CKD, then input to the flip/flops of macro cells (1) and (2). Up to 8-bit sync operation is performed at each clock. At this time, input to the CK2/I2 to CK3/I3 pins which are not used as clocks is input to the AND array.



(4) Mode 3 (4-bit sync mode)

The CK0/I0, CK1/I1, CK2/I2, and CK3/I3 pins are used for clock input. Clock input to the CKA is input to the flip/flop of macro cell (4). Clock input to the CKB is input to the flip/flop of macro cell (3). Clock input to the CKC is input to the flip/flop of macro cell (2). Clock input to the CKD is input to the flip/flop of macro cell (1). Up to 4-bit sync operation is performed at each clock.



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5~7	V
DC Input Voltage	V_{IN}	−0.5~V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5~V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35	mA
DC V_{CC}/Ground Current	I_{CC}	±70	mA
Power Dissipation	P_D	500 (DIP) *	mW
Storage Temperature	T_{stg}	−65~150	°C
Lead Temperature (10s)	T_L	300	°C

* 500mW in the range of Ta = −40~65°C. From Ta = 65°C to 85°C a derating factor of −10mW/°C should be applied up to 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	4.75~5.25	V
Input Voltage	V_{IN}	0~V_{CC}	V
Output Voltage	V_{OUT}	0~V_{CC}	V
Operating Temperature	T_{opr}	−40~85	°C
Input Rise and Fall Time	t_r, t_f	0~500 (V_{CC} = 5.0 ± 0.25V)	ns

DC ELECTRICAL CHARACTERISTICS

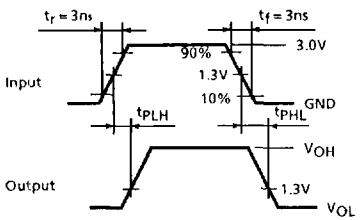
PARAMETER	SYMBOL	TEST CIRCUIT	TEST CONDITION		V_{CC}	Ta = 25°C MIN.	Ta = 25°C TYP.	Ta = 25°C MAX.	Ta = −40~85°C MIN.	Ta = −40~85°C MAX.	UNIT
High-level input voltage	V_{IH}	—			5.0 ± 0.25	2.0	—	—	2.0	—	V
Low-level input voltage	V_{IL}	—			5.0 ± 0.25	—	—	0.8	—	0.8	V
High-level output voltage	V_{OH}	—	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −20μA	4.75	4.65	4.75	—	4.65	—	V
				I_{OH} = −4mA	4.75	4.43	4.56	—	4.38	—	
Low-level output voltage	V_{OL}	—	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 20μA	4.75	—	0.0	0.1	—	—	V
				I_{OL} = 4mA	4.75	—	0.18	0.26	—	0.33	
3-State output off-state current	I_{OZ}	—	V_{IN} = V_{IH} or V_{IL}, V_{OUT} = V_{CC} or GND		5.25	—	—	±0.5	—	±5.0	μA
Input leakage current	I_{IN}	—	V_{IN} = V_{CC} or GND		5.25	—	—	±0.1	—	±1.0	
Quiescent current	I_{CCSB}	—	V_{IN} = V_{CC} or GND Standby		5.25	—	—	4.0	—	40.0	μA
Operating current	I_{CCOP}	—	f_{IN} = 1MHz Operating		5.25	—	—	—	—	40.0	mA

AC ELECTRICAL CHARACTERISTICS (C_L = 25pF, Input $t_r = t_f$ = 3ns)

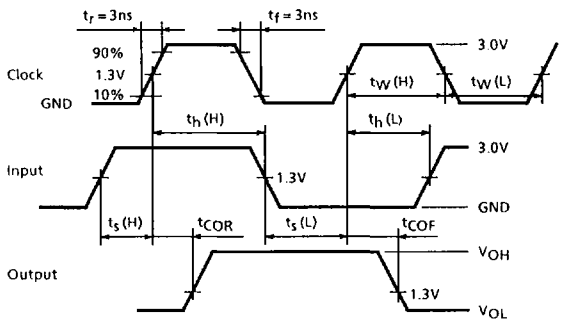
PARAMETER	SYM-BOL	TEST CIR-CUIT	TEST CONDITION		Ta = 25°C			Ta = −40 ~85°C		UNIT
				V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time (Input, I/O-Output)	t_{PLH} t_{PHL}	—		5 ± 0.25	—	33	50	—	55	ns
Propagation Delay Time (Clock-Output)	t_{COR} t_{COF}	—		5 ± 0.25	—	8	12	—	14	ns
Output Enable Time	t_{PZL} t_{PZH}	—		5 ± 0.25	—	26	40	—	44	ns
Output Disable Time	t_{PLZ} t_{PHZ}	—		5 ± 0.25	—	21	32	—	37	ns
Minimum Pulse Width	t_W (L) t_W (H)	—		5 ± 0.25	—	—	—	—	—	ns
Minimum Set-up Time	t_S	—		5 ± 0.25	—	—	42	—	47	ns
Minimum Hold Time	t_H	—		5 ± 0.25	—	—	0	—	0	ns
Minimum Removal Time	t_{rem}	—		5 ± 0.25	—	19	29	—	33	ns
Maximum Clock Frequency	f_{MAX}	—		5 ± 0.25	14	—	—	12	—	MHz

Switching Characteristic Test Waveform

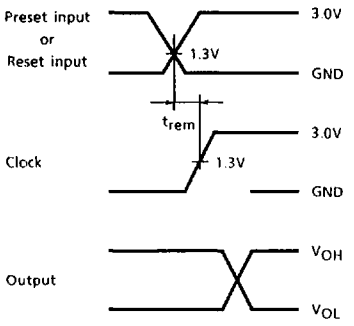
1) t_{PD} (t_{PLH}, t_{PHL})



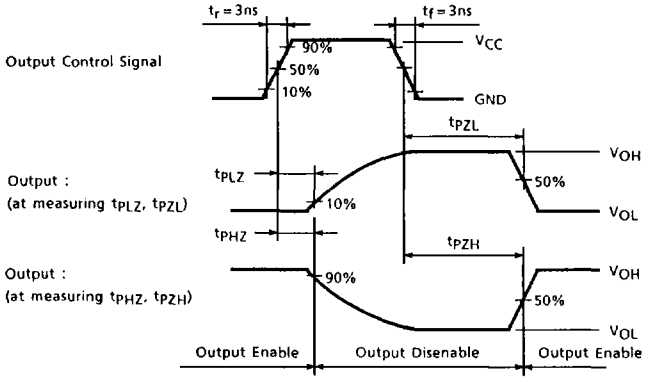
2) t_{CO} (t_{COR}, t_{COF}, t_s, t_h, t_W)



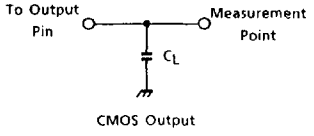
3) t_{rem}

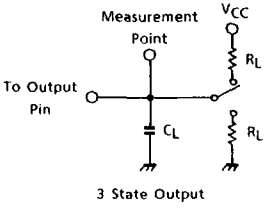


4) t_{PLZ}, t_{PHZ}, t_{PZL}, t_{PZH}



5) Output Test Connection Diagram





Note) C_L includes the capacitance of probe.