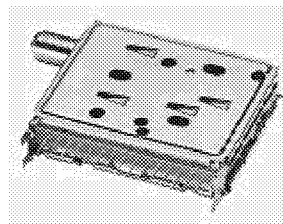


Type : **DC7L**

Part No.: **ENGA**□□□□□□

DC7L is a small size and high performance Digital DBS tuner for Digital Transmission Satellite Receiver.

Advanced frequency design technology and high density mounting technology have been applied to this tuner.



Features

- Analog I/Q detector output
- Low Phase noise (- 75 dBc / Hz)
Good stability against vibration
- High gain (0.7 Vp-p output) and low distortion
(30 dBc)
- Available in vertical mounting type and horizontal mounting type

Recommended Applications

- Digital DBS receiver

■ Performance Specifications, Summary

	Standard	Note
1. RF Input Frequency	950 to 2150 MHz	
2. Input Level	- 70 to - 25 dBm	
3. Input Impedance	75 Ω Unbalanced	
4. Noise Figure	12 dB max.	
5. Image Rejection	30 dB min.	
6. Tuning System	PLL (1 st C)	PLL (3 wire)
7. IF Frequency	479.5 MHz	
8. IF Filter Band Width	36 MHz	Other Band width & Switch Type
9. AFC	AFC > \pm 4 MHz	Fixed Type
10. Prescaler Output Level	1 / 32, 0.8 Vp-p min.	
11. Output Level	0.7 Vp-p	
12. I / Q Balance	\pm 0.5 $^{\circ}$ typ.	
13. I / Q Phase	\pm 0.5 dB typ.	
14. Phase Noise off set 10 kHz	- 75 dBc / Hz typ.	
15. Supply Voltage	5.28 V	

■ Dimensions in mm (not to scale)

● DC7L

3/8 UNEF-2A

14.2

12.5

1.7

55.6

LABEL

IF IN

15.2

47.2

38.0

25.0

1.3

3.0

11.4

8.3

7.2

0.6

1.0

0.5

0.5

1.0

1.0

1.5

1

2

3

4

5

6

7

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■ TERMINAL SUPPLY VOLTAGE		
No.	Terminal Name	Supply Voltage
1	LNB+B	25 V max.
2	NC	—
3	+5 V DC	+5.0 ± 5% V(± 0.25 V)
4	AGC	0 to +5 V
5	AFC	+5.0 ± 3 V
6	Q	—
7	GND	—
8	I	—
9	+5 V DC	+5.0 ± 5% V(± 0.25 V)
10	PS OUT	—
11	+5 V DC	+5.0 ± 5% V(± 0.25 V)
12	BT	+28.0 ± 5% V(± 1.4 V)
13	ADDR	—
14	SDA	—
15	SCL	—

■ Block Diagram (DC7L)

