

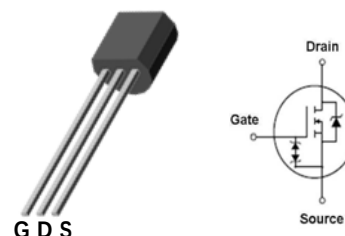
SWITCHING REGULATOR APPLICATION

Features

- High voltage: $BV_{DSS}=300V$ (Min.)
- Low gate charge: $Q_g=2.9nC$ (Typ.)
- Low drain-source On resistance: $R_{DS(on)}=8\Omega$ (Max.)
- Built-in protection zener diode
- RoHS compliant device

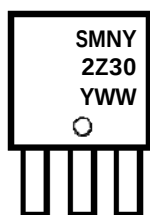
Ordering Information

Part Number	Marking	Package
SMNY2Z30	SMNY2Z30	TO-92



TO-92

Marking Information



Column 1, 2: Device Code
 Column 3: Production Information
 e.g.) YWW
 -. YWW: Date Code (year, week)

Absolute maximum ratings ($T_a=25^\circ C$ unless otherwise noted)

absolute maximum ratings (Ta = 25°C unless otherwise noted)

Characteristic	Symbol	Rating	Unit	
Drain-source voltage	V_{DSS}	300	V	
Gate-source voltage	V_{GSS}	±30	V	
Drain current (DC) *	I_D	$T_a=25^{\circ}C$	0.2	A
		$T_a=100^{\circ}C$	0.12	A
Drain current (Pulsed) *	I_{DM}	1	A	
Avalanche current (Note 2)	I_{AS}	1.3	A	
Single pulsed avalanche energy (Note 2)	E_{AS}	182.6	mJ	
Repetitive avalanche current (Note 1)	I_{AR}	0.2	A	
Repetitive avalanche energy (Note 1)	E_{AR}	1.5	mJ	
Power dissipation	P_D	0.6	W	
Junction temperature	T_J	150	°C	
Storage temperature range	T_{stg}	-55~150	°C	

* Limited only maximum junction temperature

Thermal Characteristics

Characteristic	Symbol	Rating	Unit
Thermal resistance, junction to ambient	$R_{th(j-a)}$	Max. 200	°C/W

Electrical Characteristics ($T_a=25^{\circ}\text{C}$ unless otherwise noted)

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Drain-source breakdown voltage	BV_{DSS}	$I_D=250\mu\text{A}$, $V_{GS}=0$	300	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$I_D=250\mu\text{A}$, $V_{DS}=V_{GS}$	1.5	2	2.5	V
Drain-source cut-off current	I_{DSS}	$V_{DS}=300\text{V}$, $V_{GS}=0\text{V}$	-	-	1	μA
Gate leakage current	I_{GSS}	$V_{DS}=0\text{V}$, $V_{GS}=\pm 10\text{V}$	-	-	± 10	μA
Drain-source on-resistance	$R_{DS(ON)}$	$V_{GS}=10\text{V}$, $I_D=100\text{mA}$	-	6	8	Ω
Forward transfer conductance (Note 3)	g_{fs}	$V_{DS}=10\text{V}$, $I_D=100\text{mA}$	-	0.4	-	S
Input capacitance	C_{iss}	$V_{DS}=25\text{V}$, $V_{GS}=0\text{V}$, $f=1\text{MHz}$	-	101	130	pF
Output capacitance	C_{oss}		-	15	20	
Reverse transfer capacitance	C_{rss}		-	3.2	5	
Turn-on delay time (Note 3,4)	$t_{d(on)}$	$V_{DD}=150\text{V}$, $I_D=0.2\text{A}$ $R_G=25\Omega$	-	5	-	ns
Rise time (Note 3,4)	t_r		-	17	-	
Turn-off delay time (Note 3,4)	$t_{d(off)}$		-	21	-	
Fall time (Note 3,4)	t_f		-	35	-	
Total gate charge (Note 3,4)	Q_g	$V_{DS}=240\text{V}$, $V_{GS}=10\text{V}$ $I_D=0.2\text{A}$	-	2.9	4.5	nC
Gate-source charge (Note 3,4)	Q_{gs}		-	0.4	-	
Gate-drain charge (Note 3,4)	Q_{gd}		-	0.7	-	

Source-Drain Diode Ratings and Characteristics ($T_a=25^{\circ}\text{C}$ unless otherwise noted)

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Source current (DC)	I_S	Integral reverse diode in the MOSFET	-	-	0.2	A
Source current (Pulsed)	I_{SM}		-	-	1	A
Forward voltage	V_{SD}	$V_{GS}=0\text{V}$, $I_S=8\text{A}$	-	-	1.4	V
Reverse recovery time (Note 3,4)	t_{rr}	$I_S=0.2\text{A}$, $V_{GS}=0\text{V}$ $dI_F/dt=100\text{A}/\mu\text{s}$	-	270	-	ns
Reverse recovery charge (Note 3,4)	Q_{rr}		-	0.27	-	μC

Gate to Source Zener Diode Characteristic ($T_a=25^{\circ}\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Gate-Source breakdown voltage	$I_G=\pm 1\text{mA}$, $V_{DS}=0\text{V}$	± 20	± 24	-	V

Note:

1. Repeated rating: Pulse width limited by safe operating area
2. $L=8.9\text{mH}$, $I_{AS}=8\text{A}$, $V_{DD}=50\text{V}$, $R_G=25\Omega$, Starting $T_J=25^{\circ}\text{C}$
3. Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$
4. Essentially independent of operating temperature typical characteristics

Electrical Characteristic Curves

Fig. 1 $I_D - V_{DS}$

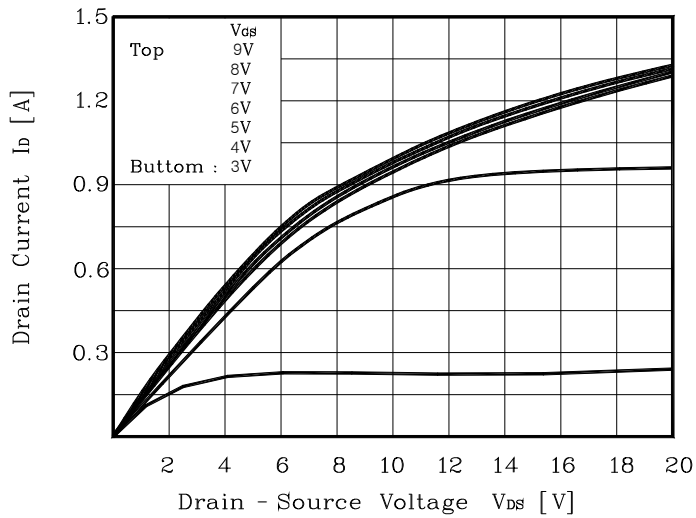


Fig. 2 $I_D - V_{GS}$

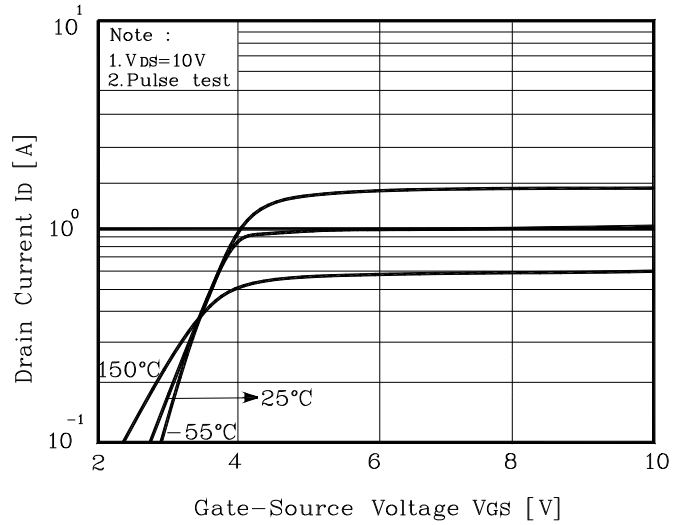


Fig. 3 $R_{DS(ON)} - I_D$

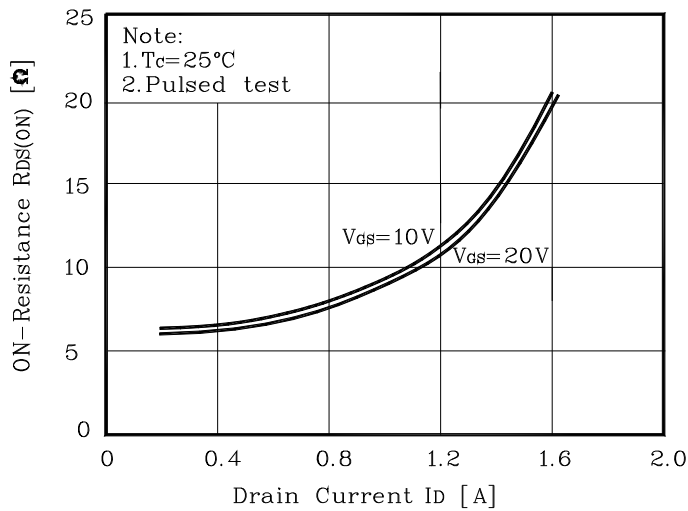


Fig. 4 $I_S - V_{SD}$

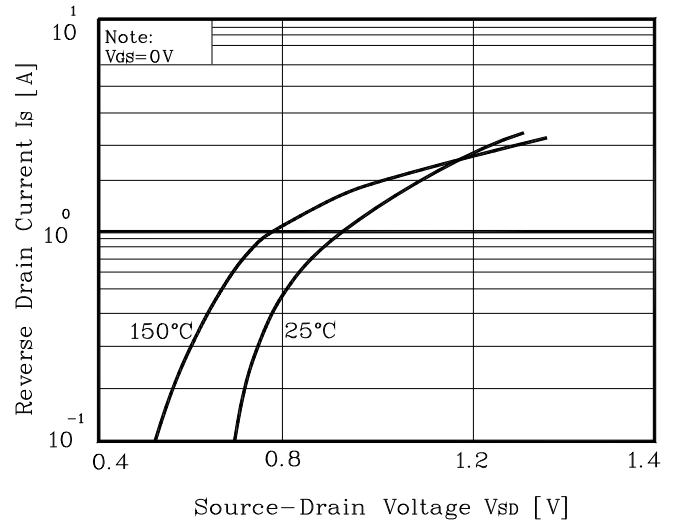


Fig. 5 Capacitance - V_{DS}

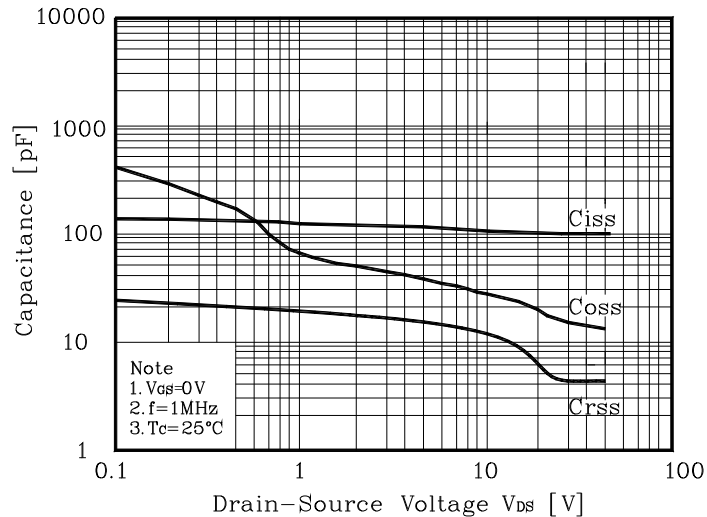
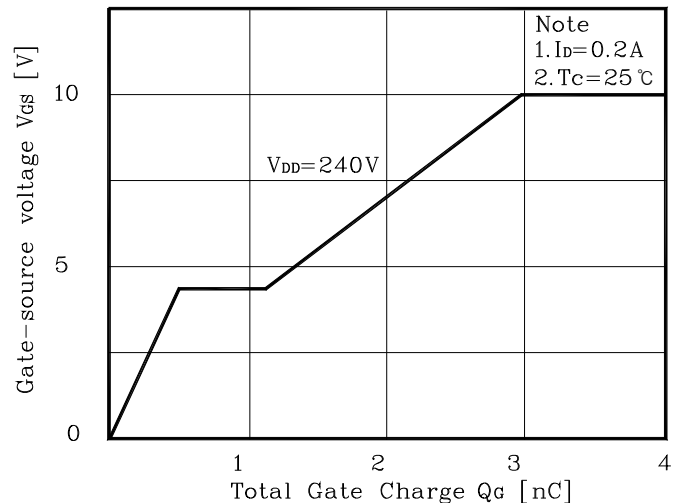


Fig. 6 $V_{GS} - Q_G$



Electrical Characteristic Curves (Continue)

Fig. 7 $BV_{DSS} - T_J$

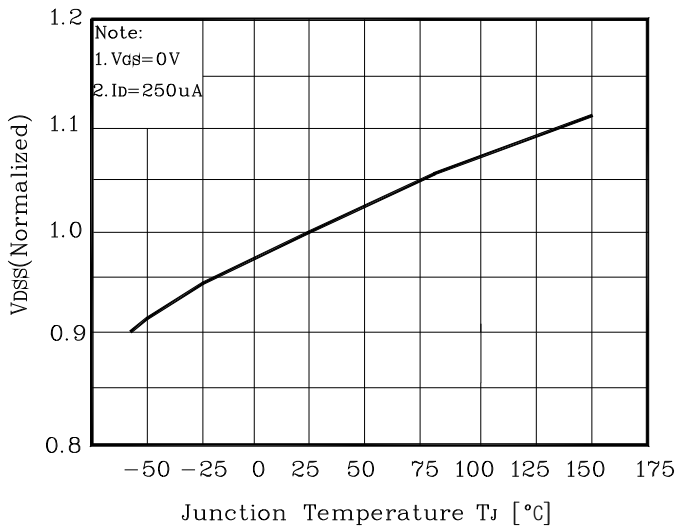


Fig. 8 $R_{DS(on)} - T_J$

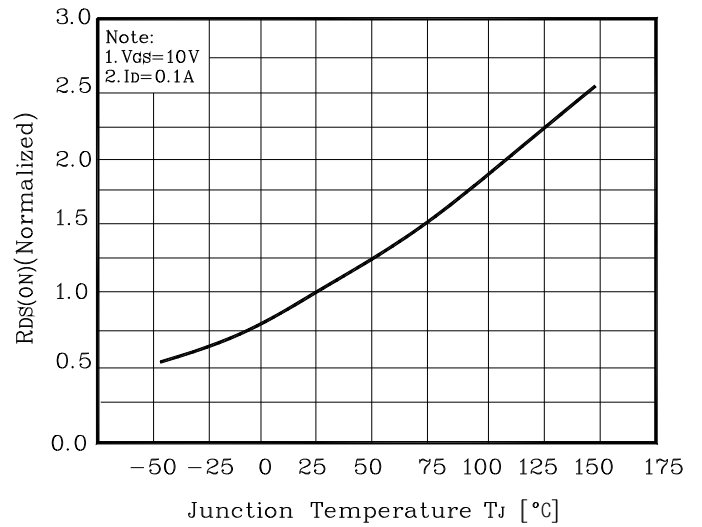


Fig. 9 $I_D - T_C$

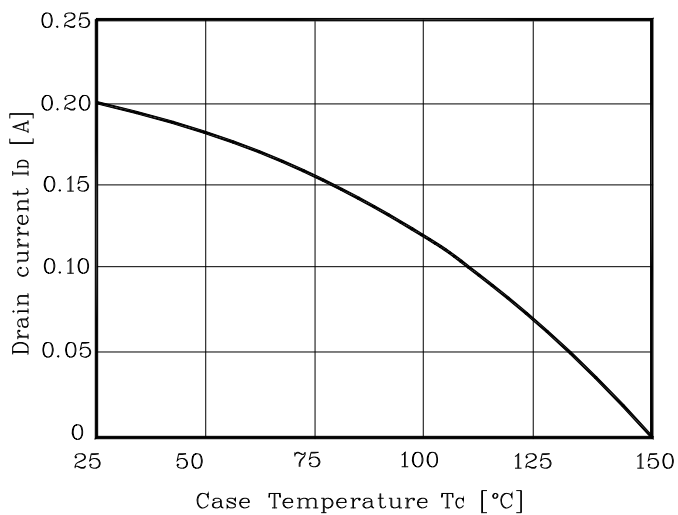


Fig. 10 Safe Operating Area

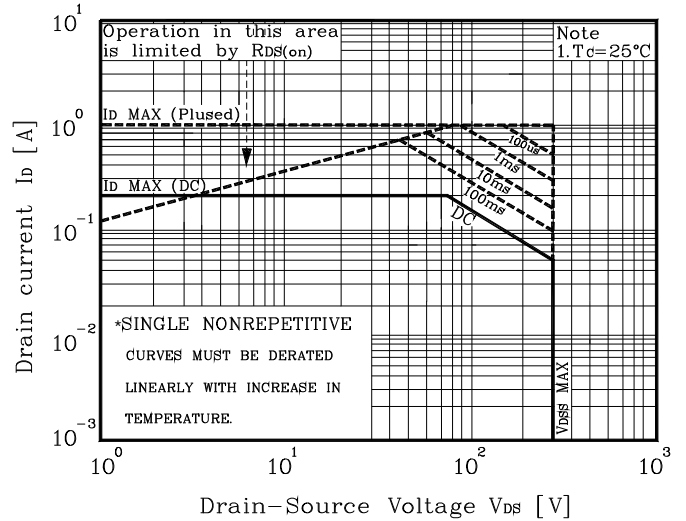


Fig. 11 Gate Charge Test Circuit & Waveform

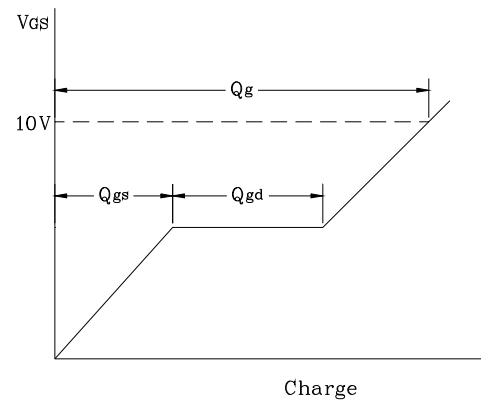
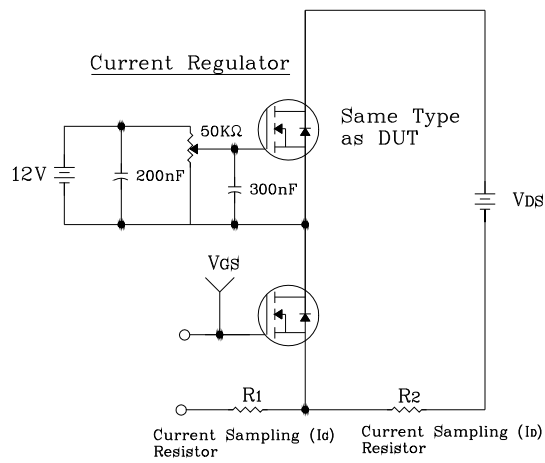


Fig. 12 Resistive Switching Test Circuit & Waveform

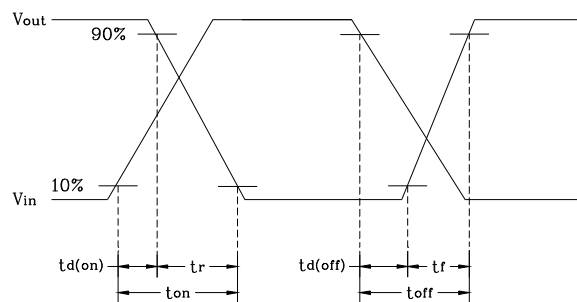
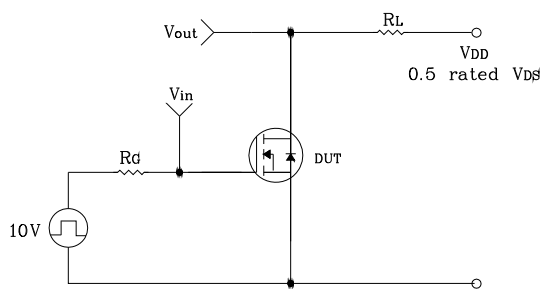


Fig. 13 E_{AS} Test Circuit & Waveform

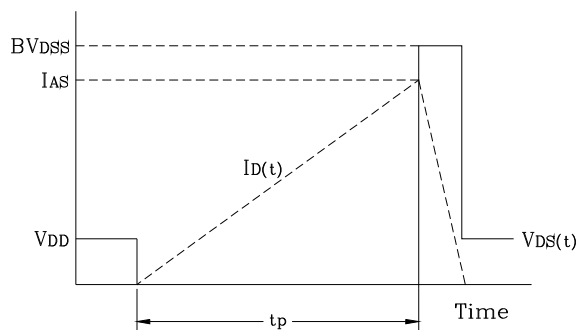
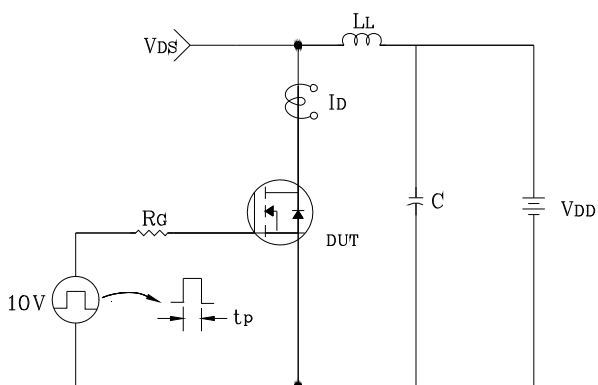
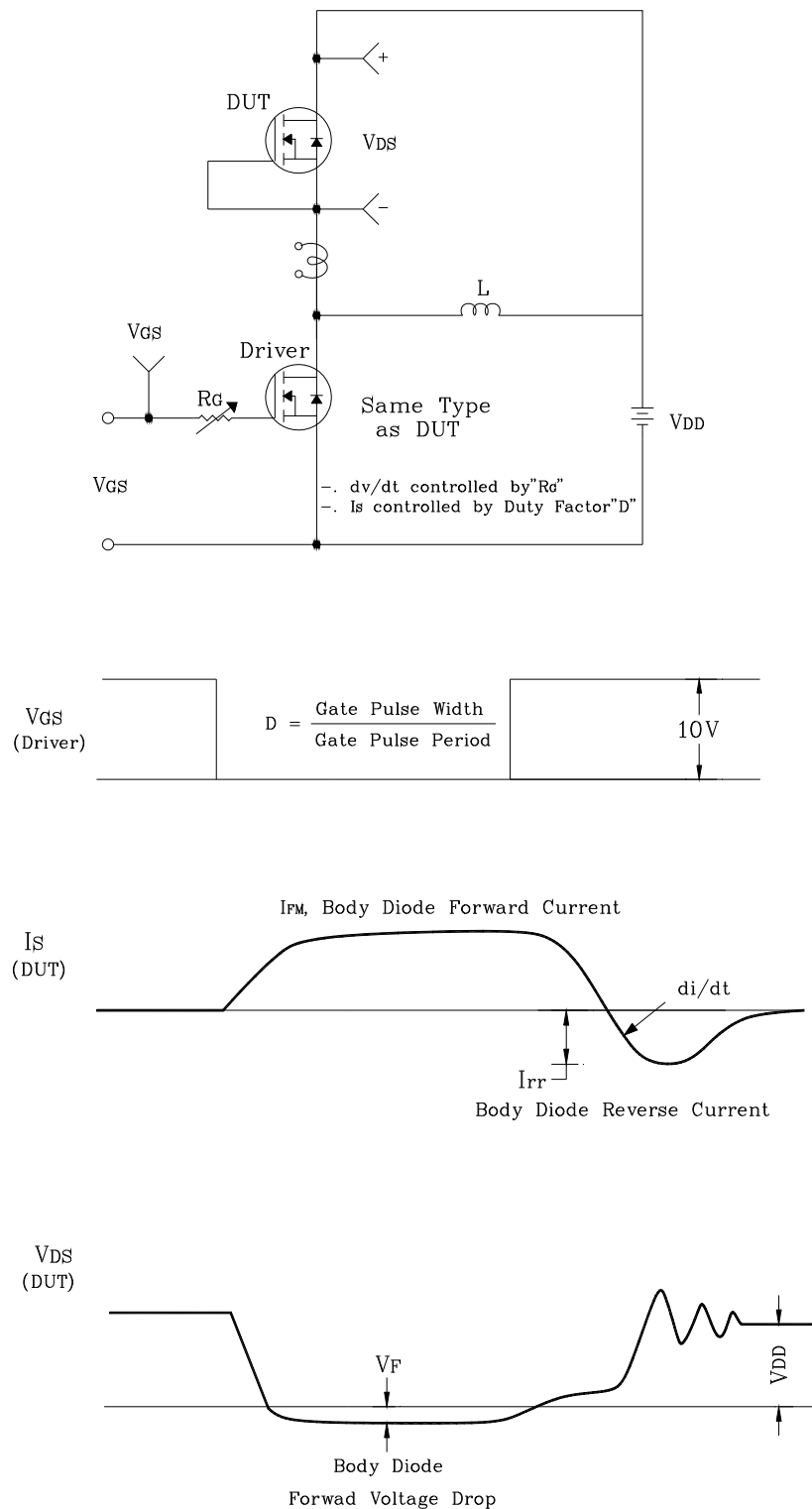


Fig. 14 Diode Reverse Recovery Time Test Circuit & Waveform



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