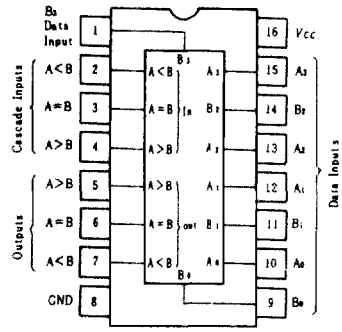
# HD74HC85 ● 4-bit Magnitude Comparator

The HD74HC85 is designed for high speed comparison of two four bit words. This circuit has eight comparison input, 4 for each word; three cascade inputs (A < B, A > B, A = B); and three decision outputs (A < B, A > B, A = B). The result of a comparison is indicated by a high level on one of the decision outputs. Thus it may be determined whether one word is "greater than," "less than," or "equal to" the other word. By connecting the outputs of the least significant stage to the cascade inputs of the next stage, words of greater than four bits can be compared. In addition the least significant stage must have a high level applied to the A = B input, and a low level to the A < B, and A > B inputs.

## ■ FEATURES

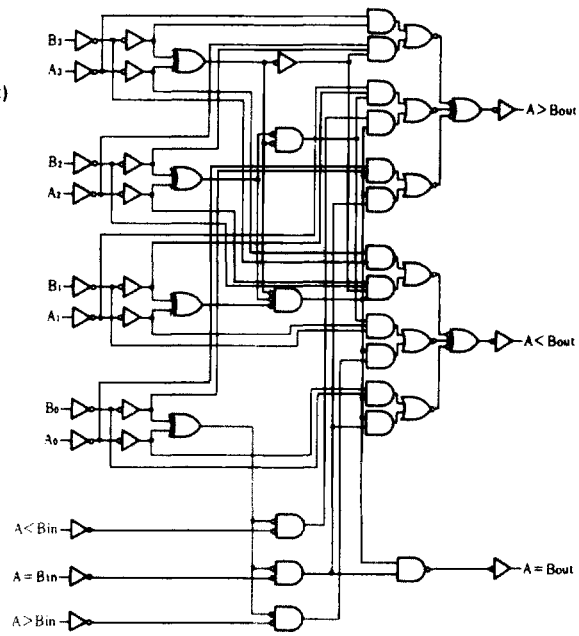
- High Speed Operation: $t_{pd}$ (Data Word Input to Output)= 20ns typ. ($C_L$=50pF)
- High Output Current: Fanout of 10 LSTTL Loads
- Wide Operating Voltage: $Vcc$=2~6V
- Low Input Current: 1μA max.
- Low Quiescent Supply Current: $Icc$ (static)=4μA max. ($Ta$=25°C)

## ■ PIN ARRANGEMENT




(Top View)

## ■ LOGIC DIAGRAM




## ■ FUNCTION TABLE

| Data Word Inputs | | | | Cascading Inputs | | | Outputs | | |
|---|---|---|---|---|---|---|---|---|---|
| $A_3$, $B_3$ | $A_2$, $B_2$ | $A_1$, $B_1$ | $A_0$, $B_0$ | A>Bin | A=Bin | A<Bin | A>Bout | A=Bout | A<Bout |
| $A_3>B_3$ | X | X | X | X | X | X | H | L | L |
| $A_3<B_3$ | X | X | X | X | X | X | L | L | H |
| $A_3=B_3$ | $A_2>B_2$ | X | X | X | X | X | H | L | L |
| $A_3=B_3$ | $A_2<B_2$ | X | X | X | X | X | L | L | H |
| $A_3=B_3$ | $A_2=B_2$ | $A_1>B_1$ | X | X | X | X | H | L | L |
| $A_3=B_3$ | $A_2=B_2$ | $A_1<B_1$ | X | X | X | X | L | L | H |
| $A_3=B_3$ | $A_2=B_2$ | $A_1=B_1$ | $A_0>B_0$ | X | X | X | H | L | L |
| $A_3=B_3$ | $A_2=B_2$ | $A_1=B_1$ | $A_0<B_0$ | X | X | X | L | L | H |
| $A_3=B_3$ | $A_2=B_2$ | $A_1=B_1$ | $A_0=B_0$ | L | L | L | H | L | H |
| $A_3=B_3$ | $A_2=B_2$ | $A_1=B_1$ | $A_0=B_0$ | L | L | H | L | L | H |
| $A_3=B_3$ | $A_2=B_2$ | $A_1=B_1$ | $A_0=B_0$ | H | L | L | H | L | L |
| $A_3=B_3$ | $A_2=B_2$ | $A_1=B_1$ | $A_0=B_0$ | H | L | H | L | L | L |
| $A_3=B_3$ | $A_2=B_2$ | $A_1=B_1$ | $A_0=B_0$ | X | H | X | L | H | L |

## ■ DC CHARACTERISTICS

| Item | Symbol | $V_{CC}$(V) | Test Conditions | | $Ta$=25℃ min | typ | max | $Ta$=−40~+85℃ min | max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| Input Voltage | $V_{IH}$ | 2.0 | | | 1.5 | — | — | 1.5 | — | V |
| | | 4.5 | | | 3.15 | — | — | 3.15 | — | |
| | | 6.0 | | | 4.2 | — | — | 4.2 | — | |
| | $V_{IL}$ | 2.0 | | | — | — | 0.5 | — | 0.5 | V |
| | | 4.5 | | | — | — | 1.35 | — | 1.35 | |
| | | 6.0 | | | — | — | 1.8 | — | 1.8 | |
| Output Voltage | $V_{OH}$ | 2.0 | $V_{in}$=$V_{IH}$ or $V_{IL}$ | $I_{OH}$=−20μA | 1.9 | 2.0 | — | 1.9 | — | V |
| | | 4.5 | | | 4.4 | 4.5 | — | 4.4 | — | |
| | | 6.0 | | | 5.9 | 6.0 | — | 5.9 | — | |
| | | 4.5 | | $I_{OH}$=−4mA | 4.18 | — | — | 4.13 | — | |
| | | 6.0 | | $I_{OH}$=−5.2mA | 5.68 | — | — | 5.63 | — | |
| | $V_{OL}$ | 2.0 | $V_{in}$=$V_{IH}$ or $V_{IL}$ | $I_{OL}$=20μA | — | 0.0 | 0.1 | — | 0.1 | V |
| | | 4.5 | | | — | 0.0 | 0.1 | — | 0.1 | |
| | | 6.0 | | | — | 0.0 | 0.1 | — | 0.1 | |
| | | 4.5 | | $I_{OL}$=4mA | — | — | 0.26 | — | 0.33 | |
| | | 6.0 | | $I_{OL}$=5.2mA | — | — | 0.26 | — | 0.33 | |
| Input Current | $I_{in}$ | 6.0 | $V_{in}$=$V_{CC}$ or GND | | — | — | ±0.1 | — | ±1.0 | μA |
| Quiescent Supply Current | $I_{CC}$ | 6.0 | $V_{in}$=$V_{CC}$ or GND, $I_{out}$=0μA | | — | — | 4.0 | — | 40 | μA |

## ■ AC CHARACTERISTICS ($C_L$=50pF, Input $t_r$=$t_f$=6ns)

| Item | Symbol | $V_{CC}$(V) | Test Conditions | $Ta$=25℃ min | typ | max | $Ta$=−40~+85℃ min | max | Unit |
|---|---|---|---|---|---|---|---|---|---|
| Propagation Delay Time | $t_{PLH}$ $t_{PHL}$ | 2.0 | Data Word Input to Output (Except A=Bout) | — | — | 210 | — | 265 | ns |
| | | 4.5 | | — | 20 | 42 | — | 53 | |
| | | 6.0 | | — | — | 36 | — | 45 | |
| | $t_{PLH}$ $t_{PHL}$ | 2.0 | Data Word Input to A=Bout | — | — | 175 | — | 220 | ns |
| | | 4.5 | | — | 20 | 35 | — | 44 | |
| | | 6.0 | | — | — | 30 | — | 37 | |
| | $t_{PLH}$ $t_{PHL}$ | 2.0 | A=Bin to A=Bout | — | — | 125 | — | 155 | ns |
| | | 4.5 | | — | 12 | 25 | — | 31 | |
| | | 6.0 | | — | — | 21 | — | 26 | |
| | $t_{PLH}$ $t_{PHL}$ | 2.0 | Cascading Input to Output (Except A=Bout) | — | — | 155 | — | 195 | ns |
| | | 4.5 | | — | 14 | 31 | — | 39 | |
| | | 6.0 | | — | — | 26 | — | 33 | |
| Output Rise/Fall Time | $t_{TLH}$ $t_{THL}$ | 2.0 | | — | — | 75 | — | 95 | ns |
| | | 4.5 | | — | 5 | 15 | — | 19 | |
| | | 6.0 | | — | — | 13 | — | 16 | |
| Input Capacitance | $C_{in}$ | — | | — | 5 | 10 | — | 10 | pF |