SONET/SDH/ATM OC-12 TRANSMITTER AND RECEIVER S3017/S3018

FEATURES

- Complies with ANSI, Bellcore, and ITU-T specifications
- On-chip high-frequency PLL for clock generation and clock recovery
- Supports 622.08 Mbit/s (OC-12/STM-4)
- Reference frequency of 77.76 MHz
- Interface to both PECL and TTL logic
- 8-bit TTL datapath
- Compact 52 PQFP TEP package
- Diagnostic loopback mode
- Lock detect
- Low jitter PECL interface
- < 2.0 Watt per set typically

APPLICATIONS

- SONET/SDH-based transmission systems
- SONET/SDH modules
- SONET/SDH test equipment
- ATM over SONET/SDH
- Section repeaters
- Add drop multiplexors
- Broad-band cross-connects
- Fiber optic terminators
- Fiber optic test equipment

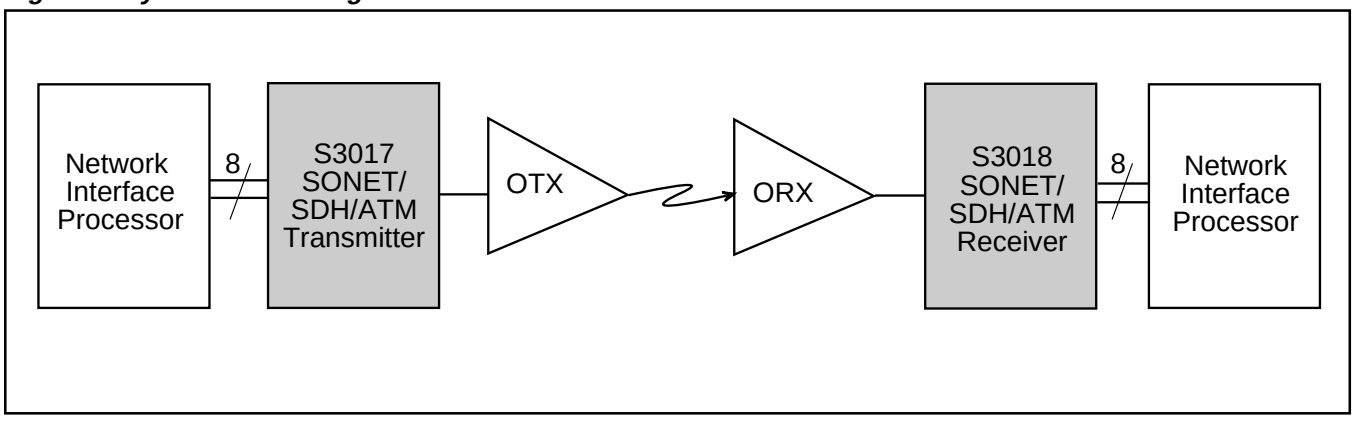
GENERAL DESCRIPTION

The S3017/S3018 SONET/SDH/ATM transmitter and receiver chips are fully integrated serialization/deserialization SONET OC-12 (622.08 Mbit/s) interface devices. With architecture developed by PMC-Sierra, Inc., the chipset performs all necessary serial-to-parallel and parallel-to-serial functions in conformance with SONET/SDH transmission standards. The devices are suitable for SONET-based ATM applications. Figure 1 shows a typical network application.

On-chip clock synthesis is performed by the high-frequency phase-locked loop on the S3017 transmitter chip allowing the use of a slower external transmit clock reference. Clock recovery is performed on the S3018 receiver chip by synchronizing its on-chip VCO directly to the incoming data stream. The S3018 also performs SONET/SDH frame detection. The chipset can be used with a 19.44 or 77.76 MHz reference clock, in support of existing system clocking schemes.

The low jitter PECL interface guarantees compliance with the bit-error rate requirements of the Bellcore, ANSI, and ITU-T standards. The S3017 and S3018 are packaged in a compact 52 PQFP, offering designers a small package outline.

Figure 1. System Block Diagram



SONET OVERVIEW

Synchronous Optical Network (SONET) is a standard for connecting one fiber system to another at the optical level. SONET, together with the Synchronous Digital Hierarchy (SDH) administered by the ITU-T, forms a single international standard for fiber interconnect between telephone networks of different countries. SONET is capable of accommodating a variety of transmission rates and applications.

The SONET standard is a layered protocol with four separate layers defined. These are:

- Photonic
- Section
- Line
- Path

Figure 2 shows the layers and their functions. Each of the layers has overhead bandwidth dedicated to administration and maintenance. The photonic layer simply handles the conversion from electrical to optical and back with no overhead. It is responsible for transmitting the electrical signals in optical form over the physical media. The section layer handles the transport of the framed electrical signals across the optical cable from one end to the next. Key functions of this layer are framing, scrambling, and error monitoring. The line layer is responsible for the reliable transmission of the path layer information stream carrying voice, data, and video signals. Its main functions are synchronization, multiplexing, and reliable transport. The path layer is responsible for the actual transport of services at the appropriate signaling rates.

Data Rates and Signal Hierarchy

Table 1 contains the data rates and signal designations of the SONET hierarchy. The lowest level is the basic SONET signal referred to as the synchronous transport signal level-1 (STS-1). An STS-*N* signal is made up of *N* byte-interleaved STS-1 signals. The optical counterpart of each STS-*N* signal is an optical carrier level-*N* signal (OC-*N*). The S3017/S3018 chipset supports OC-12 rates (622.08 Mbit/s).

Frame and Byte Boundary Detection

The SONET/SDH fundamental frame format for STS-12 consists of 36 transport overhead bytes followed by Synchronous Payload Envelope (SPE) bytes. This pattern of 36 overhead and 1044 SPE bytes is repeated nine times in each frame. Frame and byte boundaries are detected using the A1 and A2 bytes found in the transport overhead. (See Figure 3.)

For more details on SONET operations, refer to the ANSI SONET standard document.

Figure 2. SONET Structure

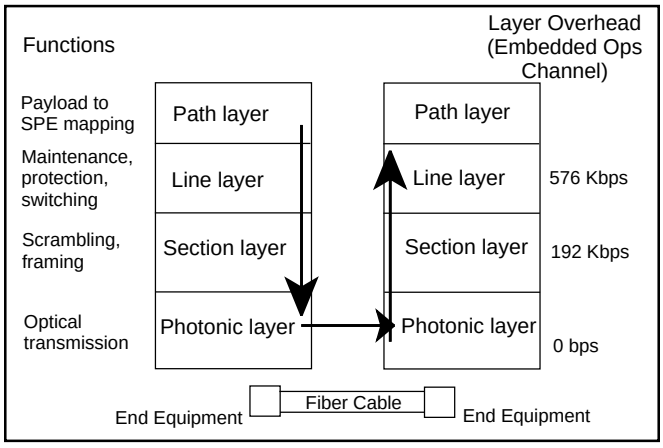
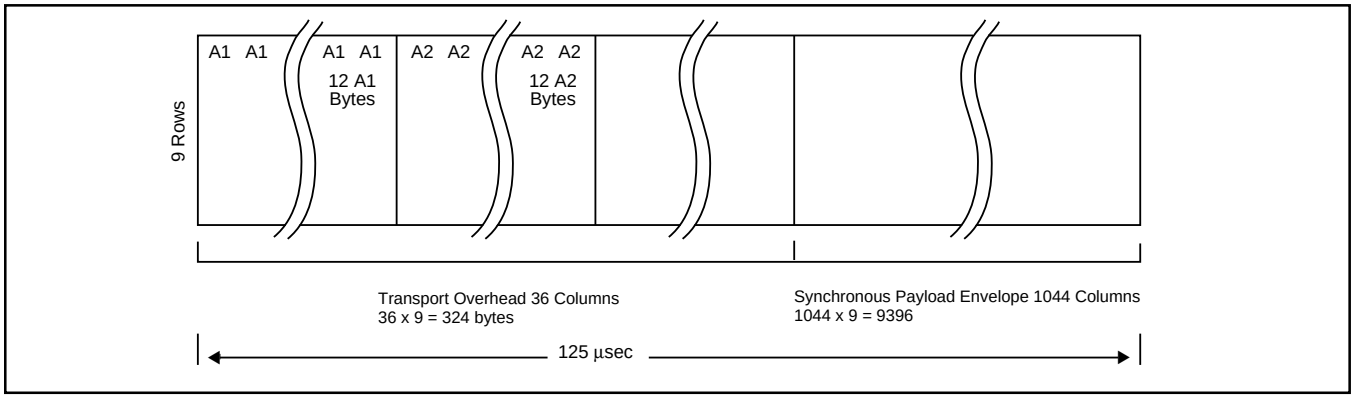


Table 1. SONET Signal Hierarchy

Elec.	ITU-T	Optical	Data Rate (Mbit/s)
STS-1		OC-1	51.84
STS-3	STM-1	OC-3	155.52
STS-12	STM-4	OC-12	622.08
STS-24		OC-24	1244.16
STS-48	STM-16	OC-48	2488.32

Figure 3. STS–12/OC–12 Frame Format



S3017/S3018 OVERVIEW

The S3017 transmitter and S3018 receiver implement SONET/SDH serialization/deserialization, transmission, and frame detection/recovery functions. The block diagrams in Figures 4 and 5 show basic operation of both chips. These chips can be used to implement the front end of SONET equipment, which consists primarily of the serial transmit interface (S3017) and the serial receive interface (S3018). The chipset handles all the functions of these two elements, including parallel-to-serial and serial-to-parallel conversion, clock generation and recovery, and system timing. The system timing circuitry consists of management of the datastream, framing, and clock distribution throughout the front end.

Operation of the S3017/S3018 chips is straightforward. The sequence of operations is as follows:

Transmitter

1. 8-bit parallel input
2. Parallel-to-serial conversion
3. Serial output

Receiver

1. Clock and data recovery from serial input
2. Frame detection
3. Serial-to-parallel conversion
4. 8-bit parallel output

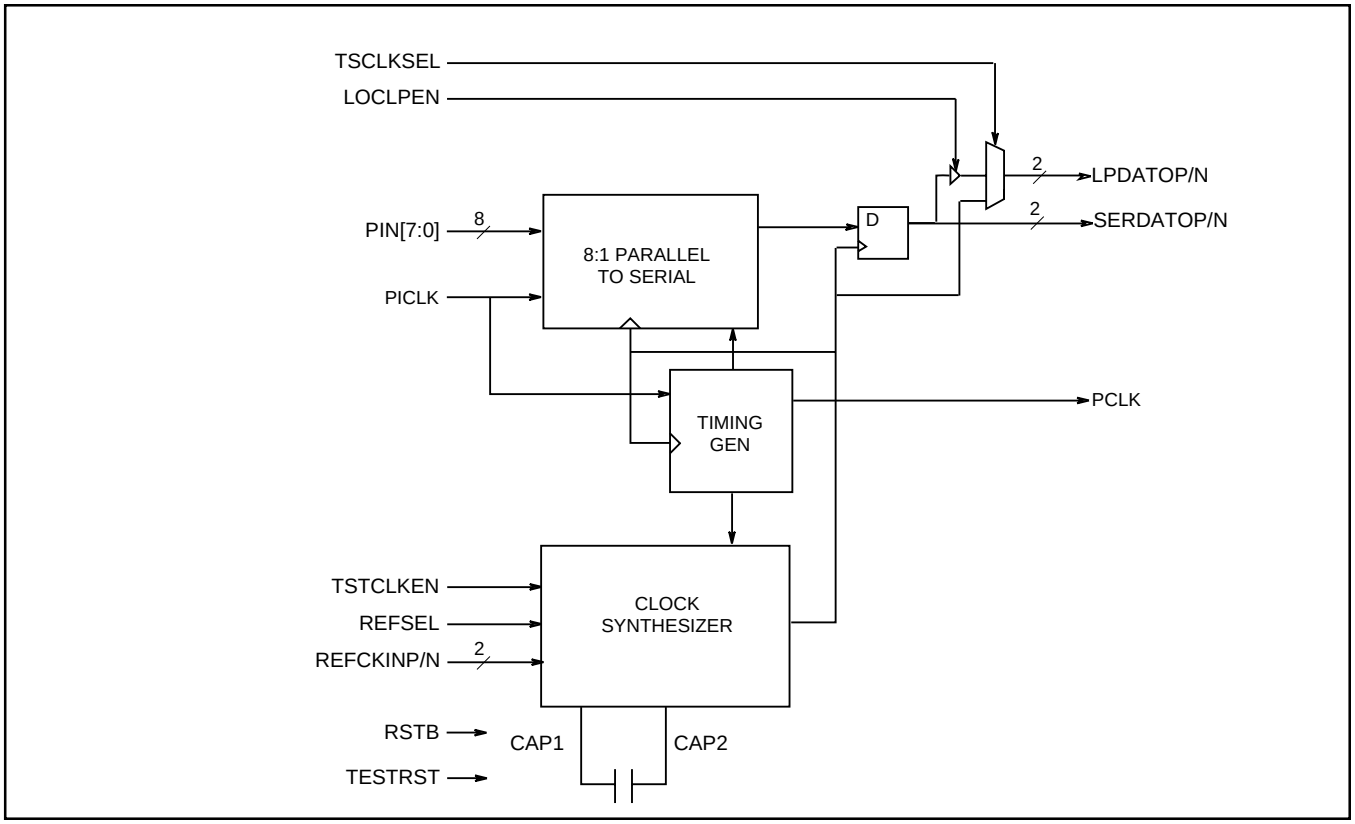
Internal clocking and control functions are transparent to the user. Details of data timing can be seen in Figures 9 through 14.

A lock detect feature is provided on the S3018, which indicates that the PLL is locked (synchronized) to the data stream, and facilitates continuous down-stream clocking in the absence of data.

Suggested Interface Devices

AMCC CONGO (S1201)	POS/ATM SONET Mapper	
AMCC NILE (S1202)	ATM SONET Mapper	
AT&T ASTROTEC1227/1230	650 Mbit/s	Fiber Optic Transmitter
Mitsubishi MF-622DF-T12-XXX	622 Mbit/s	Fiber Optic Transmitter
Sumitomo ES-9304-TD	622 Mbit/s	Fiber Optic Transmitter
AT&T ASTROTEC 1310	650 Mbit/s	Fiber Optic Receiver
Mitsubishi MF-622DS-R1X-XXX	622 Mbit/s	Fiber Optic Receiver
Sumitomo ES-9216-RD	622 Mbit/s	Fiber Optic Receiver
Finisar	1000 Mbit/s	Fiber Optic Transceiver

Figure 4. S3017 Transmitter Functional Block Diagram



S3017 TRANSMITTER FUNCTIONAL DESIGN

The S3017 transmitter chip performs the serializing stage in the processing of a transmit SONET STS-12 bit serial data stream. It converts the byte serial 77.76 Mbyte/sec data stream to bit serial format at 622.08 Mbit/sec.

A high-frequency bit clock can be generated from a 77.76 MHz frequency reference by using an integral frequency synthesizer consisting of a phase-locked loop circuit with a divider in the loop.

Diagnostic loopback is provided (transmitter to receiver) when used with the compatible S3018. (See Other Operating Modes.)

Clock Synthesizer

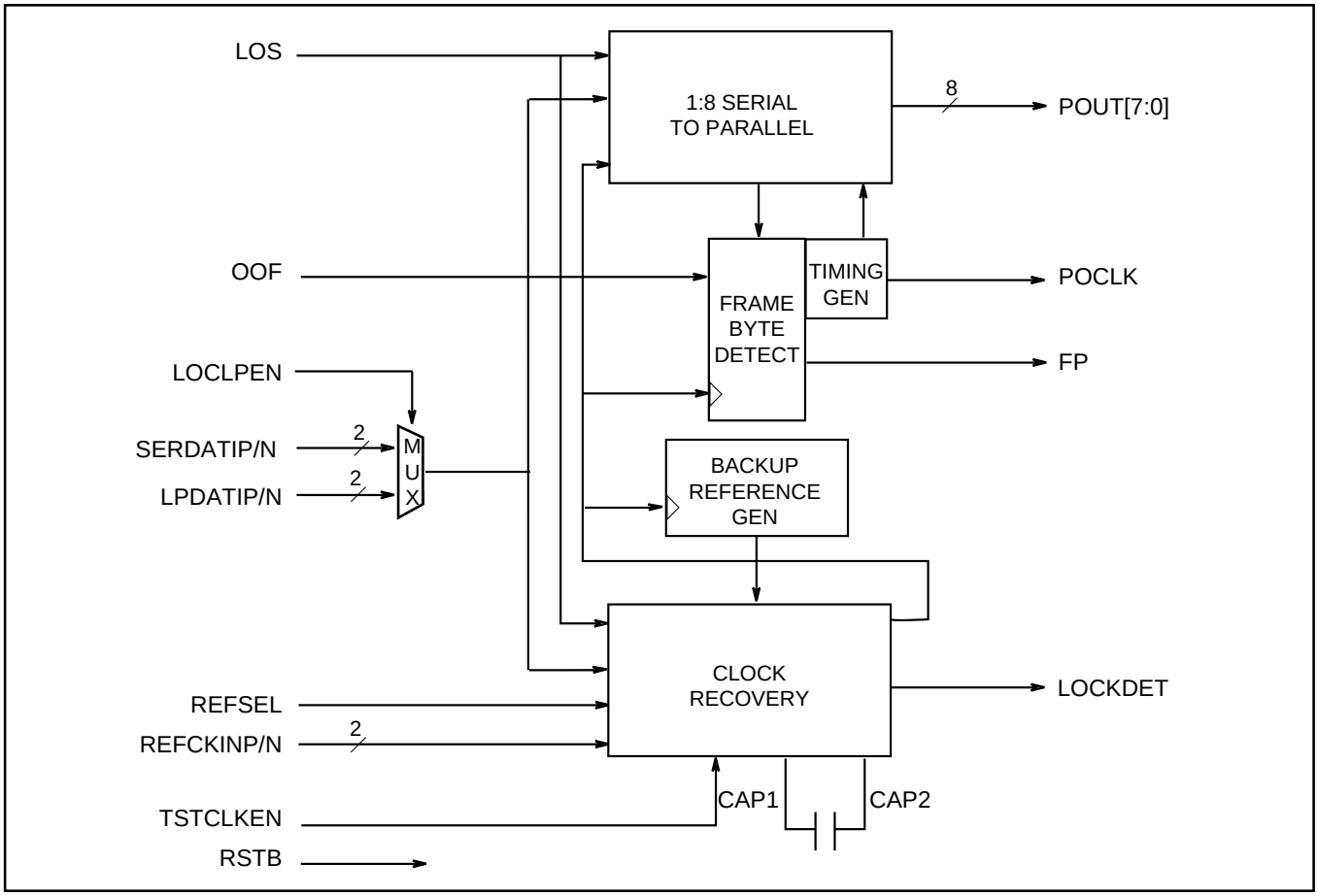
The Clock Synthesizer, shown in the block diagram in Figure 4, is a monolithic PLL that generates the serial output clock phase synchronized with the input reference clock (REFCKINP/N).

The REFCKINP/N input must be generated from a differential PECL crystal oscillator which has a frequency accuracy of better than 20 ppm in order for the TSCLK frequency to have the same accuracy required for operation in a SONET system. Lower accuracy crystal oscillators may be used in applications less demanding than SONET/SDH.

The on-chip PLL consists of a phase detector, which compares the phase relationship between the VCO output and the REFCKINP/N input, a loop filter which converts the phase detector output into a smooth DC voltage, and a VCO, whose frequency is varied by this voltage.

The loop filter generates a VCO control voltage based on the average DC level of the phase discriminator output pulses. A single external clean-up capacitor is utilized as part of the loop filter. The loop filter's corner frequency is optimized to minimize output phase jitter.

Figure 5. S3018 Receiver



Timing Generator

The Timing Generation function, seen in Figure 4, provides a byte rate version of the transmit serial clock. This circuitry also provides an internally generated load signal, which transfers the PIN[7:0] data from the parallel input register to the serial shift register.

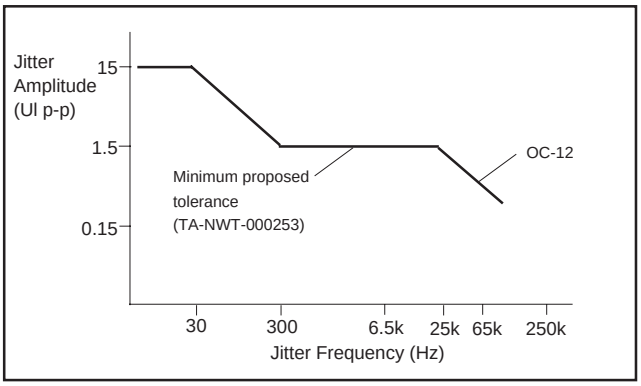
The PCLK output is a byte rate version of transmit serial clock at 77.76 MHz. PCLK is intended for use as a byte speed clock for upstream multiplexing and overhead processing circuits. Using PCLK for upstream circuits will ensure a stable frequency and phase relationship between the data coming into and leaving the S3017 device.

Parallel-to-Serial Converter

The Parallel-to-Serial converter shown in Figure 4 is comprised of two byte-wide registers. The first register latches the data from the PIN[7:0] bus on the rising edge of PICLK. The second register is a parallel loadable shift register which takes its parallel input from the first register.

The load signal, which latches the data from the parallel to the serial shift register, has a fixed relationship to PCLK. If PICLK is tied to PCLK, the PIN[7:0] data latched into the parallel register will meet the timing specifications with respect to the load signal. If PICLK is not tied to PCLK, the delay must meet the timing requirements shown in Figure 9, and PICLK must be frequency locked to the reference clock input.

Figure 6. Clock Recovery Jitter Tolerance



S3018 RECEIVER FUNCTIONAL DESIGN

The S3018 receiver chip provides the first stage of digital processing of a receive SONET STS-12 bit-serial stream. It converts the bit-serial 622.08 Mbit/sec data stream into a 77.76 Mbyte/sec byte-serial data format.

Clock recovery is performed on the incoming scrambled NRZ data stream. A 77.76 MHz reference clock is required for phase locked loop start-up and proper operation under loss of signal conditions. An integral prescaler and phase locked loop circuit is used to multiply this reference to the nominal bit rate.

A loopback mode is provided for diagnostic loopback (transmitter to receiver), when used with the compatible S3017 device.

Clock Recovery

The Clock Recovery PLL, as shown in the block diagram in Figure 5, generates a clock that is at the same frequency as the incoming data bit rate at the SERDATI or LPDATI inputs. The clock is phase aligned by a PLL so that it samples the data in the center of the data eye pattern.

The phase relationship between the edge transitions of the data and those of the generated clock are compared by a phase/frequency discriminator. Output pulses from the discriminator indicate the required direction of phase corrections. These pulses are smoothed by an integral loop filter. The output of the loop filter controls the frequency of the Voltage Controlled Oscillator (VCO), which generates the recovered clock. Frequency stability without incoming data is guaranteed by an alternate reference input (REFCKIN) that the PLL locks onto when data is lost.

The clock recovery circuit monitors the incoming data stream for loss of signal. If the incoming data stream has had no transitions for between 96 and 224 bit times (depending upon the state of an internal counter at the time of last transistion), loss of signal is declared and the PLL will switch from locking onto the incoming data to locking onto the reference clock. Alternatively, the loss-of-signal (LOS) input can be used to force a loss-of-signal condition. When set high, LOS squelches the incoming data stream, and thus causes the PLL to switch its source of reference within 128 bit times. Loss-of-signal condition is removed when LOS is low, and good data, with acceptable pulse density and run length, returns on the incoming data stream.

The loop filter transfer function is optimized to enable the PLL to track the jitter, yet tolerate the minimum transition density expected in a received SONET data signal. This transfer function yields a typical capture time of 16 µs for random incoming NRZ data. A single external clean-up capacitor is utilized as part of the loop filter.

The total loop dynamics of the clock recovery PLL yield a jitter tolerance which meets, with ample margin, the minimum tolerance proposed for SONET equipment by the Bellcore TA-NWT-000253 standard, shown in Figure 6.

Backup Reference Generator

The Backup Reference Generator seen in Figure 5 provides backup reference clock signals to the clock recovery block when the clock recovery block detects a loss of signal condition. It contains a counter that divides the clock output from the clock recovery block down to the same frequency as the reference clock REFCKINP/N.

Frame and Byte Boundary Detection

The Frame and Byte Boundary Detection circuitry searches the incoming data for three consecutive A1 bytes followed immediately by three consecutive A2 bytes. Framing pattern detection is enabled and disabled by the out-of-frame (OOF) input. Detection is enabled by a rising edge on OOF, and remains enabled for the duration that OOF is set high. It is disabled when a framing pattern is detected and OOF is no longer set high. When framing pattern detection is enabled, the framing pattern is used to locate byte and frame boundaries in the incoming data stream (SERDATI or LPDATI). The timing generator block takes the located byte boundary and uses it to block the incoming data stream into bytes for output on the parallel output data bus (POUT[7:0]). The frame boundary is reported on the frame pulse (FP) output when any 48-bit pattern matching the framing pattern is detected on the incoming data stream. When framing pattern detection is disabled, the byte boundary is frozen to the location found when detection was previously enabled. Only framing patterns aligned to the fixed byte boundary are indicated on the FP output.

The probability that random data in an STS-12 stream will generate the 48-bit framing pattern is extremely small. It is highly improbable that a mimic pattern would occur within one frame of data. Therefore, the time to match the first frame pattern and to verify it with down-stream circuitry, at the next occurrence of the pattern, is expected to be less than the required 250 µs, even for extremely high bit error rates.

Once down-stream overhead circuitry has verified that frame and byte synchronization are correct, the OOF input can be set low to disable the frame search process from trying to synchronize to a mimic frame pattern.

Serial to Parallel Converter

The Serial to Parallel Converter consists of three 8-bit registers. The first is a serial-in, parallel-out shift register, which performs serial to parallel conversion clocked by the clock recovery block. The second is an 8-bit internal holding register, which transfers data from the serial to parallel register on byte boundaries as determined by the frame and byte boundary detection block. On the falling edge of the free running POCLK, the data in the holding register is transferred to an output holding register which drives POUT[7:0].

The delay through the Serial to Parallel converter can vary from 1.5 to 2.5 byte periods (12 to 20 serial bit periods) measured from the first bit of an incoming byte to the beginning of the parallel output of that byte. The variation in the delay is dependent on the alignment of the internal parallel load timing, which is synchronized to the data byte boundaries, with respect to the falling edge of POCLK, which is independent of the byte boundaries. The advantage of this serial to parallel converter is that POCLK is neither truncated nor extended during reframe sequences.

OTHER OPERATING MODES

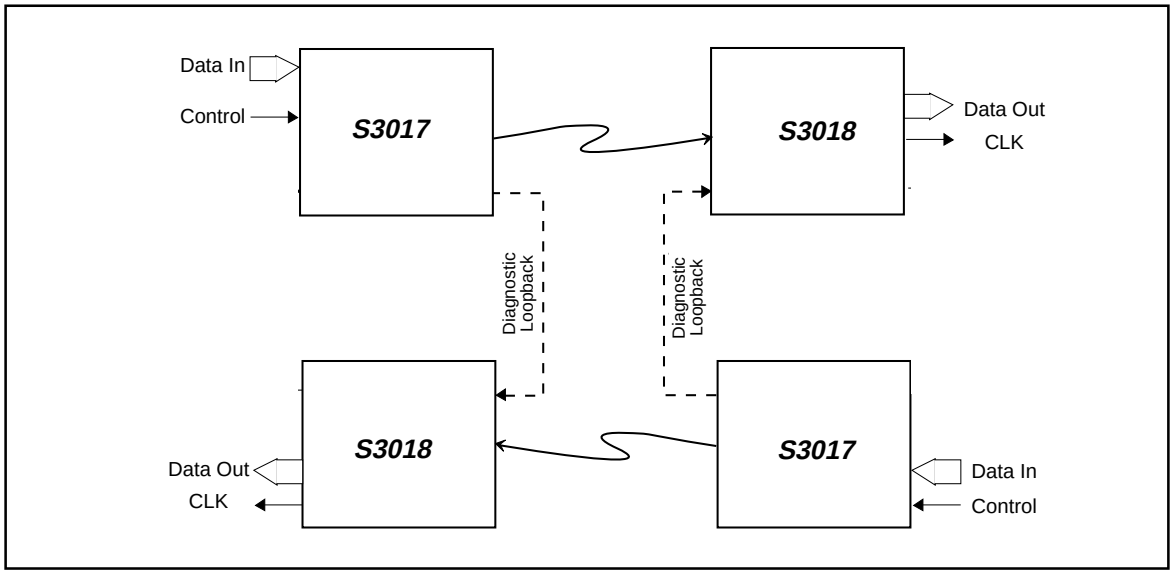
Diagnostic Loopback

The Diagnostic Loopback consists of alternate serial data outputs (in the case of the S3017) and inputs (in the case of the S3018).

On the S3017, the differential PECL output LPDATO provides Diagnostic Loopback serial data. When the Local Loopback Enable (LOCLPEN) input and TSCLKSEL are low, this data output is a replica of SERDATO. When LPDATO is connected to the S3018, a loopback from the transmitter to the receiver at the serial data rate can be set up for diagnostic purposes. When LOCLPEN is high and TSCLKSEL is low, LPDATO is held in the inactive state, with the positive output high and the negative output low. In the inactive state, there will be no interference from the transmitter to the receiver.

On the receiver side, the differential PECL input LPDATI is the Diagnostic Loopback serial data input. When the Local Loopback Enable (LOCLPEN) input is set low, the LPDATI input is routed in place of the normal data stream (SERDATI).

Figure 7. Loopback Diagram



S3017 Pin Assignment and Descriptions

Pin Name	Level	I/O	Pin #	Description
PIN7 PIN6 PIN5 PIN4 PIN3 PIN2 PIN1 PIN0	TTL	I	33 31 30 29 23 22 20 19	Parallel data input, a 77.76 Mbyte/sec word, aligned to the PICLK parallel input clock. PIN7 is the most significant bit (corresponding to the first bit transmitted). PIN0 is the least significant bit (corresponding to the last bit transmitted). PIN(7-0) is sampled on the rising edge of PICLK.
PICLK	TTL	I	12	Parallel input clock, a 77.76 MHz nominally 50% duty cycle input clock, to which PIN(7-0) is aligned. PICLK is used to transfer the data on the PIN inputs into a holding register in the parallel-to-serial converter. The rising edge of PICLK samples PIN(7-0).
TESTCLKEN	TTL	I	4	Test clock enable signal, active high to enable the reference clock to be used in place of the VCO for testing. Allows a means of testing the functions of the chip without the use of the PLL. Set low for normal operation.
REFCKINP REFCKINN	Diff. PECL	I	49 48	Reference clock input used as the reference for the internal bit clock frequency synthesizer.
LOCLPEN	TTL	I	8	Local loopback enables the LPDATO output when low and TSCLKSEL is low. When LOCLPEN is high, the LPDATO output is held in the inactive state to prevent interference between the transmit and receive devices.
RSTB	TTL	I	9	Reset input for the device, active low. During reset, PCLK does not toggle.
TSCLKSEL	TTL	I	35	Active high transmit clock select input which, when enabled, directs the transmit serial clock through the LPDATOP/N output.
TESTRST	TTL	I	11	Test reset, used to reset portions of the clock recovery PLL during production testing. Held low for normal operation.
REFSEL	TTL	I	7	Reference select, used to select the reference clock frequency. Set low to select 77.76 MHz. Set high to select 19.44 MHz for applications less demanding than SONET/SDH.
CAP1 CAP2	–	I	1 52	The loop filter capacitor is connected to these pins. The capacitor value should be 0.01µf ±10% tolerance, X7R dielectric. 50 V is recommended (16 V is acceptable).
SERDATOP SERDATON	Diff. PECL	O	47 45	High-speed, source-terminated differential PECL. Serial output data stream signals, normally connected to an optical transmitter module.

S3017 Pin Assignment and Descriptions (Continued)

Pin Name	Level	I/O	Pin #	Description
LPDATOP LPDATON	Diff. PECL	O	44 43	Loopback serial data stream signals, normally connected to a companion S3018 device for diagnostic loopback purposes. They are held inactive when LOCLPEN is high and TSCLKSEL is low. The serial data stream is output when LOCLPEN is low and TSCLKSEL is low. When enabled by the TSCLKSEL input, the transmit serial clock will be output through this pin. The transmit serial clock is a buffered version of the internal frequency synthesizer clock, which is phase-aligned with the SERDATO output signal. The SERDATO is updated on the falling edge of the transmit serial clock.
PCLK	TTL	O	16	Parallel reference clock generated by dividing the internal bit clock by eight. It is normally used to coordinate byte-wide transfers between upstream logic and the S3017 device.
AVEE	0V	–	2, 39, 41, 42, 51	Analog 0V
AVCC	+5V	–	3, 38, 40, 46, 50	Analog +5V
ECLVCC	+5V	–	5, 15, 25, 28, 37	Digital +5V
ECLVEE	0V	–	6, 10, 18, 21, 32, 36	Digital 0V
TTLGND	0V	–	13, 17, 27	Digital 0V
TTLVCC	+5V	–	14, 24, 26	Digital +5V
NC	–	–	34	No Connection

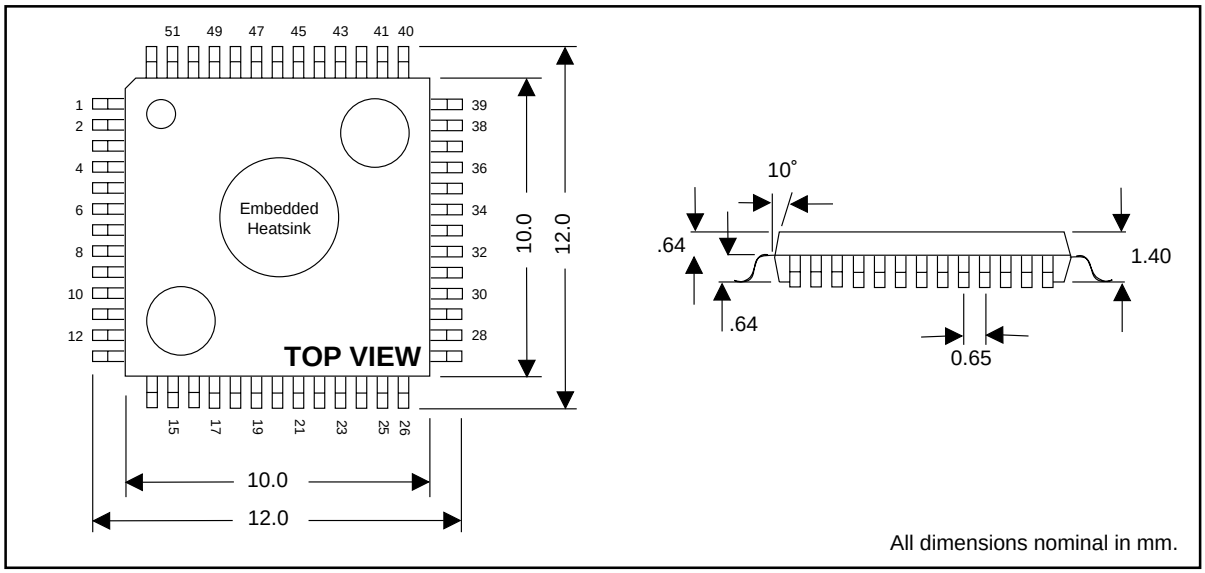
S3018 Pin Assignment and Descriptions

Pin Name	Level	I/O	Pin #	Description
SERDATIP SERDATIN	Diff. PECL	I	45 46	Serial data stream signals normally connected to an optical receiver module. A clock is recovered from transitions on the SERDATI inputs.
LPDATIP LPDATIN	Diff. PECL	I	42 44	Serial data stream signal, normally connected to a companion S3017 device for diagnostic loopback purposes. Clock is recovered from transitions on the LPDATI inputs while in diagnostic loopback.
LOCLPEN	TTL	I	8	Selects diagnostic loopback. When LOCLPEN is high, the S3018 device uses the primary data (SERDATI) input. When low, the S3018 device uses the diagnostic loopback data (LPDATI) input.
TSTCLKEN	TTL	I	4	Test clock enable signal, set high to enable the reference clock to be used in place of the VCO for testing. Allows a means of testing the functions of the chip without the use of the PLL. Set low for normal operation.
OOF	TTL	I	31	Out of frame indicator used to enable framing pattern detection logic in the S3018. This logic is enabled by a rising edge on OOF, and remains enabled until frame boundary is detected or when OOF is set low, whichever is longer. OOF is an asynchronous signal with a minimum pulse width of one POCLK period. (See Figures 13 and 14.)
LOS	PECL	I	34	An active-high, single-ended 10K ECL input to be driven by the external optical receiver module to indicate a loss of received optical power. When LOS is high, the data on the Serial Data In (SERDATIP/N) pins will be internally forced to a constant zero, LOCKDET will be forced low, and the PLL will lock to the REFCKINP/N inputs. This signal must be used to assure correct automatic reacquisition to serial data following an interruption and subsequent reconnection of the optical path. (This ensures that the PLL does not "wander" out of reacquisition range by tracking the random phase/frequency content of the optical detector's noise floor while monitoring "dark" fiber.) When LOS is low, data on the SERDATIP/N pins will be processed normally.
REFCKINP REFCKINN	Diff. PECL	I	49 48	Input normally used as the reference for the integral clock recovery PLL.
RSTB	TTL	I	33	Master reset input for the device, active low. Initializes the device to a known state and forces the PLL to acquire to the reference clock. A reset of at least 16 ms should be applied at power-up and whenever the user wishes to force the PLL to re-acquire to the reference clock. The S3018 will also re-acquire to the reference clock if the serial data input is held quiescent for at least 16 ms.

S3018 Pin Assignment and Descriptions (Continued)

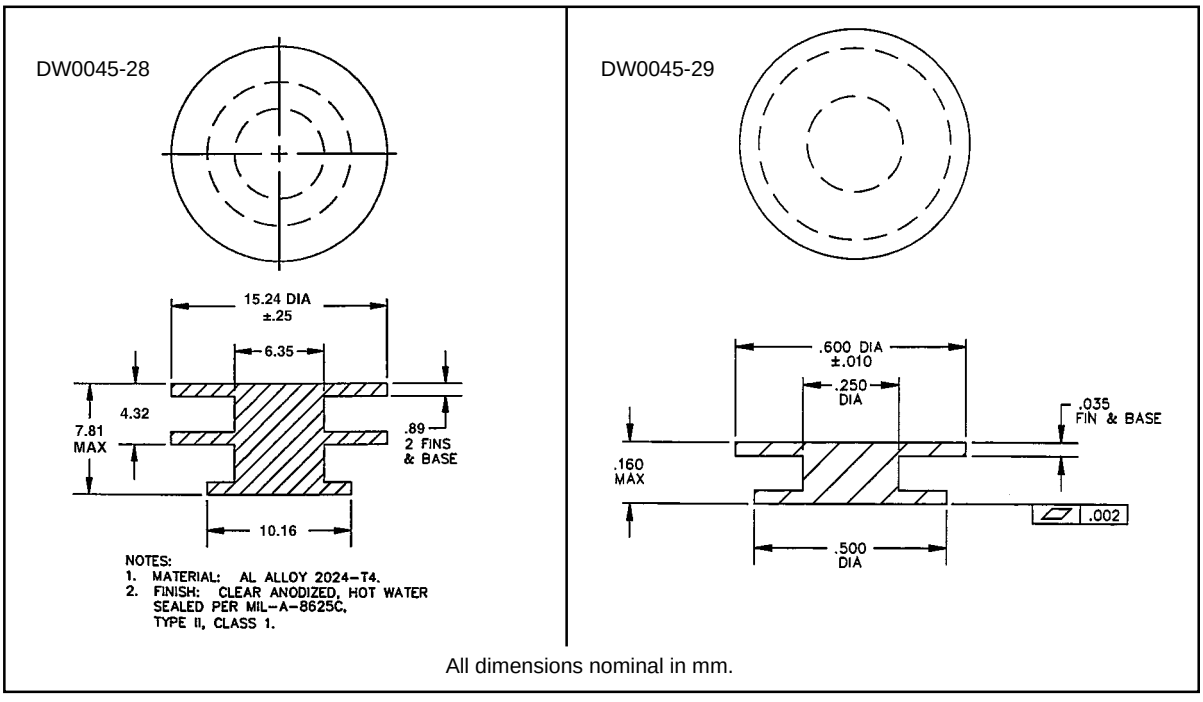
Pin Name	Level	I/O	Pin #	Description
REFSEL	TTL	I	7	Reference select used to select the reference clock frequency. Set low to select 77.76 MHz. Set high to select 19.44 MHz for applications less demanding than SONET/SDH.
CAP1 CAP2	–	I	1 52	The loop filter capacitor is connected to these pins. The capacitor value should be 0.1µf ±10% tolerance, X7'R dielectric. 50V is recommended (16V is acceptable).
POUT7 POUT6 POUT5 POUT4 POUT3 POUT2 POUT1 POUT0	TTL	O	30 29 23 22 20 19 16 12	Parallel data bus, a 77.76 Mbyte/sec word, aligned to the POCLK parallel output clock. POUT7 is the most significant bit (corresponding to bit 1 of each PCM word, the first bit received). POUT0 is the least significant bit (corresponding to bit 8 of each PCM word, the last bit received). POUT(7-0) is updated on the falling edge of POCLK.
FP	TTL	O	11	Frame pulse. Indicates frame boundaries in the incoming data stream (SERDATI). If framing pattern detection is enabled, as controlled by the OOF input, FP pulses high for one POCLK cycle when a 48-bit sequence matching the framing pattern is detected on the serial data inputs. When framing pattern detection is disabled, FP pulses high when the incoming data stream, after byte alignment, matches the framing pattern. FP is updated on the falling edge of POCLK.
POCLK	TTL	O	9	Parallel output clock, a 77.76 MHz nominally 50% duty cycle, byte rate output clock, that is aligned to POUT(7-0) byte serial output data. POUT(7-0) and FP are updated on the falling edge of POCLK.
LOCKDET	TTL	O	35	Clock recovery indicator. Set high when the internal clock recovery has locked onto the incoming data stream. LOCKDET is an asynchronous output.
AVEE	0V	–	2, 39, 41, 43	Analog 0V
AVCC	+5V	–	3, 38, 40, 47	Analog +5V
ECLVCC	+5V	–	5, 15, 25, 28, 37, 50	Digital +5V
ECLVEE	0V	–	6, 10, 18, 21, 32, 36	Digital 0V
TTLGND	0V	–	13, 17, 27	Digital 0V
TTLVCC	+5V	–	14, 24, 26	Digital +5V
NC	–	–	51	No Connection

Figure 8. 52 PQFP Package



All dimensions nominal in mm.

Heatsinks DW0045-28 and DW0045-29



All dimensions nominal in mm.

Performance Specifications

Parameter	Min	Typ	Max	Units	Condition
Nominal VCO Center Frequency		622.08		MHz	
PECL Data Output Jitter OC-12/STS-12			16	ps (rms)	In CSU mode, given 14 ps rms jitter on REFCKIN in 12KHz to 5 MHz band
Reference Clock Frequency Tolerance Clock Synthesis Clock Recovery	 -20 -100		 +20 +100	 ppm ppm	Required to meet SONET output frequency specification
OC-12/STS-12 Capture Range Lock Range		 ±200ppm +2,-8%			 With respect to fixed reference frequency Minimum transition density of 20%
Acquisition Lock Time			16	µsec	With device already powered up and valid reference clock
Reference Clock Input Duty Cycle	30		70	% of period	
Reference Clock Rise & Fall Times			2.0	ns	10% to 90% of amplitude
PECL Output Rise & Fall Times (S3017 LPDATOP/N)			600	ps	20% to 80%, 50 Ω to Vcc -2V equivalent load, 5pF cap
Source Terminated Diff. PECL Compatible Output Rise & Fall Times (S3017 SERDATOP/N)			450	ps	20% to 80%, 100 Ω line to line

Absolute Maximum Ratings

Parameter	Min	Typ	Max	Units
Case Temperature Under Bias	–55		125	˚C
Junction Temperature Under Bias	–55		150	˚C
Storage Temperature	–65		150	˚C
Voltage on V_{CC} with Respect to Ground	–0.5		+7.0	V
Voltage on Any TTL Input Pin	–0.5		+5.5	V
Voltage on Any PECL Input Pin	V_{CC}–3		V_{CC}	V
TTL Output Sink Current			20	mA
TTL Output Source Current			10	mA
High Speed PECL Output Source Current			50	mA

ESD Ratings

The S3017/S3018 are rated to the following ESD voltages based on the human body model:

1. All pins are rated at or above 1000 V.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Ambient Temperature Under Bias	–40		185	˚C
Junction Temperature Under Bias	–10		+125	˚C
Voltage on V_{CC} with Respect to Ground	4.75	5.0	5.25	V
Voltage on Any TTL Input Pin	0		V_{CC}	V
Voltage on Any PECL Input Pin	V_{CC}–2		V_{CC}	V
S3017 ICC		178	238	mA
S3018 ICC		216	260	mA

TTL Input/Output DC Characteristics

(T_A = -40°C to +85°C, V_{CC} = 5 V ±5%)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
V_{IL}[1]	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage
V_{IH}[1]	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage
I_{IL}	Input LOW Current	-400.0			µA	V_{CC} = MAX, V_{IN} = 0.5V
I_{IH}	Input HIGH Current			50.0	µA	V_{CC} = MAX, V_{IN} = 2.7V
I_I	Input HIGH current at Max. VCC			1.0	mA	V_{CC} = MAX, V_{IN} = 5.5V
I_{OS}	Output Short Circuit Current	-100.0		-25.0	mA	V_{CC} = MAX, V_{OUT} = 0.5V
V_{IK}	Input Clamp Diode Voltage	-1.2			Volts	V_{CC} = MIN, I_{IN} = -18 ma
V_{OL}	Output LOW Voltage			0.5	Volts	V_{CC} = MIN, I_{OL} = 8 ma
V_{OH}	Output HIGH Voltage	2.7			Volts	V_{CC} = MIN, I_{OH} = -1 ma

1. These input levels provide zero noise immunity and should only be tested in a static, noise-free environment.

Thermal Management

Device	Power	Theta-ja Still Air w/ DW0045-28 Heatsink	Max Still Air[1] w/ DW0045-28 Heatsink	Required Air[2] w/ DW0045-29 Heatsink
S3017	1.25W	32.7˚C/W	89˚C	100 LFPM
S3018	1.36W	32.7˚C/W	85˚C	100 LFPM

Notes:

1. Max ambient temperature permitted in still air to maintain Tj <130˚C.
2. Airflow required in 85˚C ambient conditions to maintain Tj <130˚C.

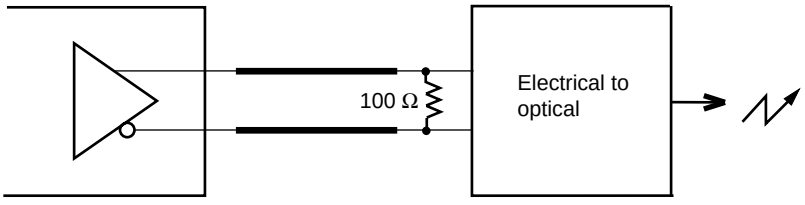
PECL Input/Output DC Characteristics[1,2]

(T_A = -40°C to +85°C, V_{CC} = 5 V ±5%)

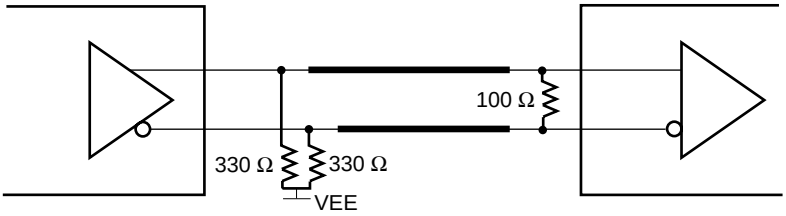
Symbol	Parameter	Min	Typ	Max	Unit	Conditions
V_{IL}	Input LOW Voltage	V_{CC} -2.000		V_{CC} -1.441	Volts	Guaranteed Input LOW Voltage for single-ended inputs
V_{IH}	Input HIGH Voltage	V_{CC} -1.225		V_{CC} -0.570	Volts	Guaranteed Input HIGH Voltage for single-ended inputs
V_{IL}	Input LOW Voltage	V_{CC} -2.000		V_{CC} -0.700	Volts	Guaranteed Input LOW Voltage for differential inputs
V_{IH}	Input HIGH Voltage	V_{CC} -1.750		V_{CC} -0.450	Volts	Guaranteed Input HIGH Voltage for differential inputs
V_{ID}	Input Diff. Voltage	0.250	0.500	1.400	Volts	Differential Input Voltage
I_{IH}	Input High Current	-0.500		20.000	µA	V_{ID} = 500mV
I_{IL}	Input Low Current	-0.500		20.000	µA	V_{ID} = 500mV
V_{OL}	Output LOW Voltage	V_{CC} -2.000		V_{CC} -1.500	Volts	50 ohm termination to V_{CC} -2V
V_{OH}	Output HIGH Voltage	V_{CC} -1.110		V_{CC} -0.670	Volts	50 ohm termination to V_{CC} -2V
V_{OD}	Output Diff. Voltage	0.390		1.330	Volts	Differential Output Voltage

1. These conditions will be met with no airflow.
2. When not used, tie the positive differential PECL pin to V_{CC} and the negative differential ECL pin to ground via a 3.9K resistor.

Differential ECL Input and Output Applications



S3017 SERDATOP/N to Fiber Optic Transmitter

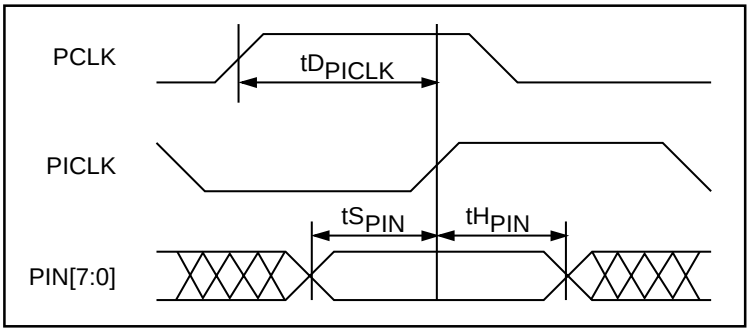


Reference Clock Crystal Oscillator Source (ECL Driver) to REFCKINP/N Inputs.
S3017 LPDATOP/N to S3018 LPDATIP/N.
Fiber Optic Receiver to S3018 SERDATIP/N.

Table 2. S3017 AC Timing Characteristics **(T_A = -40°C to +85°C, V_{CC} = 5 V ±5%)**

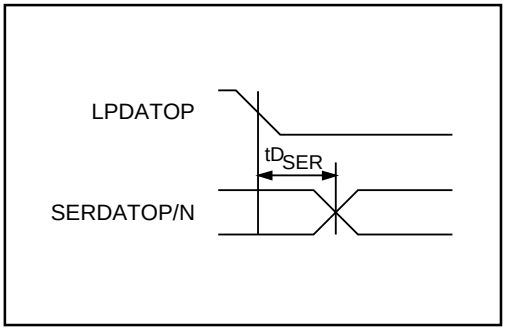
Symbol	Description	Min	Typ	Max	Units
tD_{PICLK}	PICLK Delay from PCLK	0		5.5	ns
tS_{PIN}	PIN [7:0] Set-up Time w.r.t. PICLK	1.5			ns
tH_{PIN}	PIN [7:0] Hold Time w.r.t. PICLK	1			ns
tD_{SER}	Serial Clock (LPDATOP) Low to SERDATOP/N Valid Prop Delay	0		500	ps
	Serial Clock (LPDATOP) Duty Cycle	40		60	%
tD_{RP}	REFCKINP High to PCLK High Valid Prop Delay	7.0		11.0	ns

Figure 9. PIN AC Input Timing



Notes on TTL Output Timing:
1. When a set-up time is specified on TTL signals between an input and a clock, the set-up time is the time in nanoseconds from the 50% point of the input to the 50% point of the clock.
2. When a hold time is specified on TTL signals between an input and a clock, the hold time is the time in nanoseconds from the 50% point of the clock to the 50% point of the input.

Figure 10a. Clock and Data Output Timing with TSCLKSEL Asserted



Notes on PECL Output Timing:
1. Output propagation delay time of high speed PECL outputs is the time in nanoseconds from the cross-over point of the reference signal to the cross-over point of the output.

Figure 10b. REFCKIP High to PCLK High Valid Prop Delay

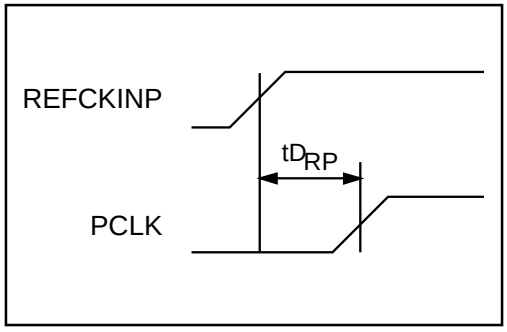
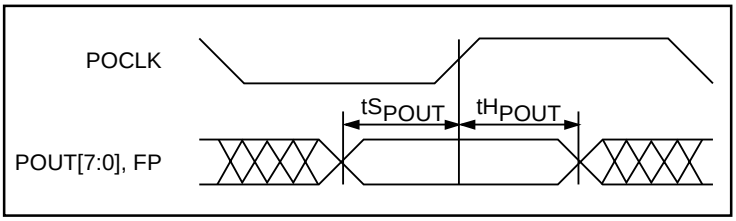


Table 3. S3018 AC Timing Characteristics **(T_A = -40°C to +85°C, V_{CC} = 5 V ±5%)**

Symbol	Description	Min	Typ	Max	Units
	POCLK Duty Cycle	40		60	%
tS_{POUT}	POUT[7:0] and FP Set-up Time w.r.t. POCLK	4			ns
tH_{POUT}	POUT[7:0] and FP Hold Time w.r.t. POCLK	2			ns
	SERDATIP/N Minimum Pulse Width	400			ps

Figure 11. Output Timing Diagram



Notes on TTL Output Timing:
1. Output propagation delay time of TTL outputs is the time in nanoseconds from the 50% point of the reference signal to the 30% or 70% point of the output.
2. Maximum output propagation delays and duty cycles of TTL outputs are measured with a 15 pF load and 500 ohms to ground on the outputs.

RECEIVER FRAMING

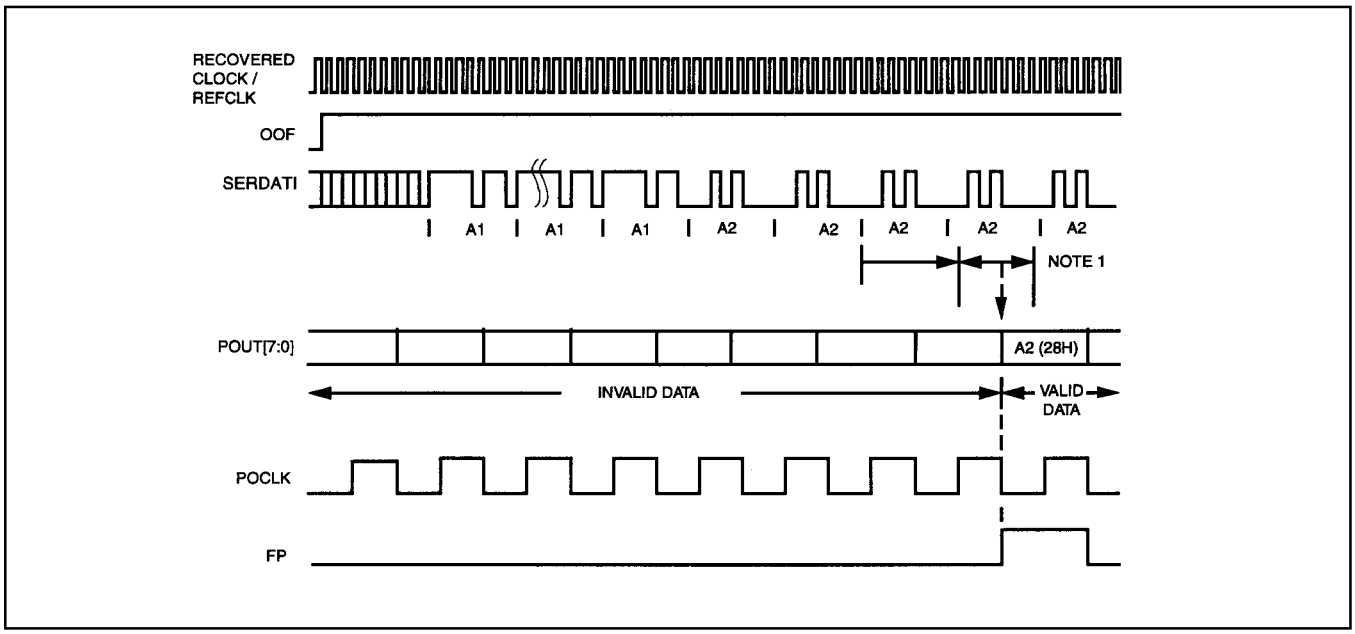
Figure 12 shows a typical reframe sequence in which a byte realignment is made. The frame and byte boundary detection is enabled by the rising edge of OOF and remains enabled while OOF is high. Realignment occurs upon receipt of the first A1 byte. The frame boundary is recognized upon receipt of the third A2 byte, which is the first data byte to be reported with the correct byte alignment on the outgoing data bus (POUT[7:0]). Concurrently, the frame pulse is set high for one POCLK cycle.

When interfacing with a section terminating device, the OOF input remains high for one full frame after the first frame pulse while the section terminating device verifies internally that the frame and byte alignment are correct, as shown in Figure 13. Since at least one framing pattern has been detected since the rising edge of OOF, boundary detection is disabled when OOF is set low.

The frame and byte boundary detection block is activated by the rising edge of OOF, and stays active until the first FP pulse or until OOF goes low, whichever occurs last. Figure 13 shows a typical OOF timing pattern which occurs when the S3018 is connected to a down stream section terminating device. OOF remains high for one full frame after the first FP pulse. The frame and byte boundary detection block is active until OOF goes low.

Figure 14 shows the frame and byte boundary detection activation by a rising edge of OOF, and deactivated by the first FP pulse.

Figure 12. Frame and Byte Detection



NOTE 1: Range of input to output delay can be 1.5 to 2.5 POCLK cycles

Figure 13. OOF Operation Timing with PM5312 STTX or PM5355 SUNI-622

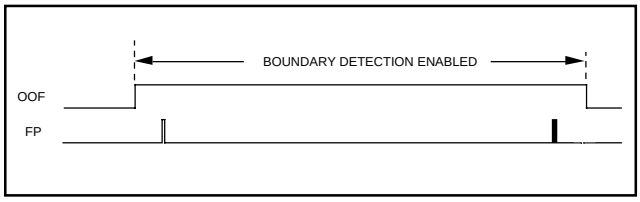
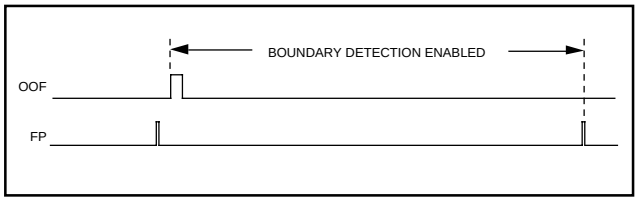


Figure 14. Alternate OOF Timing



S3017 WITH DATA CLOCK SYNCHRONOUS TO REFERENCE CLOCK

INTRODUCTION

In some applications it is necessary to “forward clock” the data in a SONET/SDH system. In this application the reference clock from which the high speed serial clock is synthesized and the parallel data clock both originate from the same (usually TTL/CMOS) clock source. This application note explains how the AMCC S3017 can be configured to operate in this mode.

Clock Control Logic Description

The timing control logic in the S3017 automatically generates an internal load signal which has a fixed relationship to the reference clock. The logic takes into account the variation of the reference clock to the internal load signal over temperature and voltage.

The connections required to implement the design are shown in Figure 15, and the timing specifications are shown in Figure 16. The setup and hold times for the PICLK to the data must be met by the controller ASIC. We recommend latching the data on the falling edge of the output reference clock in order to meet the required specifications.

Possible Problems

In order to meet the jitter generation specifications required by SONET, the jitter of the reference clock must be minimized. It may be difficult to meet the SONET jitter generation specifications using a reference clock input with a TTL reference source.

Figure 15. S3017 with Data Clocked by Reference Clock

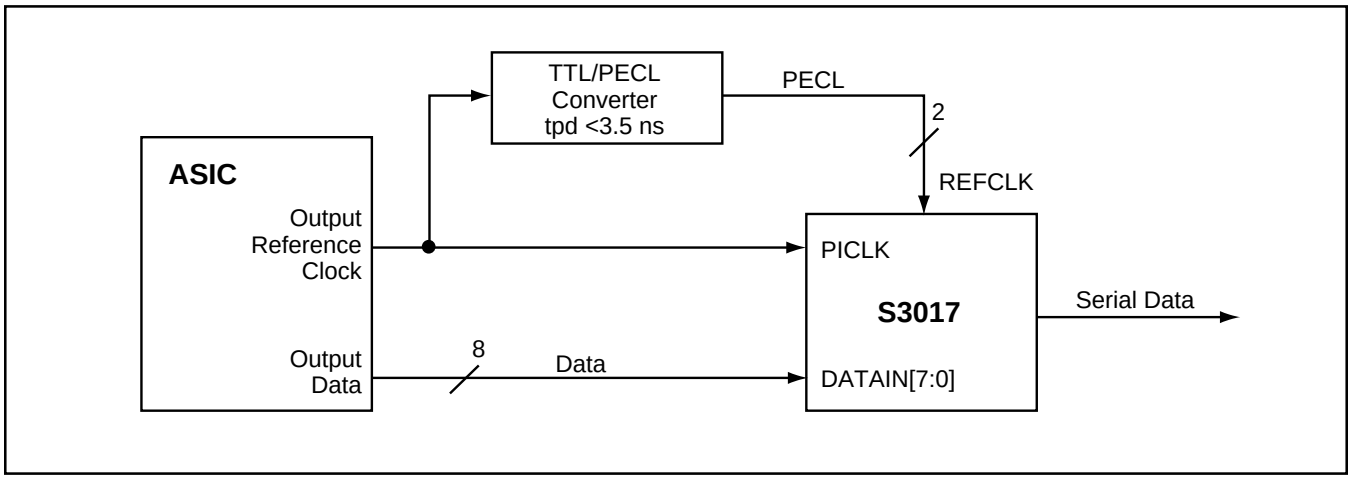


Figure 16. Data Timing with Respect to PICLK

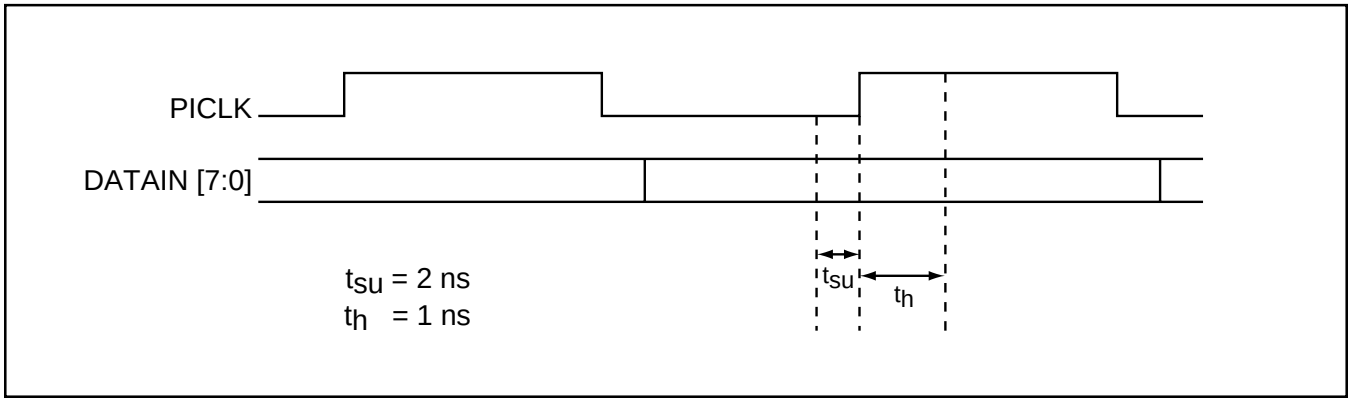
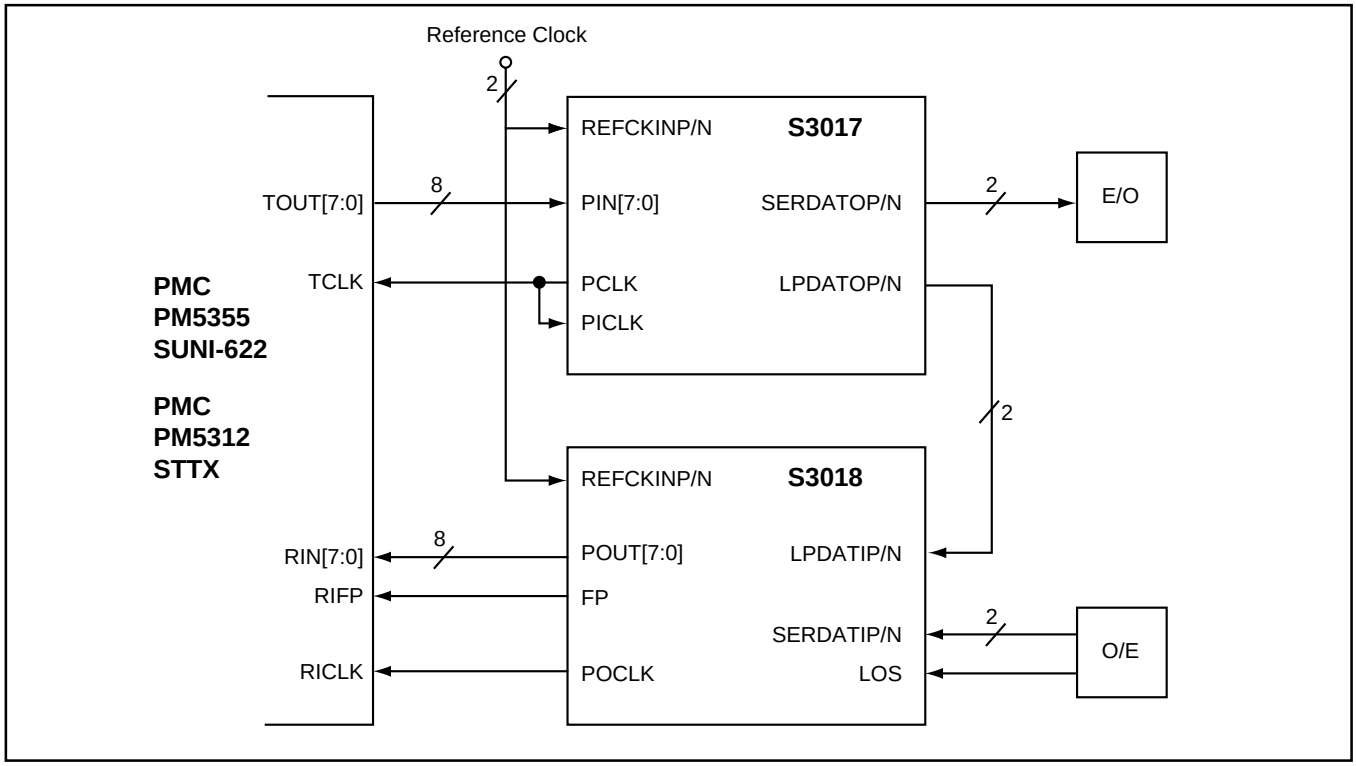


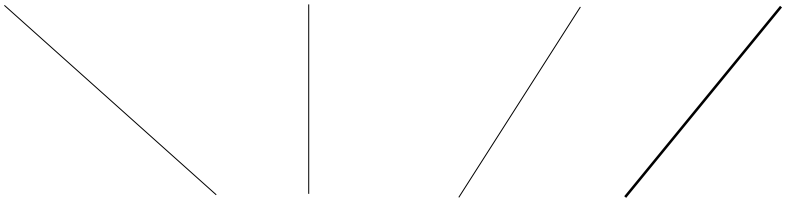
Figure 17. System Block Diagram



Ordering Information

PREFIX	DEVICE	PACKAGE	HEATSINK
S – Integrated Circuit	3017	A – 52 PQFP TEP	H1 – w/DW0045-28 heatsink unattached H2 – w/DW0045-29 heatsink unattached

PREFIX	DEVICE	PACKAGE	HEATSINK
S – Integrated Circuit	3018	A – 52 PQFP TEP	H1 – w/DW0045-28 heatsink unattached H2 – w/DW0045-29 heatsink unattached



X XXXX X / XX

Prefix Device Package Heatsink (Heatsink identifier not marked on part)

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http://www.amcc.com