HD81504FE

ISDN I-Interface LSI

HD81504FE is a full-duplex transceiver for an ISDN basic rate user-network interface specified by ITU-T I Series Recommendations.

This LSI contains layer 1 and HDLC functions following I.430 and I.441 at S/T reference point, and also includes 8-bit CPU, Timer, MMU and Upper layer CPU interface. Upper Layser CPU interface is selectable data transfer mode (DMA/Programmed I/O), for direct connection to 3-type of microprocesser.

Moreover, this LSI includes the following functions; (1) Driver/Receiver circuit for line interface. (2) Internal CPU improved with high operational frequency (Max 12.288 MHz). (3) Master/Slave operation mode for various kind of Terminal equipment (TE) and Network termination (NT).

Features

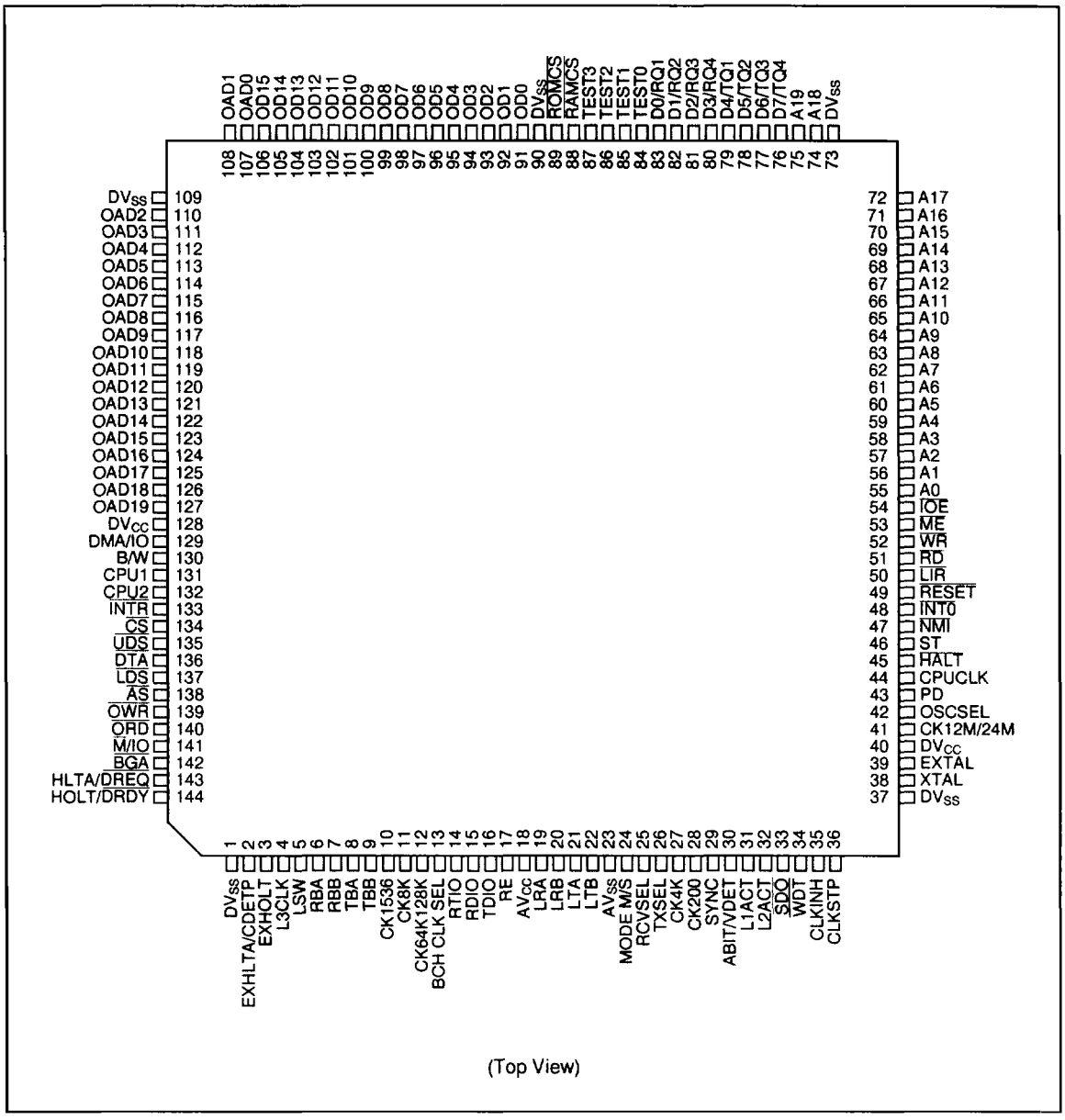
- Layer 1 control following ITU-T recommendation I.430
  - 192 kb/s transmission rate
  - 2B + D channel structure
  - Driver/Receiver circuit provided
  - Synchronization control (Timing recover, frame alignment)
  - D-channel collision control by E-bit with retransmission function
  - Multiframing control by Q-bit
  - E-bit output function
  - Master/Slave mode operation
  - Selectable B-channel use
    Individual use of B1 and B2 (64 kb/s)
    Bulk use of B1 + B2 (128 kb/s)
  - B channel data Input/Output clock selectable (Internal or external clock)
  - Incoming signal detect function
- HDLC function following ITU-T recommendation I.441
  - HDLC frame control (Flag control, FCS Addition/Check, 0 Insertion/Deletion)
- Upper CPU interface function
  - Direct connection to 3 type of microprocessor bus: 8086 type, 68000 type, H8 type
  - Selectable data transfer mode: DMA/Programmed I/O
  - Selectable data transfer width
- Built-in 8-bit microprocessor (64180 Core: Max 12.288 MHz)
  - Protcol processing for over Layer 2
  - MMU: 1-MB address space
  - Two timers
  - Watchdog timer (W.D.T)

- B channel select function
  - — Selectable Input/Output pins for B1 and B2 channel
- Loopback test function
- Individual operation modes of layer 1 and layer 2 function
- Power down mode for low power operation
- Oscillation circuit provided
- 0.8 μm CMOS technology
- TTL/CMOS compatible Input/Output
- Single power supply 5 V ± 5%
- 144 pin quad flat package

Main Operation Mode

- Operation layer selectable
  - — All layer operation
  - — Layer 1 individual operation
  - — Layer 2 individual operation
- Master/Slave mode selectable
- Receive timing selectable at master mode
  - — Transmit synchronized mode for short passive bus
  - — Receive synchronized mode for point to point bus and extended bus
- B channel data Input/Output clock selectable (8 kHz, 64 kHz/128 kHz)
  - — Internal Clock Mode
  - — External Clock Mode
- B-channel use selectable
  - — Normal use; B1 and B2 (64 kb/s) 2 channel
  - — Bulk use; B1 + B2 (128 kb/s) 1 channel
- Collision control function
  - — Normal mode; The collision detection function operates only on the address field.
  - — ID mode; The collision detection function operates on the address to information fields.
- B-channel select function
  - — Normal mode; Receive B1 and B2 channel data on RBA and RBB, respectively; Transmit B1 and B2 channel data on TBA TBB, respectively;
  - — Reverse mode; Receive B2 and B1 channel data on RBA and RBB, respectively; Transmit B2 and B1 channel data on TBA TBB, respectively;
- Loopback mode
  - — D-channel Local/Remote loop
  - — B-channel Local/Remote loop
- Upper CPU interface bus selectable
  - — 8086 type
  - — 68000 type
  - — H8 type
- Data transfer mode selectable
  - — Programmed I/O transfer mode
  - — DMA transfer mode
- Data transfer width selectable at DMA
  - — 8 bit data transfer width
  - — 16 bit data transfer width
- Low power dissipation mode selectable
  - — Normal mode: Internal CPU operation clock 12.288 MHz/6.144 MHz
  - — Power down mode: Internal CPU operation clock 6.144 MHz/3.072 MHz
  - — Clock stop mode: All function disabled expect incoming detector

Pin Arrangement

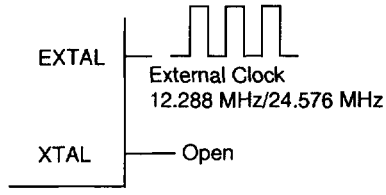


(Top View)

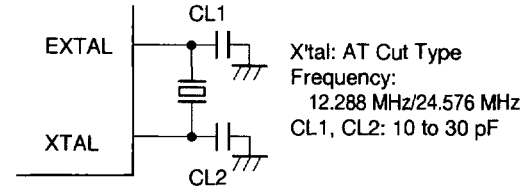
Pin Descriptions

Common Part

Pin No.	Symbol	I/O	Function
40, 90, 128	DV_{CC}	I	Digital power supply: 5 V ± 5%
1, 37, 73, 109	DV_{SS}	I	Digital ground
18	AV_{CC}	I	Analog power supply: 5 V ± 5%
23	AV_{SS}	I	Analog ground
38	XTAL	O	Oscillator output: X'tal connect
39	EXTAL	I	Oscillator input: X'tal connect or External Clock Input



(A) External Input Mode



(B) X'tal Mode

44	CPU CLK	O	System clock: Internal CPU system clock output
41	CK12M/24M	O	12 MHz/24 MHz clock output:
42	OSC SEL	I	System clock select: X'tal (External clock) select

OSC SEL	X'tal (Extarnal clock)
0	12.288 MHz
1	24.576 MHz

43	PD	I	Power down set: Internal CPU system clock select

PPD	PD	Internal CPU system clock
0	0	X'tal (External clock)/2
0	1	X'tal (External clock)/4
1	0	
1	1	X'tal (External clock)/8

Note: PPD is set in the test function register or external test register.

49	$\overline{\text{RESET}}$	I	Reset: LSI is RESET if this pin remains low level for over 6 cycles.

Common Part (cont)

Pin No.	Symbol	I/O	Function
84	TEST0	I	Mode set: LSI is set as follows by these pins.
85	TEST1		**T3 T2 T1 T0 Mode** 0 0 0 0 Normal Mode 0 0 0 1 Internal CPU Inactive for ASE In CPU inactive mode, the internal CPU is isolated from external pins. This mode sllows direct access to the internal CPU interface registers.
86	TEST2		
87	TEST3		
35	CIKINH	I	Clock Inhibit: If internal CPU executes SLP instruction with IOSTOP bit set to "1" (System stop mode) after this pin is high, PD pin (or PPD bit in register) is high and CLKSTP Enable bit set to "1", the oscillation circuit is disabled and the CPU CLK stays high. In this state, only the incoming detection circuit operates. When CLKINH is sent high, $\overline{WDT}$ goes low and a recovery request is issued to the external circuit. Sending the output of $\overline{WDT}$ to the RESET pin, to send it low, causes oscillation to be restarted.
36	CLKSTP	O	Clock Stop: This pin indicates the oscillation circuit state; it goes high in clock stop mode and low in normal mode.
37	$\overline{WDT}$	O	Watch Dog Timer: 1. When the watchdog timer elapses, this pin goes low for approximately 32 ms. A reset start is performed by feeding the $\overline{WDT}$ output into the $\overline{RESET}$ pin. 2. When the clock inhibit input (CLKINH) goes low in clock stop mdoe (CLKSTP = H), $\overline{WDT}$ goes low. If $\overline{WDT}$ is connected to the $\overline{RESET}$ pin, CLKSTP goes low and oscillation restarts. $\overline{WDT}$ will remain low for 20 to 72 ms after $\overline{RESET}$ goes low.

Internal CPU Part

Pin No.	Symbol	I/O	Function
48	$\overline{INT0}$	I/O (Open drain)	Interrupt 0: This input is request pin for maskable interrupt level 0. At this LSI, operation mode 2 (IM2; VECTER method) must be set. This pin is connected to internal interrupt factors, and each interrupt factors are controlled by daisy chain system. This pin must be connected to V_{CC} through resister (10 k – 100 kΩ).
47	$\overline{NMI}$	I	Non Maskable Interrupt: This pin is request pin for nonmaskable interrupt. Nomally connected to V_{CC}.
51	$\overline{RD}$	I (3-state)	Read: Indicates read cycle of internal CPU.
52	$\overline{WR}$	I (3-state)	Write: Indicates write cycle of internal CPU.
53	$\overline{ME}$	I (3-state)	Memory Enable: Indicates memory read/write cycle of internal CPU.
54	$\overline{IOE}$	I (3-state)	I/O Enable: Indicates I/O read/write cycle of internal CPU.
45	HALT	I/O	Halt: When internal CPU executes HALT or SLP operands, this output truns to "LOW" which means HALT/SLEEP/SYSTEM STOP mode.
50	LIR	I/O	Load Instruction Register: This output indicates that execution cycle is Op-code fetch cycle. However if LIRE bit in the operation mode control register is set to "0", this pin trun to "LOW" only during RETI instruction cycle or INT0 acknowledge cycle.
46	ST	O	Status: This signal indicates operation status as follows.

ST	HALT	LIR	Operation
0	1	0	CPU Operation (1st Ope-code cycle)
1	1	0	CPU Operation (2nd, 3rd Ope-code cycle)
1	1	1	CPU Operation (except for Ope-code cycle)
0	0	0	Halt Mode
1	0	1	Sleep/System Stop Mode

76 to 83	D7 to D0	I/O (3-state)	Data Bus: These are bi-directional 8 bits data buses of internal CPU. At L1MODE1, these pins trun to Q-bit input/output pins.
76 to 83	A0 to A15	I/O (3-state)	Address Bus: These are address pins for 16 bits memory space (64 kB). These go high impedance at reset status.
71 72 74 75	A16 A17 A18 A19	I/O (3-State)	Address Bus: These are address extension pins for MMU. These pins go "LOW" when the MMU is not used.
88 89	$\overline{RAMCS}$ $\overline{ROMCS}$	O	RAM and ROM Chip Selects: These pins output "LOW" when the address is in a spacified range during a memory accese (ME = "LOW"). These pins must be cinnected to the external RAM and ROM chips, respectively. The RAM address space can be from 0E00H to 0FFFFH, 0C000H to 0FFFFH or 08000H to 0FFFFH depending on internal register settings. The ROM address space is everthing outside the RAM space.

Layer 1 and Layer 2 Control Parts

Pin No.	Symbol	I/O	Function
19 20	LRA LRB	I	Line Receive A: Line Receive B: Input for the receive AMI signal. The bit rate is 192 kbps.
21 22	LTA LTB	O	Line Transmit A: Line Transmit B: Output for the transmit AMI signal. The bit rate is 192 kbps.
24	MODE M/S	I	Master/Slave Mode Select: • Slave mode at "LOW" level input • Master mode at "HIGH" level input
31 32	L1ACT L2ACT	I	Layer 1 Active: Layer 2 Active: Operation layer can be seleted as follows by these pins.

L1ACT	L2ACT	Mode	Function
1	0	L1MODE1	Layer 1 individual (1)
0	0	L1MODE2	Layer 1 individual (2)
0	1	L2MODE	Layer 2 individual
1	1	NORMAL	All layers operation

25	RCVSEL	I	Receive Timming Select: Receive timming select pin at master mode. At slave mode, "LOW" level should be input. • "LOW" level input; Receive synchronized mode. Receive side operates by clock synchronized to receive AMI. • "HIGH" level input; Transmit synchronized mode. Receive side operates by timming extracted from external 1.536 MHz clock.
13	BCH CLK SEL	I	Bch Clock Select: Select pin for Bch data input/output clock. This pin also switches input/output mode of CK8K pin and CK64K/128K pin.

Input	Synchronized Clock	CK8K	CK64K/128K
0	Internal clock	Output	Output
1	External clock	Input	Input

11	CK8K	I/O	Bch Frame Timming: Input/output pin for frame timing of RBA, RBB and TBA, TBB. This clock is not disabled by a reset cycle.
12	CK64K/128K	I/O	Bch Bit Timming: Input/output pin for bit timing of RBA, RBB, and TBA, TBB. This clock is not disabled by a reset cycle. A 64 kHz or 128 kHz clock is selected according to the bulk set bit in the B-channel select register (94H) or the external B-channel register. Normal mode; 64 kHz clock Bulk mode; 128 kHz clock

Layer 1 and Layer 2 Control Parts (cont)

Pin No.	Symbol	I/O	Function
6 7	RBA RBB	O	Raceive Bch Data A: Raceive Bch Data B: These are output pins for receive B1/B2 channel data. Can output B1 channel data, B2 channel data, or can be disabled ("HIGH") according to the B1 Enable, B2 Enable, and Exchange bits in the B-channel select register (94H) or the external B-channel register. The external clock register can be set to hold the RBA and RBB pins "LOW". Default Settings After a Reset • RBA; Receive B1 channel data • RBB; Receive B2 channel data
8 9	TBA TBB	I	Transmit B-ch Data A: Transmit B-ch Data B: These are input pins for transmit B1/B2 channel data. Can input B1 channel data, B2 channel data, or can be disabled ("HIGH") according to the B1 Enable, B2 Enable, and Exchange bits in the B-channel select register (94H) or the external B-channel register. Default Settings After a Reset • RBA; Receive B1 channel data • RBB; Receive B2 channel data
33	$\overline{SOD}$	O	Signal Detect Out: This output truns to "LOW", when a receive AMI signal is detected. If no input is received for 1.75 to 2.00 ms, this output truns to "HIGH".
26	TXSEL	I	Test Mode: This pin is used test mode. At normal mode, "LOW" level should be input.
27	CK4K	O	4 kHz Clock: 4 kHz clock of receive line flame output.
28	CK200	O	200 Hz Clock: M bit frame pulse output. This output truns only at multi frame (M-bit = "1")
14	RTIO	I/O	Dch Data Receive/Transmit Timing Clock: Input/output pin for 16 kHz clock. Duty isn't 50%.

Settings for Normal and Bulk Modes

Symbol	Normal Mode	Bulk Mode
RBA RBB	Receive B1 and B2 are output separately	Receive B1 + B2 is output
TBA TBB	Transmit B1 and B2 are input separately	Receive B1 + B2 is input
CK8K	8 kHz clock	8 kHz clock
CK64K/128K	64 kHz clock	128 kHz clock
Configuration	Separate 64 kb/s channels	128 kb/s channel

Note: The RBA/RBB and TBA/TBB pins are assigned to channels by B-channel select register or external B-channel register.

Layer 1 and Layer 2 Control Parts (cont)

Pin No.	Symbol	I/O	Function
15	RDIO	I/O	Receive D ch Data: Input/output pin for receive D ch data (HDLC format). Data input/output is synchronized to RTIO timing.
16	TDIO	I/O	Transmit D ch Data: Input/output pin for transmit D ch data (HDLC format). Data input/output is synchronized to RTIO timing. Input/output of above pins are controlled as follows.

	L1 Mode	L2 Mode	Normal Mode
RTIO	Output	Input	Output
RDIO	Output	Input	Output
TDIO	Input	Output	Output

10	CK1536	I/O	1.536 MHz Clock: • At master mode, input pin for transmit basis clock 1.536 MHz. • At slave mode, output pin of 1.536 MHz clock in DPLL.
30	ABIT/VDET	I	Abitset/Vdet: • At master mode, input pin for activation of layer 1. Only at L1MODE, this pin may be used. If this gose "HIGH" level, A-bit in the transmit frame trun to "1". At normal mode, this pin must be connected to V_{SS}. • At slave mode, input pin for power feed detection. Power feed detection is noticed to LSI by "HIGH" level input. If power is removed, layer 1 transmits Info 0 signal and TE is deactivated.
17	RE	O	Echo Bit Receive: Output pin for receive E-bit data (HDLC format). Data output is synchronized to RTIO timing.
29	SYNC	O	Synchronization: This pin indicates establishment of receive frame synchronization. • At master mode, this pin outputs "HIGH" level when frame alignment is established according to ITU-T I.430. • At slave mode, this pin outputs "HIGH" level when 3 consecutive "1"s of A-bit are detected after frame alignment.
5	LSW	I/O	Layer 1 Activation Switch: Input/output pin for layer 1 activation signal. • At L1MODE1, a "HIGH" input on this pin enables layer 1 part to activate. • At other mode, this is an output of internal CPU indication for layer 1 activation.
76 to 79	TQ4 to TQ1	I	Transmit Q-Bit: At L1MODE1, input pins for Q-bit or S-bit in the transmit frames. • At master mode, there are used to set S-bit. These should be input "LOW" level if Q-bit is not utilized. • At slave mode, there are used to set Q-bit. These should be input "HIGH" level if S-bit is not utilized.

Layer 1 and Layer 2 Control Parts (cont)

Pin No.	Symbol	I/O	Function
80 to 83	RQ4 to RQ1	O	Receive Q-Bit: At L1MODE1, output pins for Q-bit or S-bit in the receive frames. • At master mode, there are used to output Q-bit. • At slave mode, there are used to output S-bit.
143	$\overline{\text{DREQ}}$	I	Request for Transmit D ch: At L1MODE2, this input is requested the transmit D ch data to collision controlor by external LAP-D device.
144	$\overline{\text{DRAY}}$	O	Rady for Transmit D ch: At L1MODE2, this pin goes "LOW" to enable transmission from external LAP-D device.
2	CDETP	O	Collision Detect: At L1MODE2, indicates collision detect to external LAP-Device.

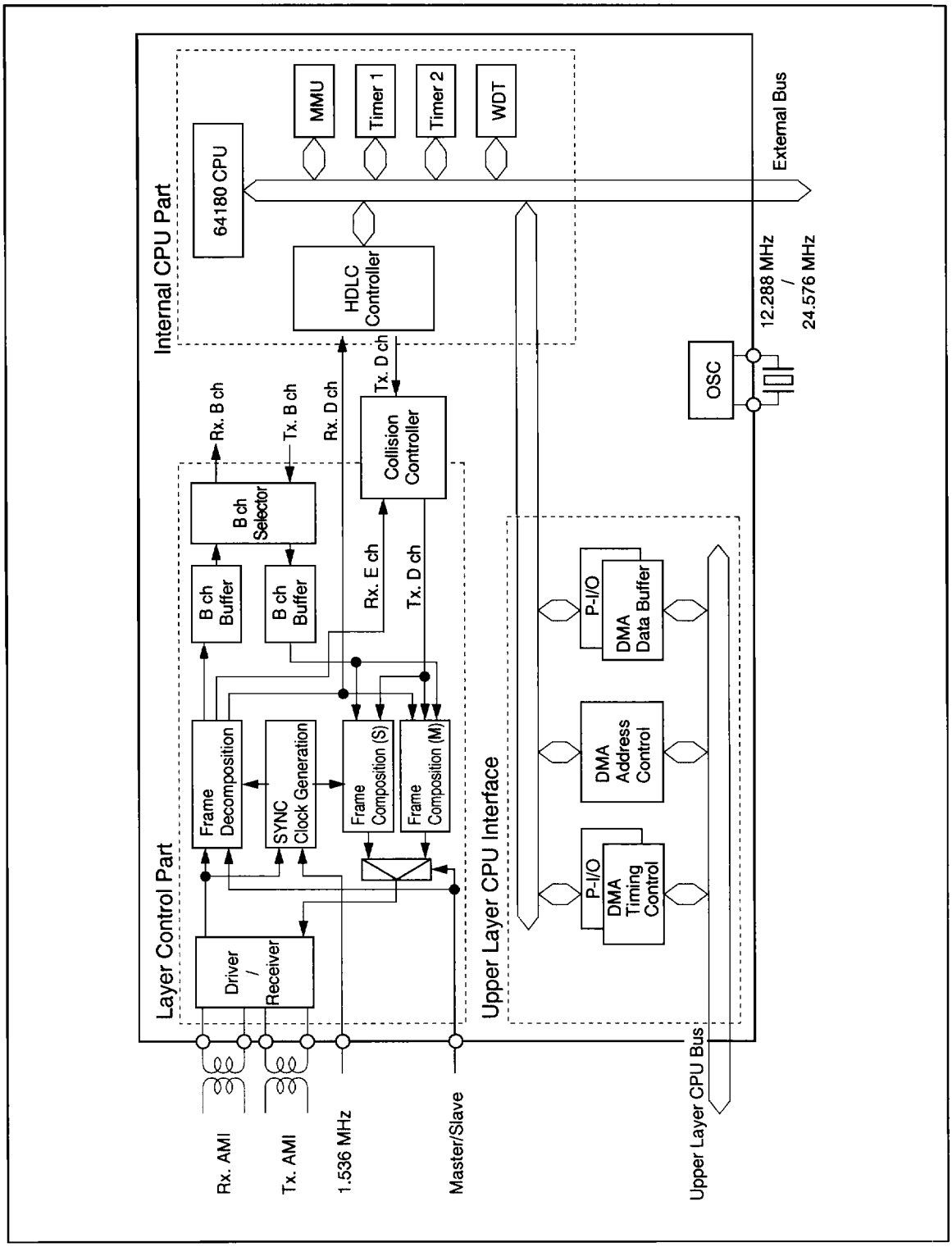
Upper Layer CPU Interface Part

Pin No.	Symbol	I/O	Function
129	DMA/IO	I	DMA/IO Mode Select: This pin sets transfer mode to upper CPU buses as follows. **DMA/IO** — **Transfer Mode** 0 — Programmed I/O Transfer Mode 1 — DMA Transfer Mode
130	B/W	I	Byte/Word Select: At DMA transfer mode, this pin sets data transfer width for upper CPU as follows. **B/W** — **Data Transfer Width** 0 — 8-bit 1 — 16-bit
131 132	CPU1 CPU2	I	CPU Type Select: These pins determine upper CPU types as follows. **CPU1** — **CPU2** — **CPU Type** 0 — 0 — 80 Type (8086 etc) 0 — 1 — 68 Type (68000 etc) 1 — 0 — H8 Type (H8/500, H8/300H etc)
134	$\overline{CS}$	I	Chip Select: This is used by upper CPU to select this LSI when this signal is active "LOW". This pin is available during programmed transfer input/output at programmed I/O transfer mode or DMA transfer mode. During DMA transfer at DMA transfer mode, this pin must be remained "HIGH" level.
91 to 98	OD0 to OD7	I/O (3-state)	Data Bus for Upper CPU: There are bi-directional 8 bits buses for upper CPU interface.
99 to 106	OD8 to OD15	I/O (3-state)	Data Bus for Upper CPU: At DMA transfer mode, there are bi-directional for upper CPU interface when 16-bit data transfer width is selected.
107 108 110	OAD0 OAD0 OAD2	I/O (3-state)	Address Bus for Upper CPU: During programmed transfer, upper CPU interface registers are selected by this pins. During DMA transfer, there are outputs of DMA address.
111 to 126	OAD3 to OAD18	O (3-state)	Address Bus for Upper CPU: There are outputs of DMA address during DMA transfer.
127	OAD19	I/O (3-state)	Address Bus for Upper CPU: This is output of DMA address except for 80 type or H8 type selection. In case of selecting 80 type or H8 type, this is used as $\overline{READY}$ or $\overline{WAIT}$. $\overline{READY}$ or $\overline{WAIT}$ signal is active "LOW".

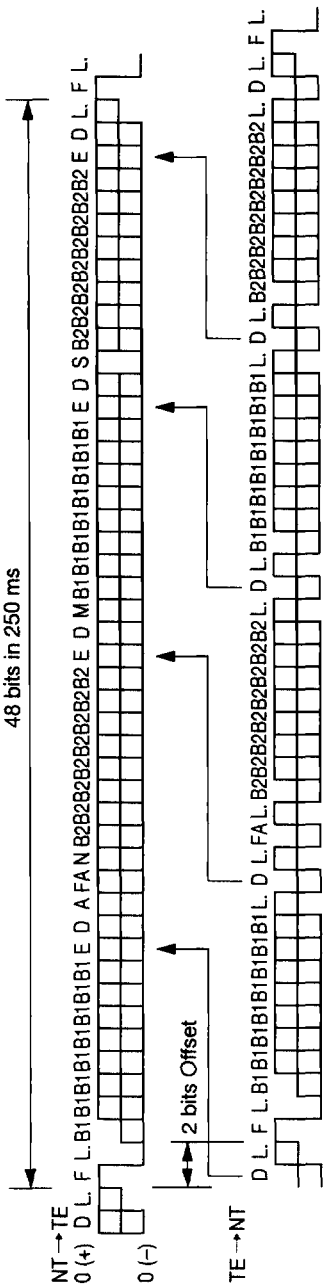
Upper Layer CPU Interface Part (cont)

Pin No.	Symbol	I/O	Function
133	$\overline{INTR}$	O (open drain)	Interrupt Request to Upper CPU: This output indicates interrupt to upper CPU. Upper CPU must to read the upper interrupt source register after accepts interrupt request. This pin outputs logical OR the interrupt factors in the upper interrupt source register. This is "LOW" active.
4	L3CLK	I	Upper CPU System Clock: System clock input of upper CPU.
139	$\overline{OWR}$	I/O (3-state)	Write for Upper CPU: This pin corresponds to $\overline{WR}$ of 8086 and R/$\overline{W}$ of 68000. This is "LOW" active.
140	$\overline{ORD}$	I/O (3-state)	Read for Upper CPU: This pin corresponds to RD of H8 and 8086. This is "LOW" active.
144	HOLT	O	Hold Request for Upper CPU: This pin is output of bus request signal which corresponds to HOLD ("HIGH" active) of 8086, $\overline{BREQ}$ ("LOW" active) of H8 and $\overline{BR}$ ("LOW" active) of 68000.
143	HLTA	I	Hold Acnowledgment from Upper CPU: Bus release signal from upper CPU is provided to this pin. This signal corresponds to HLDA ("HIGH" active) of 8086, $\overline{BACK}$ ("LOW" active) of H8 and $\overline{BG}$ ("LOW" active) of 68000.
141	$\overline{M}$/IO	I/O (3-state)	Memory Request to 8086 Bus: This gose "LOW" level during DMA transfer at 80 type, which corresponds to inverted signal of M/IO.
138	$\overline{AS}$	I/O (3-state)	Address Strobe: This pin corresponds to AS of H8 and 68000. This is "LOW" active.
135	$\overline{UDS}$	I/O (3-state)	Upper Data Strobe: This is used only at DMA transfer mode. This pin corresponds to $\overline{BHE}$ of 8086, $\overline{UDS}$ of 68000 and $\overline{HWR}$ of H8. During DMA transfer, this pin goes "LOW" and selects upper byte of data buses.
137	$\overline{LDS}$	I/O (3-state)	Lower Data Strobe: This pin corresponds to A0 of 8086, $\overline{LDS}$ of 68000. On H8 bus, this pin will be connected to write signal ($\overline{WR}$, $\overline{LWR}$ or $\overline{HWR}$). During DMA transfer, this pin goes "LOW" and selects lower byte of data buses.
136	$\overline{DTA}$	I/O (3-state)	Data Transfer Acknowledge: This pin corresponds to $\overline{DTACK}$ of 68000. This is "LOW" active.
142	$\overline{BGA}$	I/O (3-state)	Bus Grant Acknowledge: This pin corresponds to $\overline{BGACK}$ of 68000. This is "LOW" active.
3	EXHOLT	I	External Bus Master Hold: This is connected to bus request signal from external DMAC. If there is bus request of external DMAC, this LSI will execute bus arbitration between internal and external DMACs. When unused, this pin must be set as follows. This pin is valid only at DMA transfer mode. • 80 Type; Pull down • H8 Type, 68000 Type; Pull up
2	EXHLTA	O	HLTA to External Bus Master: This is HOLD acknowledge signal to external DMAC. This pin is valid only at DMA transfer mode.

Block Diagram



Frame Structure at Reference Point S and T



F = Framing Bit
L. = DC Balancing Bit
D = D-Channel Bit
E = D-Echo-Channel bit
FA = Auxiliary Framing Bit
N = Bit set to binary value N = Not (FA)
B1 = Bit within B-Channel 1
B2 = Bit within B-Channel 2
A = Bit used for activation
S = Reserved for future standadization
M = Multiframing Bit

Notes: 1. Dots (.) demarcate those parts of the frame that are independenty DC-balanced.
2. FA Bit (TE → NT) is used as Q-Bit every 5 frame at mutiframing.
3. Nominal 2 bits offset is applied at TE output. The offset at NT point might become large by the interface cable delay or connection configration.

Electrical Characteristics (V_{CC} = 5 V ± 5%, V_{SS} = 0 V, Ta = –20 to 75°C unless otherwise noted)

DC Characteristics

Item	Symbol	Min	Typ	Max	Unit	Test condition
Input "HIGH" voltage $\overline{\text{RESET}}$, EXTAL, $\overline{\text{NMI}}$, VDET, TEST0, TEST1, TEST2, TEST3	V_{IH1}	V_{CC} – 0.6	—	V_{CC} + 0.3	V	
Input "HIGH" voltage other inputs	V_{IH2}	2.2	—	V_{CC} + 0.3	V	
Input "LOW" voltage $\overline{\text{RESET}}$, EXTAL, $\overline{\text{NMI}}$, VDET, TEST0, TEST1, TEST2, TEST3	V_{IL1}	–0.3	—	0.6	V	
Input "LOW" voltage other inputs	V_{IL2}	–0.3	—	0.8	V	
Output "HIGH" voltage all outputs	V_{OH}	2.4	—	—	V	I_{OH} = –200 µA
		V_{CC} – 1.2	—	—	V	I_{OH} = –20 µA
Output "LOW" voltage all outputs	V_{OL}	—	—	0.45	V	I_{OL} = 2.2 mA
Input leakage current inputs except extal	$\lvert I_{IL} \rvert$	—	—	10	µA	Vin = 0.5 V to V_{CC} – 0.5 V
Three-state current	$\lvert I_{TL} \rvert$	—	—	10	µA	Vin = 0.5 V to V_{CC} – 0.5 V
Power dissipation*1 (Normal operation)	I_{CC1}	—	30	45	mA	OSC = 12.288 MHz, f = 6.144 MHz
		—	22	33	mA	OSC = 12.288 MHz, f = 3.072 MHz
	I_{CC2}	—	42	63	mA	OSC = 24.576 MHz, f = 12.288 MHz
		—	33	50	mA	OSC = 24.576 MHz, f = 6.144 MHz
Power dissipation*1 (Clock stop mode)	I_{CCSTP}	—	—	550	µA	
Pin capacitance	C_P	—	—	15	pF	

Note: 1. At no load expect 50 Ω load resistance of ITU-T recomentations.

AC Characteristics

Lain Interface

Item	Symbol	Min	Typ	Max	Unit	Test condition
Delay between RCV. data and TX. data	Rtd	—	2.0	—	bit	Figure 1
X'tal frequency deviation	D_{XTL}	–100	—	+100	p.p.m	I.430 8.1.2
Timing extraction jitter	J	–7	—	+7	%	I.430 8.2.2
Total phase deviation	TPD	–7	—	+15	%	I.430 8.2.3
Tolerance round trip delay	Drt	10	—	14	μs	I.430 A2.1.2
Receiver input voltage	V_{LR}	0.3	—	V_{CC} + 0.3	V	Figure 4
Receiver input impedance	Z_{LR}	—	5	—	kΩ	
Transmitter output pulse amplitude	V_{LT50}	1350	—	1650	mV	Correspond to R_L = 50 Ω of I.430. Figures 3, 4
	V_{LT400}	1350	—	2400	mV	Correspond to R_L = 400 Ω of I.430. Figures 3, 4
	V_{LT56}	—	—	300	mV	Correspond to R_L = 5.6 Ω of I.430. Figures 3, 4
Transmitter output impedance	Z_{LT0}	—	24	—	Ω	
	Z_{LT1}	—	5	—	kΩ	
Transmitter output pulse rise time	t_{LTr}	—	450	—	ns	Figure 4
Transmitter output limit current	I_{LT}	—	—	13	mA	

B-Channel Interface

Item	Symbol	Min	Typ	Max	Unit	Test condition
Clock period (Normal mode)	t_{BCYCN}	15.623	—	15.627	µs	Figure 5 (f = 64 kHz)
Clock period (Bulk mode)	t_{BCYCB}	7.811	—	7.814	µs	Figure 6 (f = 128 kHz)
Clock duty	Duty	45	50	55	%	Figure 5, 6, D = t_{CH}/t_{CYC}
Clock rise time	t_{cr}	—	—	50	ns	Figure 5, 6
Clock fall time	t_{cf}	—	—	50	ns	
Frame clock deviation	t_{CD}	–80	—	80	ns	
RCV. data output delay	t_{BD}	—	—	1	µs	
TX. data det-up time	t_{BS}	3	—	—	µs	
TX. data hold time	t_{Bh}	3	—	—	µs	

D-Channel Interface

Item	Symbol	Min	Typ	Max	Unit	Test condition
Timing clock period	t_{RTCYC}	62.49	62.50	62.51	µs	Figure 7 (RTIO)
Timing clock rise time	t_{RTr}	—	—	50	ns	
Timing clock fall time	t_{RTf}	—	—	50	ns	
RCV. D ch data output delay (Normal mode)	t_{RD}	—	—	1.0	µs	Figure 7 (RDIO)
TX. D ch data output timing (Normal mode)	t_{TD}	—	—	1.0	µs	Figure 7 (TDIO)
RCV. D ch data input delay (Layer 2 mode)	t_{RD}	0	—	1.0	µs	Figure 7 (RDIO)
TX. D ch data input timing (Layer 1 mode)	t_{TD}	0	—	1.0	µs	Figure 7 (TDIO)

E-bit Interface

Item	Symbol	Min	Typ	Max	Unit	Test condition
RCV. E-bit data output timing	t_{RE}	5.8	—	9.7	µs	Figure 8

Internal CPU Interface

Item	Symbol	Min	Typ	Max	Unit	Test condition
Clock period	t_{CYC}	81	—	666	ns	Figure 11
Clock pulse width "HIGH"	t_{CHW}	30	—	—	ns	
Clock pulse width "LOW"	t_{CLW}	30	—	—	ns	
Clock fall time	t_{cf}	—	—	10	ns	
Clock rise time	t_{cr}	—	—	10	ns	
External clock rise time	t_{EXr}	—	—	25	ns	Figure 9
External Clock fall time	t_{EXf}	—	—	25	ns	
Address delay time	t_{AD}	—	—	40	ns	Figure 11
Address set-up time (for $\overline{ME}$ or $\overline{IOE}$ ↓)	t_{AS}	10	—	—	ns	
ME delay time 1	t_{MED1}	—	—	35	ns	
RD delay time 1*1	t_{RDD1}	—	—	35	ns	
LIR delay time 1	t_{LD1}	—	—	35	ns	
Address hold time (for $\overline{ME}$, $\overline{IOE}$, $\overline{RD}$ or $\overline{WR}$ ↑)	t_{AH}	15	—	—	ns	
$\overline{ME}$ delay time 2	t_{MED2}	—	—	35	ns	
$\overline{RD}$ delay time 2	t_{RDD2}	—	—	35	ns	
$\overline{LIR}$ delay time 2	t_{LD2}	—	—	35	ns	
Data read set-up time	t_{DRS}	20	—	—	ns	Figures 11, 12
Data read hold time	t_{DRH}	0	—	—	ns	
ST delay time 1	t_{STD1}	—	—	35	ns	Figure 11
ST delay time 2	t_{STD2}	—	—	35	ns	
Write data floating delay time	t_{WDZ}	—	—	40	ns	
$\overline{WR}$ delay time 1	t_{WRD1}	—	—	35	ns	
Write data delay time	t_{WDD}	—	—	40	ns	
Write data set-up time (for $\overline{WR}$ ↓)	t_{WDS}	10	—	—	ns	
$\overline{WR}$ delay time 2	t_{WRD2}	—	—	35	ns	
$\overline{WR}$ pulse width	t_{WRP}	100	—	—	ns	
Write data hold time (for $\overline{WR}$ ↑)	t_{WDH}	15	—	—	ns	
$\overline{IOE}$ delay time 1*1	t_{IOD1}	—	—	35	ns	
$\overline{IOE}$ delay time 2	t_{IOD2}	—	—	35	ns	

Internal CPU Interface (cont)

Item	Symbol	Min	Typ	Max	Unit	Test condition
$\overline{IOE}$ delay time 3 (for $\overline{LIR}$ ↓)	t_{IOD3}	170	—	—	ns	Figure 12
$\overline{INT0}$ set-up time (for CPU CLK ↓)	t_{INTS}	20	—	—	ns	
$\overline{INT0}$ hold time (for CPU CLK ↓)	t_{INTH}	20	—	—	ns	
$\overline{NMI}$ pulse width	t_{NMIW}	80	—	—	ns	
$\overline{HALT}$ delay time 1	t_{HAD1}	—	—	35	ns	
$\overline{HALT}$ delay time 2	t_{HAD2}	—	—	35	ns	
$\overline{ROMCS}$ delay time	t_{ROMCSD}	—	—	35	ns	Figure 11
$\overline{ROMCS}$ delay time	t_{RAMCSD}	—	—	35	ns	
$\overline{RESET}$ set-up time	t_{RES}	50	—	—	ns	
$\overline{RESET}$ hold time	t_{REH}	30	—	—	ns	
$\overline{RESET}$ rise time*2	t_{Rr}	—	—	50	ns	
$\overline{RESET}$ fall time*2	t_{Rf}	—	—	50	ns	
Input terminal rise time*2 (Except $\overline{RESET}$)	t_{Ir}	—	—	100	ns	Figure 11
Input terminal fall time*2 (Except $\overline{RESET}$)	t_{If}	—	—	100	ns	
Oscillation start time	t_{OSC}	—	—	15	ms	Figure 10
Valid $\overline{RESET}$ pulse width	t_{RVALID}	6	—	—	cycle	

Notes: 1. There values are specified from CPUCLK falling edge at IOC = "1", otherwise from CPUCLK rising edge at IOC = "0" (Z80 compatible mode).

2. Even if specification are satisfied, when other specification are not, rise time and fall time should best be satisfied with such specifications.

80 Type Bus Interface

I/O Bus Interface

Item	Symbol	Min	Typ	Max	Unit	Test condition
$\overline{ORD}$, $\overline{OWR}$ active delay 1	t_{CSD}	0	—	—	ns	Figure 13
$\overline{ORD}$, $\overline{OWR}$ active delay 2	t_{ADD}	0	—	—	ns	
Data output delay time	t_{DD}	—	—	120	ns	
Data output hold time	t_{DH}	0	—	—	ns	
Address, $\overline{CS}$ hold time	t_{AH}	20	—	—	ns	
Data set-up time	t_{DSUP}	60	—	—	ns	
Data hold time	t_{DHL}	35	—	—	ns	
$\overline{ORD}$ pulse width	t_{WRD}	160	—	—	ns	
$\overline{OWR}$ pulse width	t_{WWR}	120	—	—	ns	

DMA Bus Interface

Item	Symbol	Min	Typ	Max	Unit	Test condition
Clock period	t_{CLCL}	100	—	500	ns	Figure 14
Clock pulse width "LOW"	t_{CLCH}	40	—	—	ns	
Clock pulse width "HIGH"	t_{CHCL}	40	—	—	ns	
Clock rise time	t_{CH1CH2}	—	—	10	ns	
Clock fall time	t_{CL2CL1}	—	—	10	ns	
HLDA set-up time	t_{HAVCV}	60	—	—	ns	
Signal valid delay	t_{DMD}	—	—	100	ns	
Address hold time	t_{AHLD}	20	—	—	ns	
Data hold time	t_{CLDXDM}	0	—	—	ns	
Data set-up time	t_{DVCLDM}	60	—	—	ns	
Write data hold time	t_{WHDXDM}	20	—	—	ns	
READY set-up time	t_{RDYSET}	60	—	—	ns	
READY hold time	t_{RDYHLD}	60	—	—	ns	

68000 Type Bus Interface

I/O Bus Interface

Item	Symbol	Min	Typ	Max	Unit	Test condition
$\overline{CS}$ "L" → $\overline{AS}$, $\overline{LDS}$ "L" delay time	t_{CSVSL}	0	—	—	ns	Figure 15
Address valid → $\overline{AS}$, $\overline{LDS}$ "L" delay time	t_{ADVSL}	0	—	—	ns	
$\overline{AS}$, $\overline{LDS}$ "H" → Address, $\overline{CS}$ invalid delay time	t_{SHAI}	20	—	—	ns	
$\overline{AS}$, $\overline{LDS}$ pulse width "LOW" ($\overline{LDS}$ for only read cycle)	t_{SL}	160	—	—	ns	
$\overline{OWR}$ "H" → $\overline{AS}$, $\overline{LDS}$ "L" (Read cycle)	t_{RHSL}	50	—	—	ns	
$\overline{LDS}$ pulse width "LOW" (Write cycle)	t_{DSL}	120	—	—	ns	
$\overline{OWR}$ "L" → $\overline{AS}$, $\overline{LDS}$ "L" (Write cycle)	t_{RLSL}	50	—	—	ns	
$\overline{AS}$, $\overline{LDS}$ "H" → $\overline{OWR}$ "H"	t_{SHRH}	0	—	—	ns	
$\overline{AS}$, $\overline{LDS}$ "L" → $\overline{DTA}$ "L" delay time	t_{DSTR}	—	—	100	ns	
$\overline{AS}$, $\overline{LDS}$ "H" → $\overline{DTA}$ "H" delay time	t_{SHDAH}	—	—	100	ns	
$\overline{AS}$, $\overline{LDS}$ "L" → Data output delay (Read cycle)	t_{SLDO}	—	—	120	ns	
$\overline{AS}$, $\overline{LDS}$ "H" → Data output hold (Read cycle)	t_{SHDOH}	0	—	—	ns	
Input data set-up time (Write cycle)	t_{DIVSH}	60	—	—	ns	
Input data hold time (Write cycle)	t_{SHDII}	35	—	—	ns	

DMA Bus Interface

Item	Symbol	Min	Typ	Max	Unit	Test condition
Clock period	t_{CYC}	100	—	500	ns	Figure 16
Clock pulse width "LOW"	t_{CL}	40	—	—	ns	
Clock pulse width "HIGH"	t_{CH}	40	—	—	ns	
Clock rise time	t_{CR}	—	—	10	ns	
Clock fall time	t_{CF}	—	—	10	ns	
$\overline{BG}$ set-up time	t_{BGST}	60	—	—	ns	
Strobe, R/$\overline{W}$ float delay	t_{GLZ}	—	—	100	ns	
$\overline{BGA}$ "L" → $\overline{BG}$ "H" delay	t_{GALGH}	1.5	—	3.0	Clock	
$\overline{BGA}$ "L" → $\overline{BG}$ "H" delay	t_{BGKBR}	20	—	—	ns	
$\overline{BGA}$ valid time	t_{BGAD}	—	—	100	ns	
CLK "L" → Signal delay time	t_{CLAVD}	—	—	100	ns	Figure 17
CLK "H" → Signal delay time	t_{CHAVD}	—	—	100	ns	
$\overline{DTA}$ set-up time	t_{DKST}	60	—	—	ns	
$\overline{DTA}$ hold time	t_{DKLH}	10	—	200	ns	
Address set-up time	t_{AVSL}	20	—	—	ns	
Data set-up time	t_{DICLD}	60	—	—	ns	
Data hold time	t_{SHDID}	20	—	—	ns	
Output data hold time	t_{SHDOI}	20	—	—	ns	

H8 Type Bus Interface

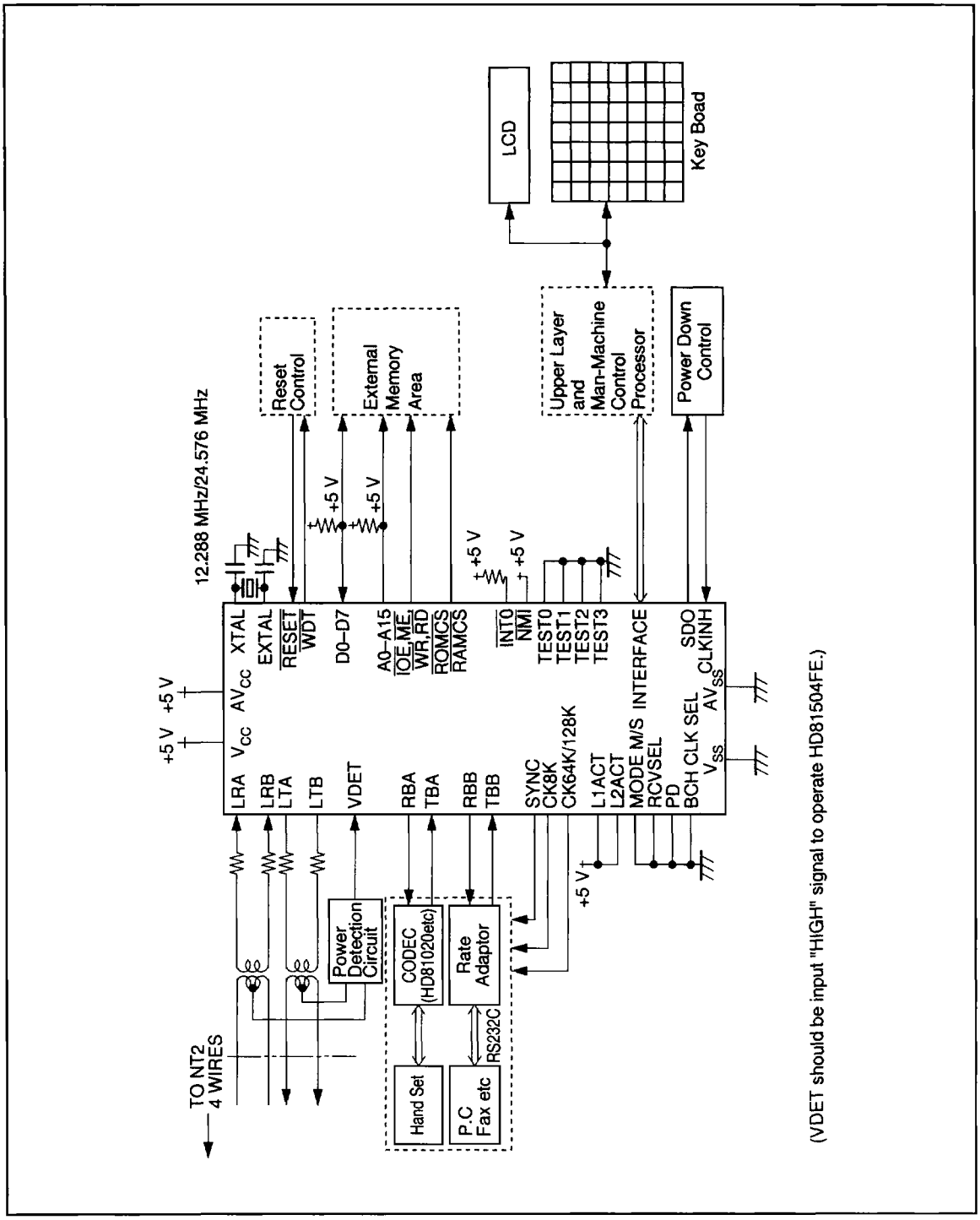
I/O Bus Interface

Item	Symbol	Min	Typ	Max	Unit	Test condition
$\overline{AS}$ active delay 1	t_{CSD}	0	—	—	ns	Figure 18
$\overline{AS}$ active delay 2	t_{AD}	0	—	—	ns	
Address, $\overline{CS}$ hold time	t_{AHL}	20	—	—	ns	
$\overline{AS}$ pulse width	t_{WAS}	160	—	—	ns	
$\overline{ORD}$ pulse width	t_{WRD}	160	—	—	ns	
Data output delay time	t_{RDD}	—	—	120	ns	
Data output hold time	t_{RDHL}	0	—	—	ns	
Write signal pulse width	t_{WWR}	120	—	—	ns	
Data set-up time	t_{WDSUP}	60	—	—	ns	
Data hold time	t_{WDHL}	35	—	—	ns	

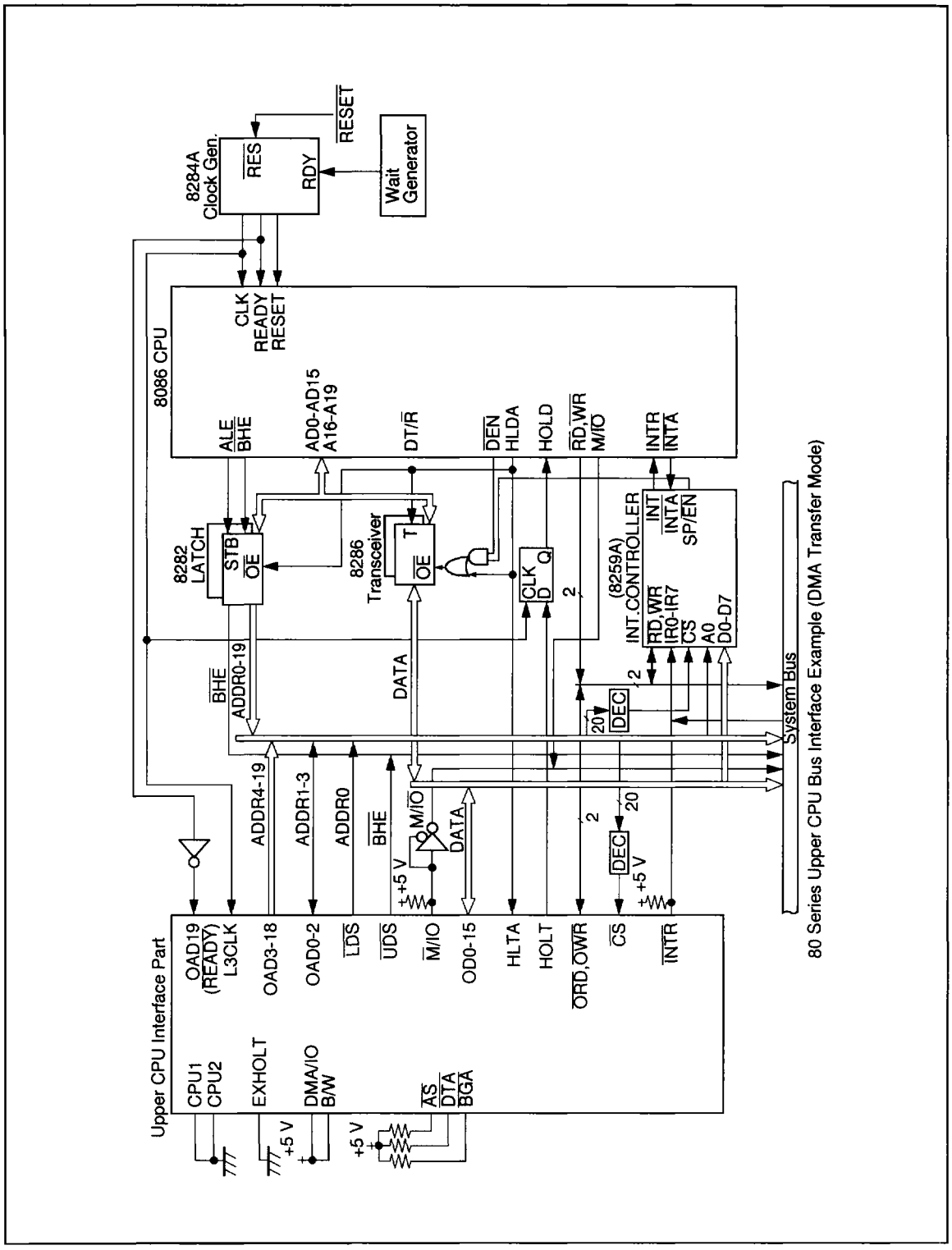
DMA Bus Interface

Item	Symbol	Min	Typ	Max	Unit	Test condition
Clock period	t_{CYC}	100	—	500	ns	Figure 19
Clock pulse width "HIGH"	t_{CH}	40	—	—	ns	
Clock pulse width "LOW"	t_{CL}	40	—	—	ns	
Clock rise time	t_{CR}	—	—	10	ns	
Clock fall time	t_{CF}	—	—	10	ns	
$\overline{BACK}$ set-up time	t_{BACKS}	60	—	—	ns	
Valid signal delay time	t_{DVLD}	—	—	100	ns	
$\overline{WAIT}$ set-up time	t_{WTS}	60	—	—	ns	
$\overline{WAIT}$ hold time	t_{WTH}	60	—	—	ns	
Write data hold time	t_{WDH}	20	—	—	ns	
Read data set-up time	t_{RDS}	60	—	—	ns	
Read data hold time	t_{RDH}	0	—	—	ns	
Address set-up time	t_{AS}	20	—	—	ns	
Address hold time	t_{AH}	20	—	—	ns	

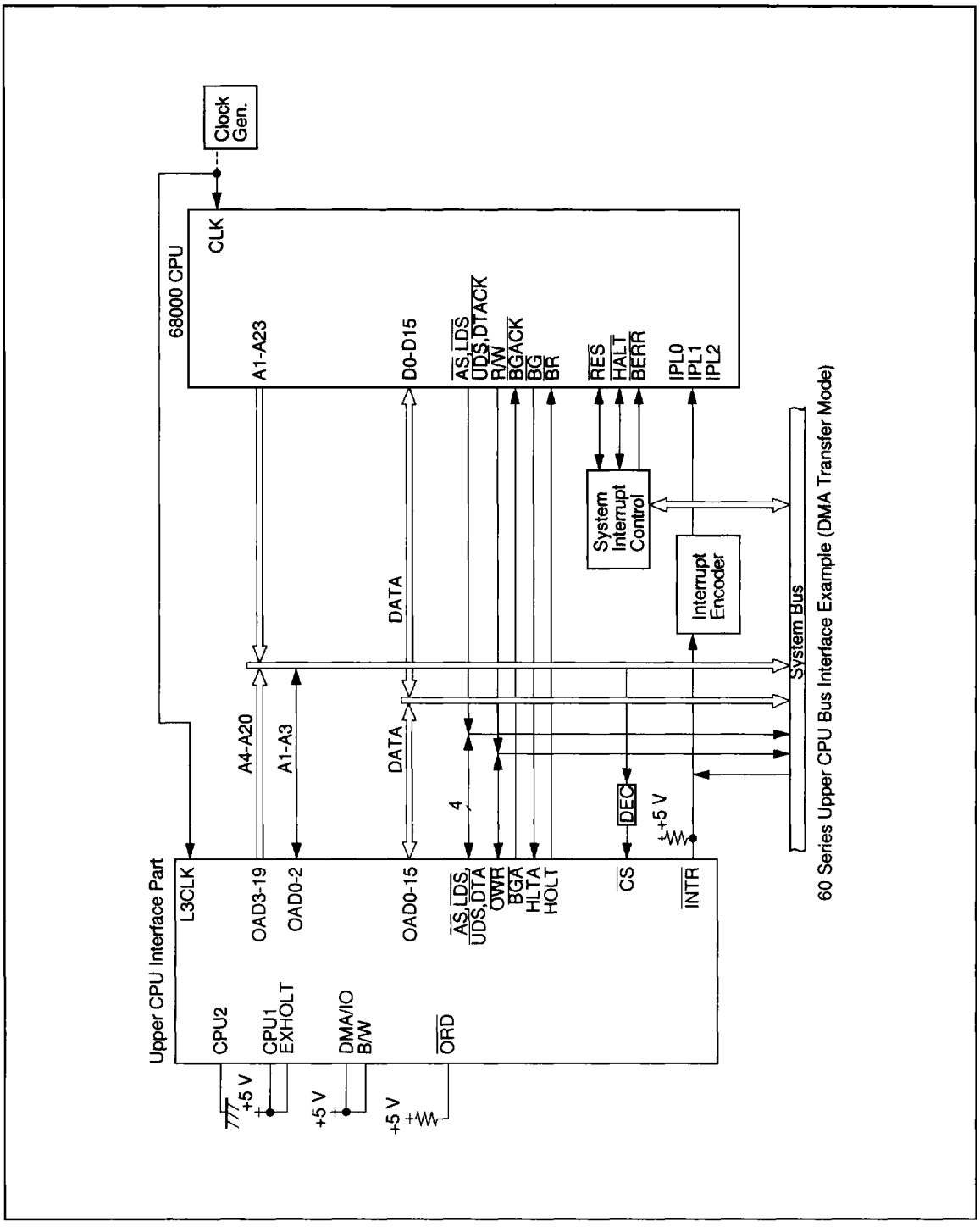
Application for Digital Telephone



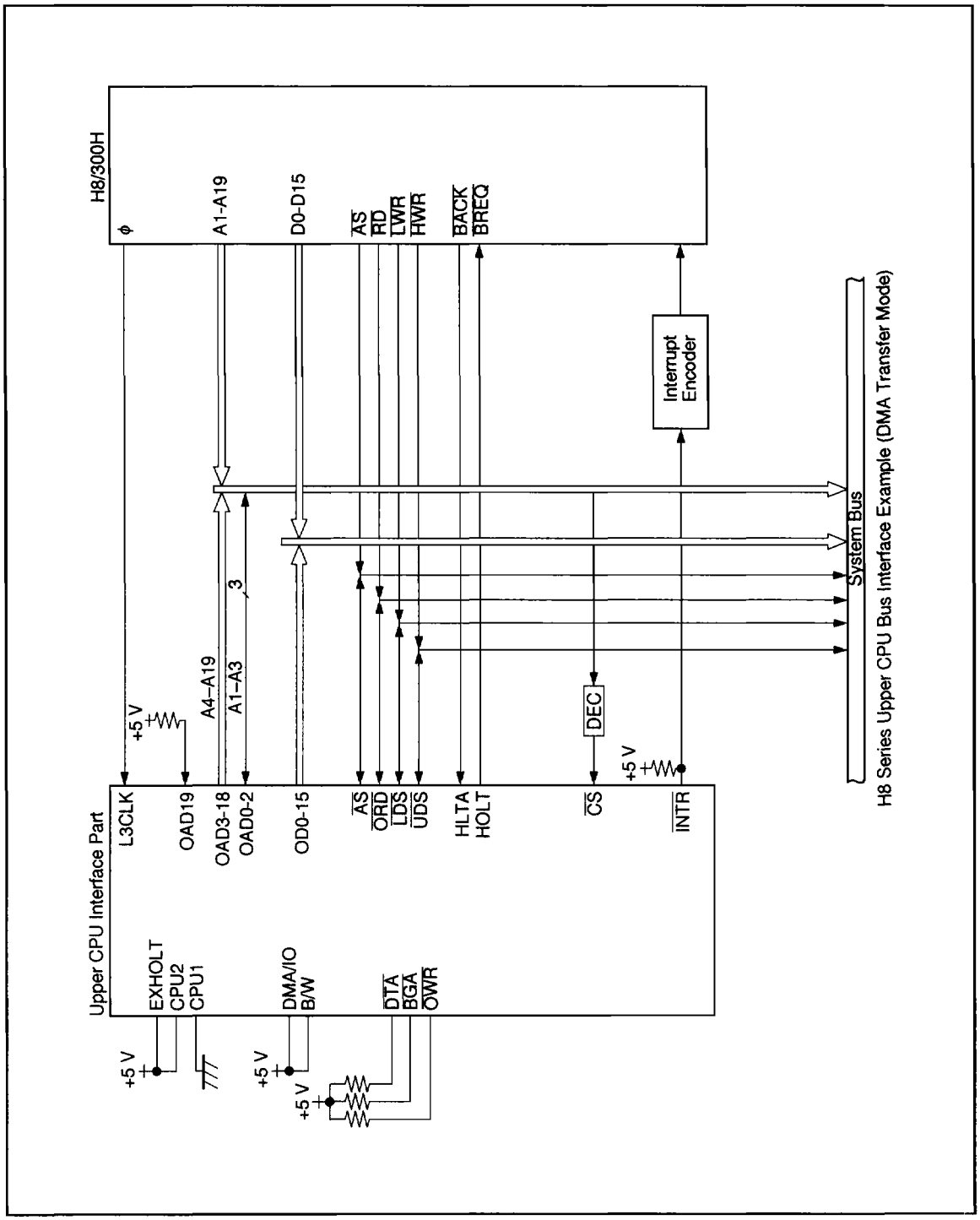
80 Series Upper CPU Interface Example (DMA Transfer Mode)



60 Series Upper CPU Interface Example (DMA Transfer Mode)



H8 Series Upper CPU Interface Example (DMA Transfer Mode)



Timing Chart

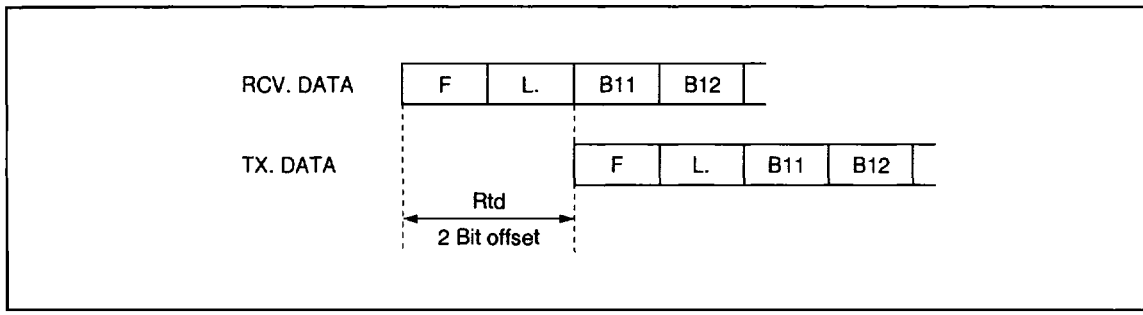


Figure 1 The Offset from Receive Data to Transmit Data at TE Mode

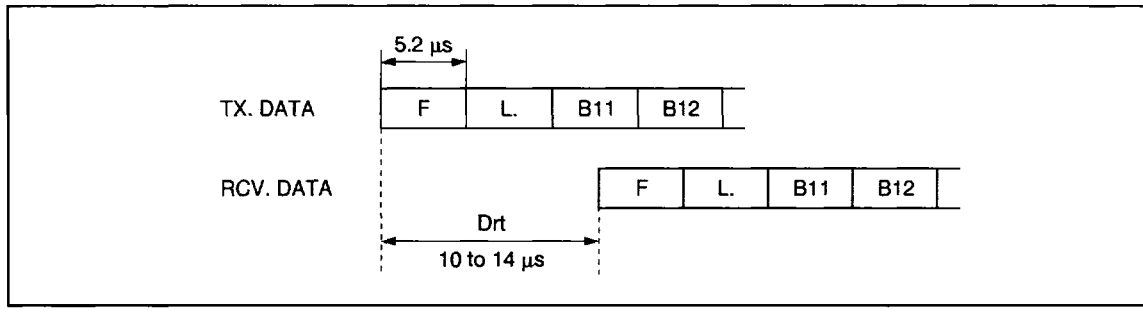


Figure 2 Torelance Round Trip Delay in Short Passive Bus at NT Mode

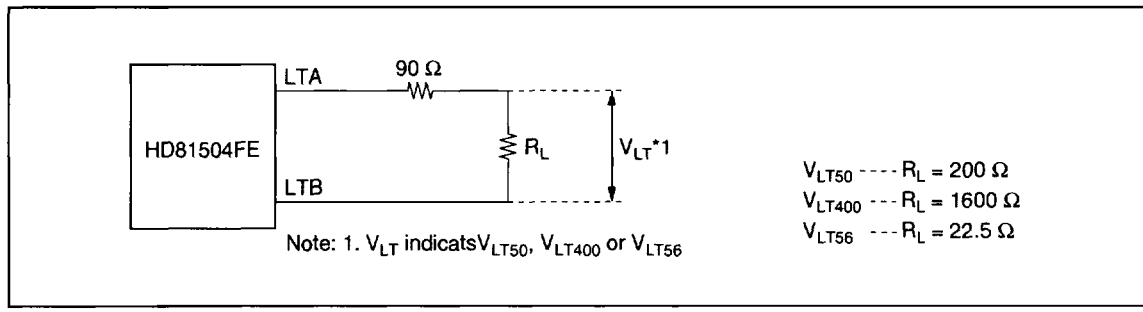


Figure 3 Driver Output Test Circuit

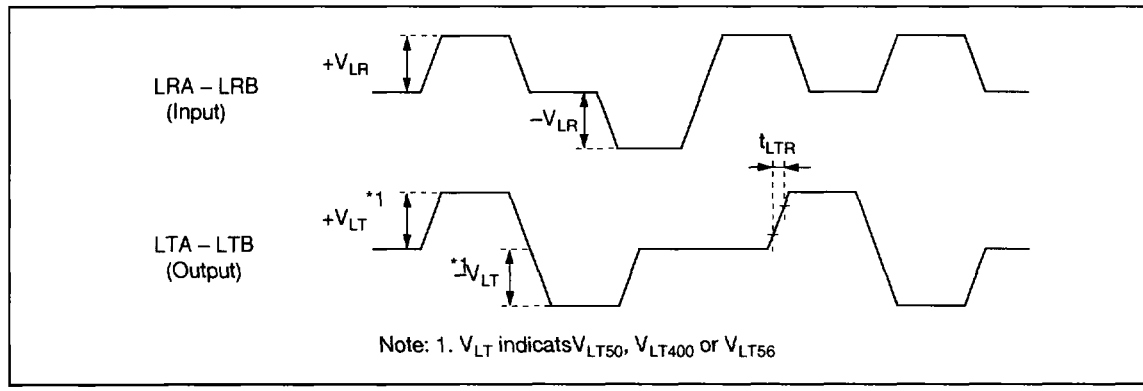


Figure 4 Receiver Input/Driver Output

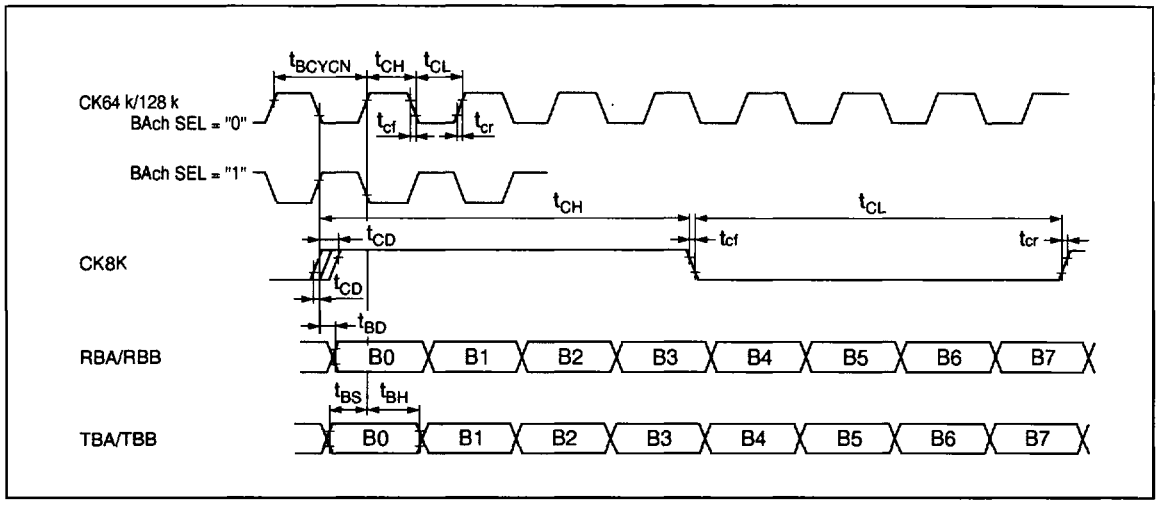


Figure 5 Bch Data Input/Output Timing (BULKSET = 0...Normal Mode)

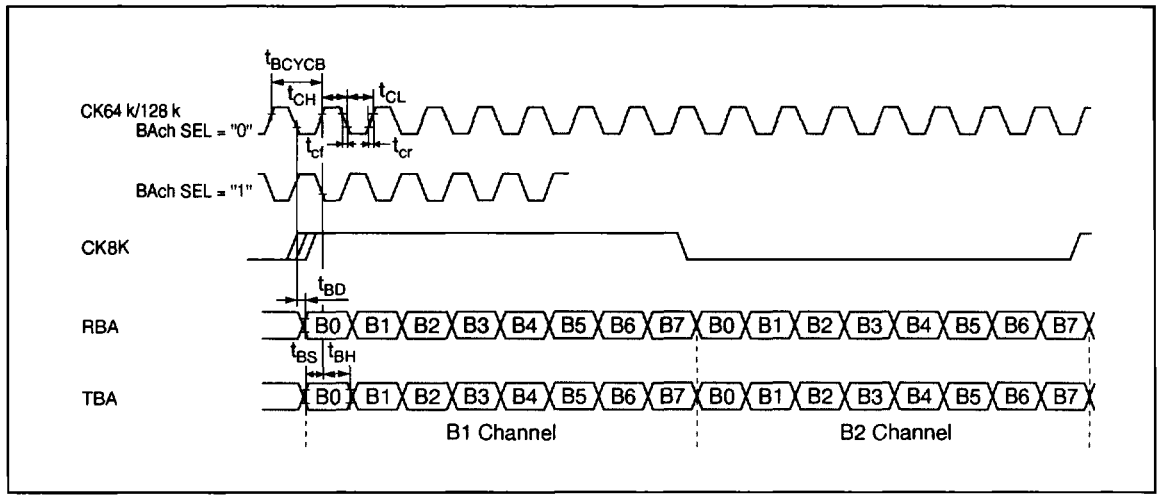


Figure 6 Bch Data Input/Output Timing (BULKSET = 1...Bulk Mode)

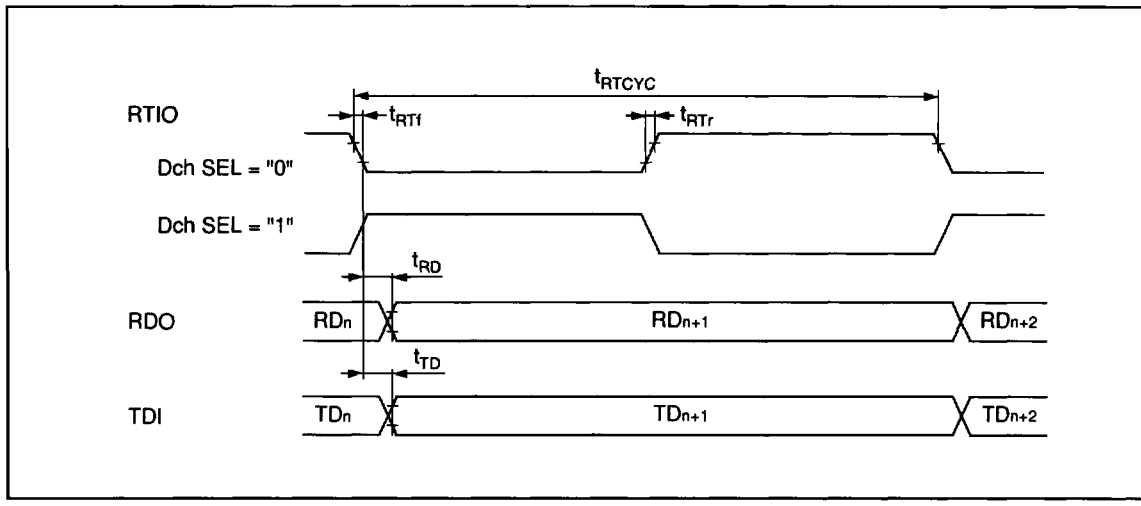


Figure 7 Dch Input/Output Timing

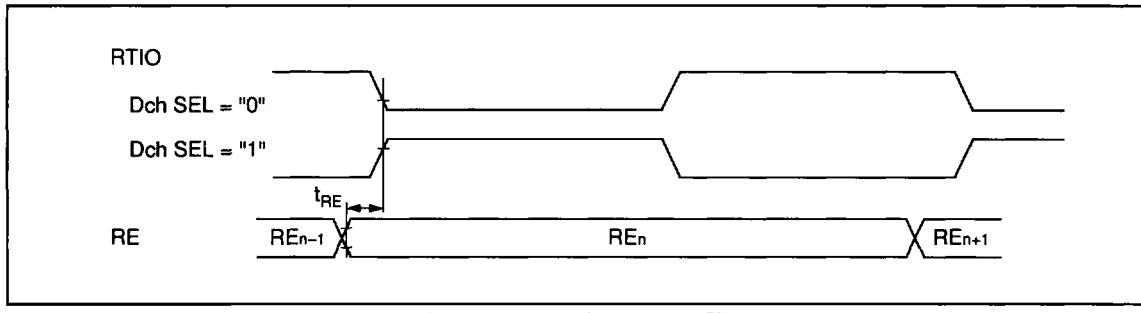


Figure 8 E-bit Output Timing

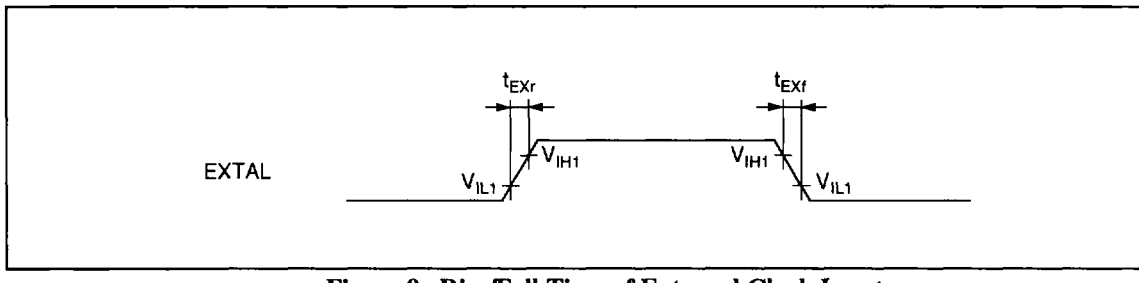


Figure 9 Rise/Fall Time of External Clock Input

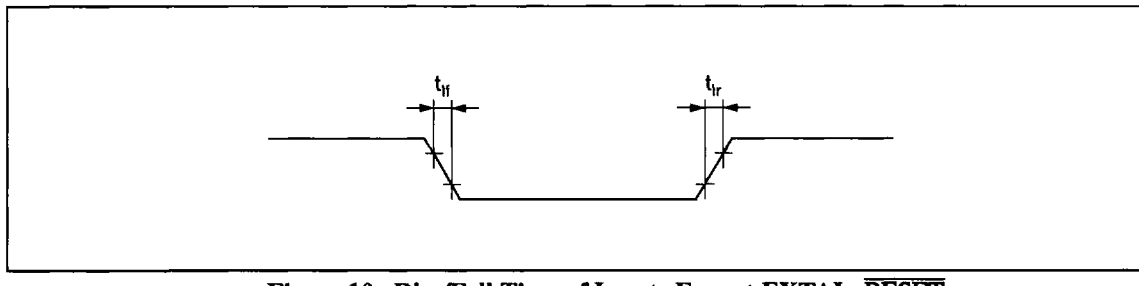
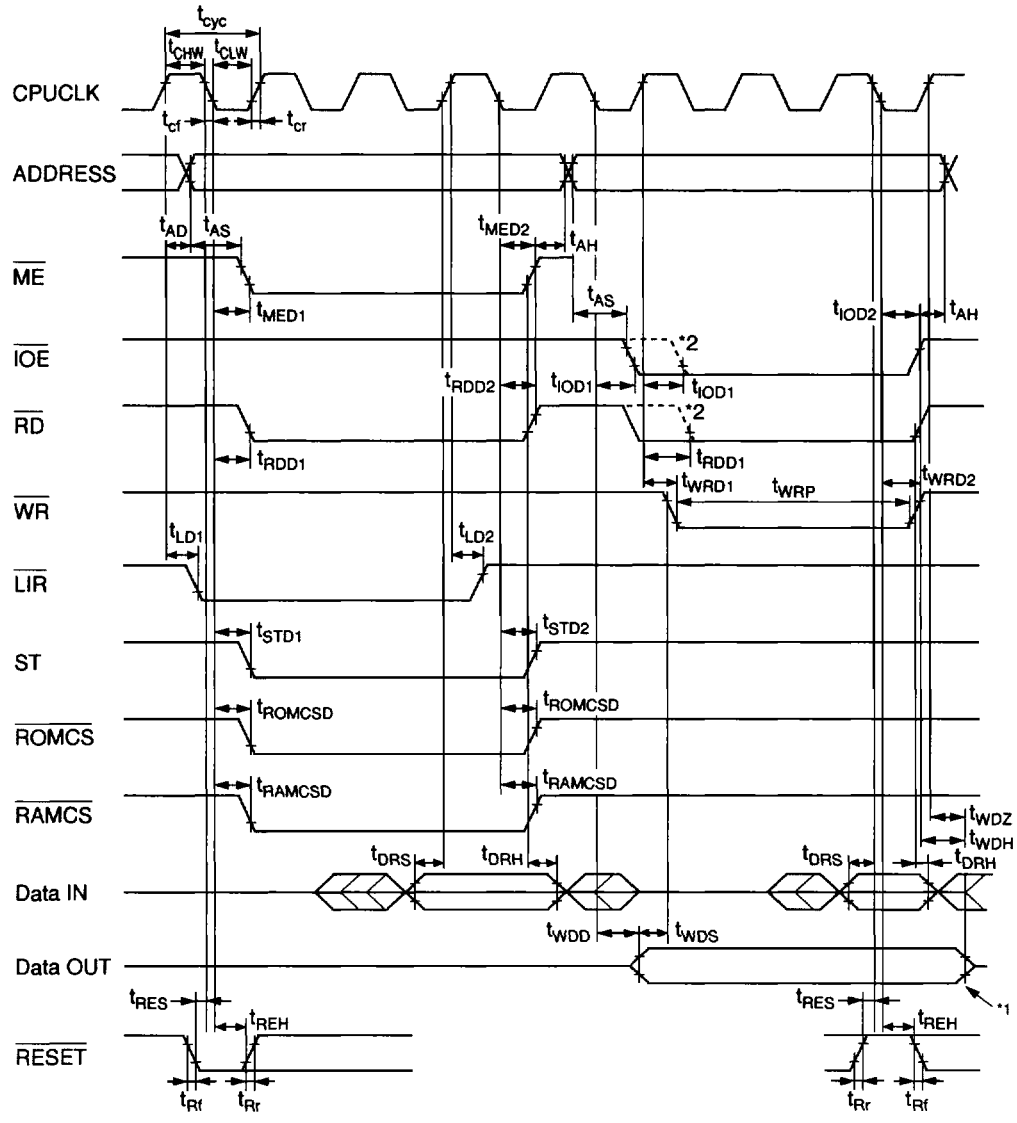
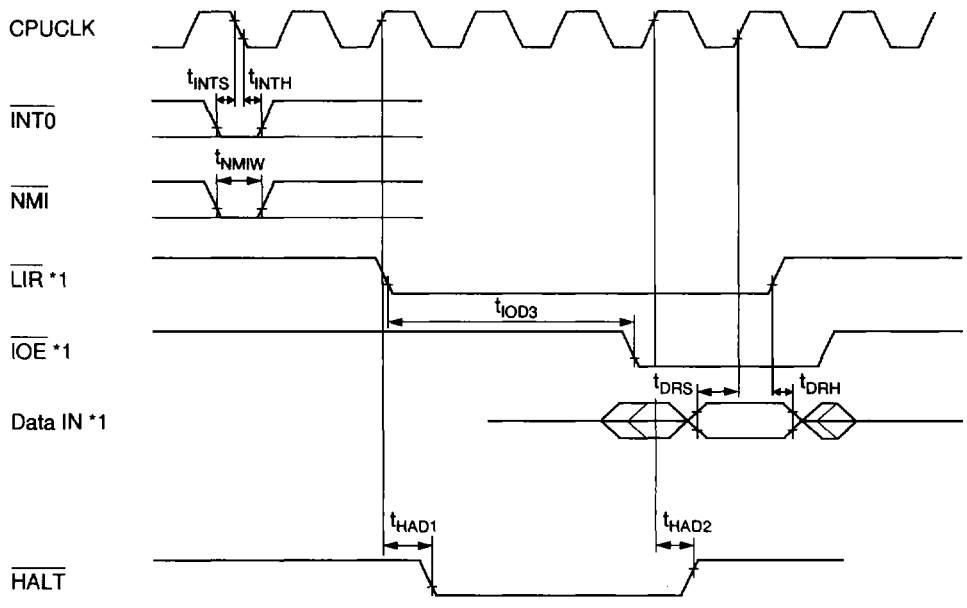


Figure 10 Rise/Fall Time of Inputs Except EXTAL, $\overline{\text{RESET}}$



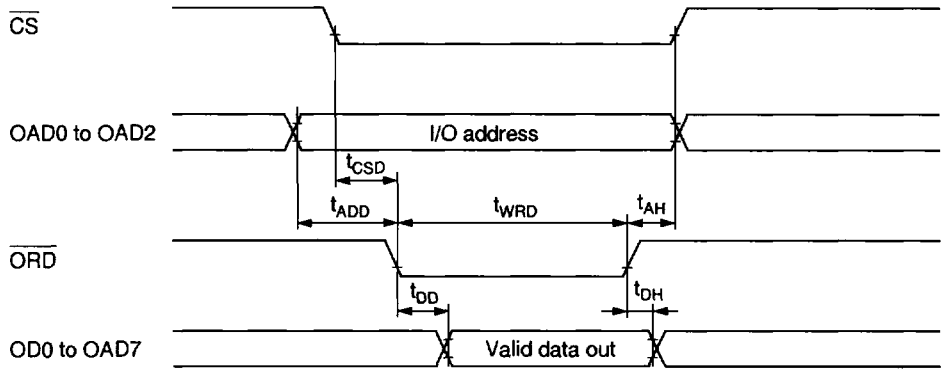
Notes: 1. At point of output buffer "OFF"
2. These specification are measured from CPUCLK falling edge at $\overline{IOC}$ = "1", otherwise from CPUCLK rising edge at $\overline{IOC}$ = "0" (Z80 compatible mode).

Figure 11 CPU Timing (1)

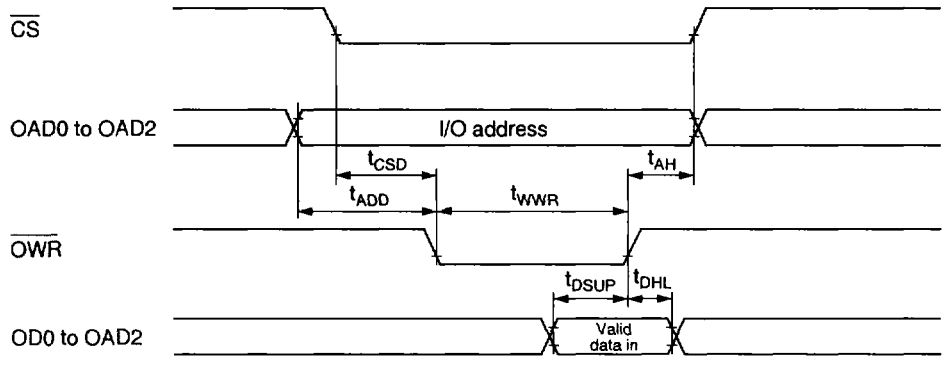


Note: 1. At point of $\overline{INT0}$ acknowledge cycle

Figure 12 CPU Timing (2)

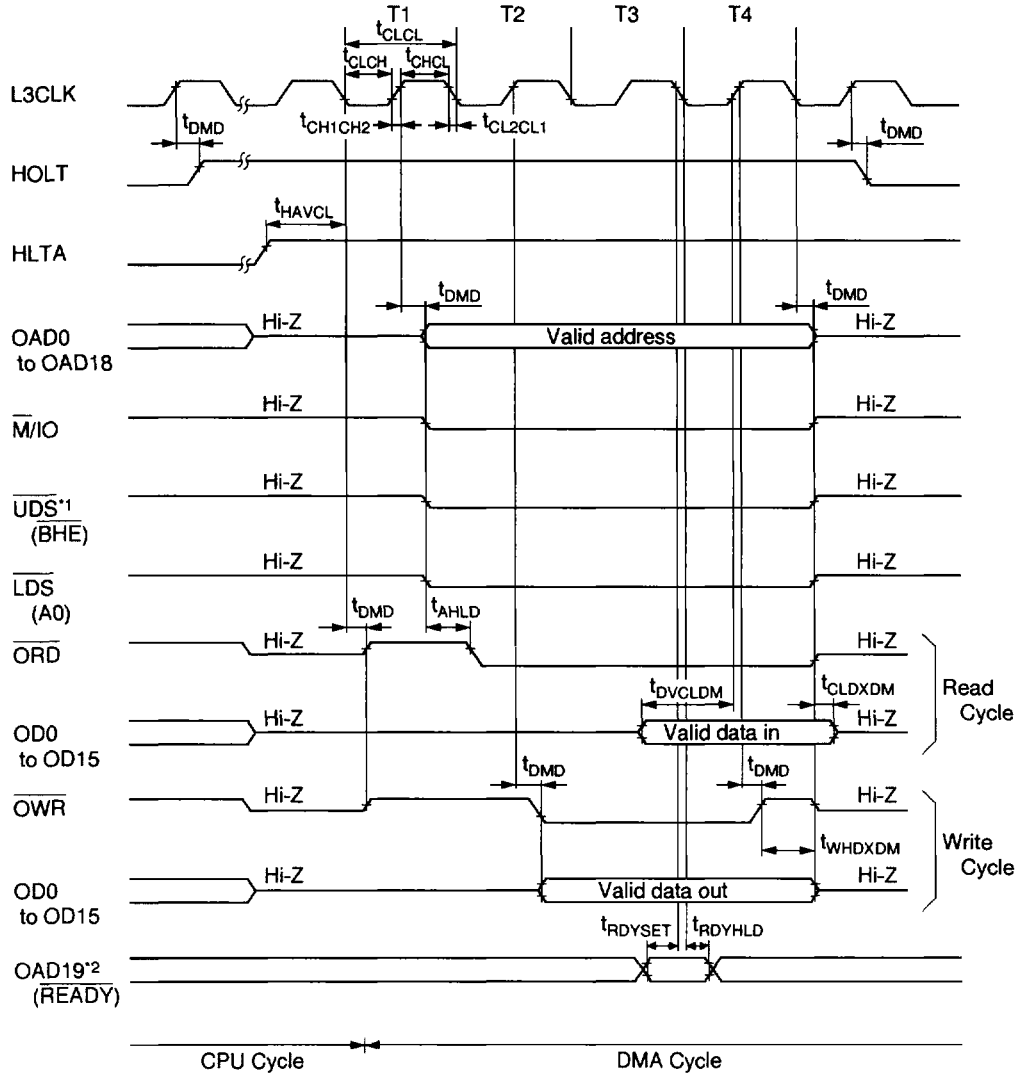


(1) Read Cycle



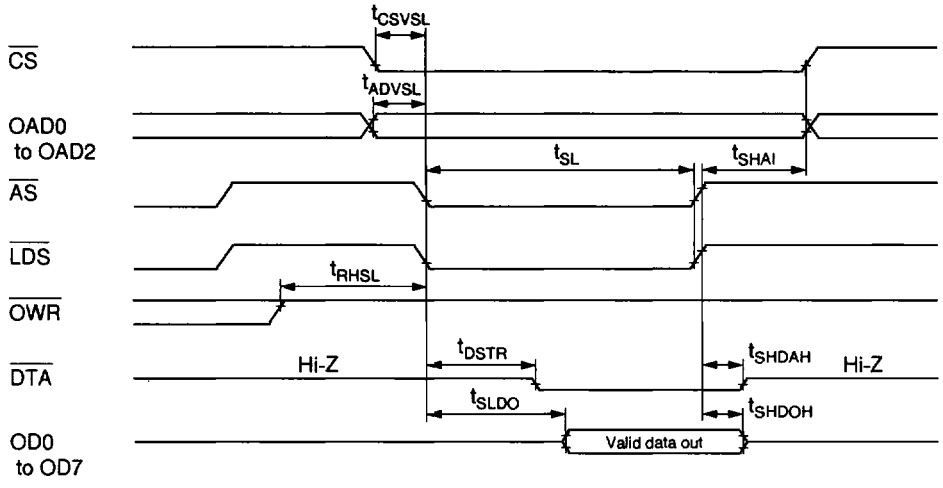
(2) Write Cycle

Figure 13 80 Type I/O Mode Timing

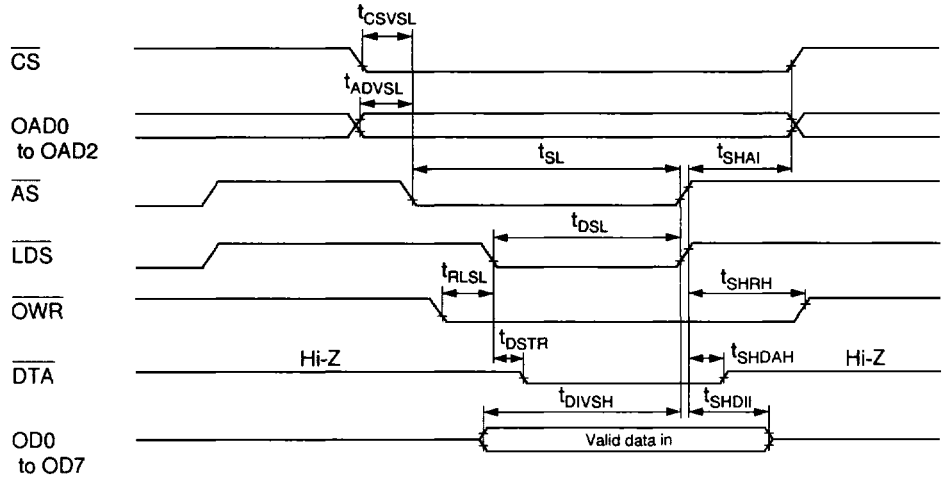


Notes: 1. At 16-bit data with mode (B/W = "0"). At 8-bit data with. This goes "HIGH" during DMA transfer.
2. OAD19 pin turns to $\overline{\text{READY}}$ input.

Figure 14 80 Type DMA Mode Timing

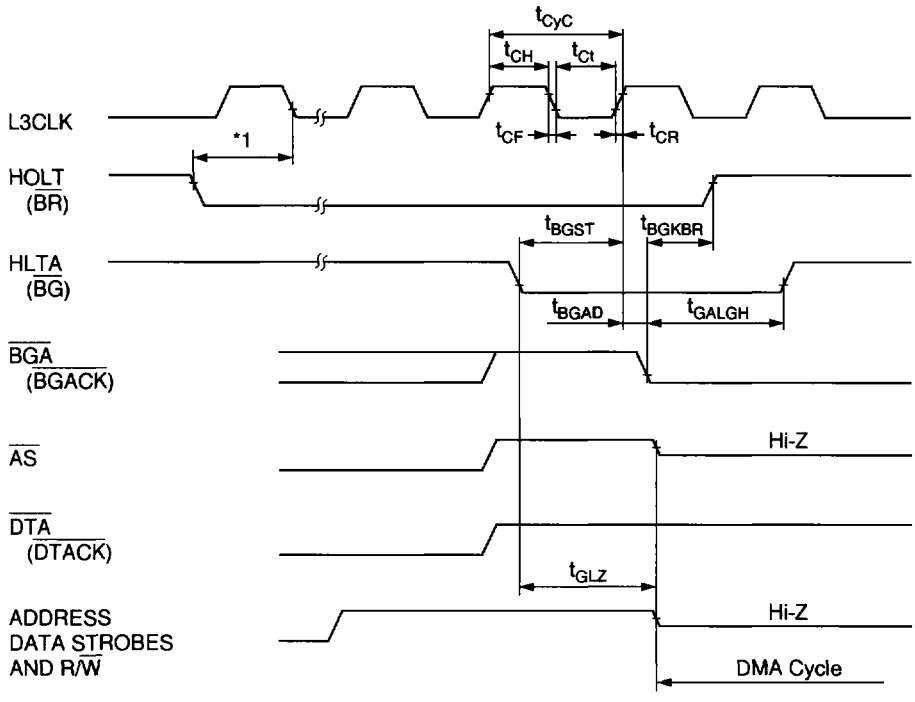


(1) Read Cycle



(2) Write Cycle

Figure 15 68000 Type I/O Mode Timing



Note: 1. HOLT isn't synchronized to L3CLK. If set-up time is insufficient for L3CLK rising edge, HOLT is fetched by upper CPU after 1 clock cycle.

Figure 16 68000 Type Bus Arbitoration

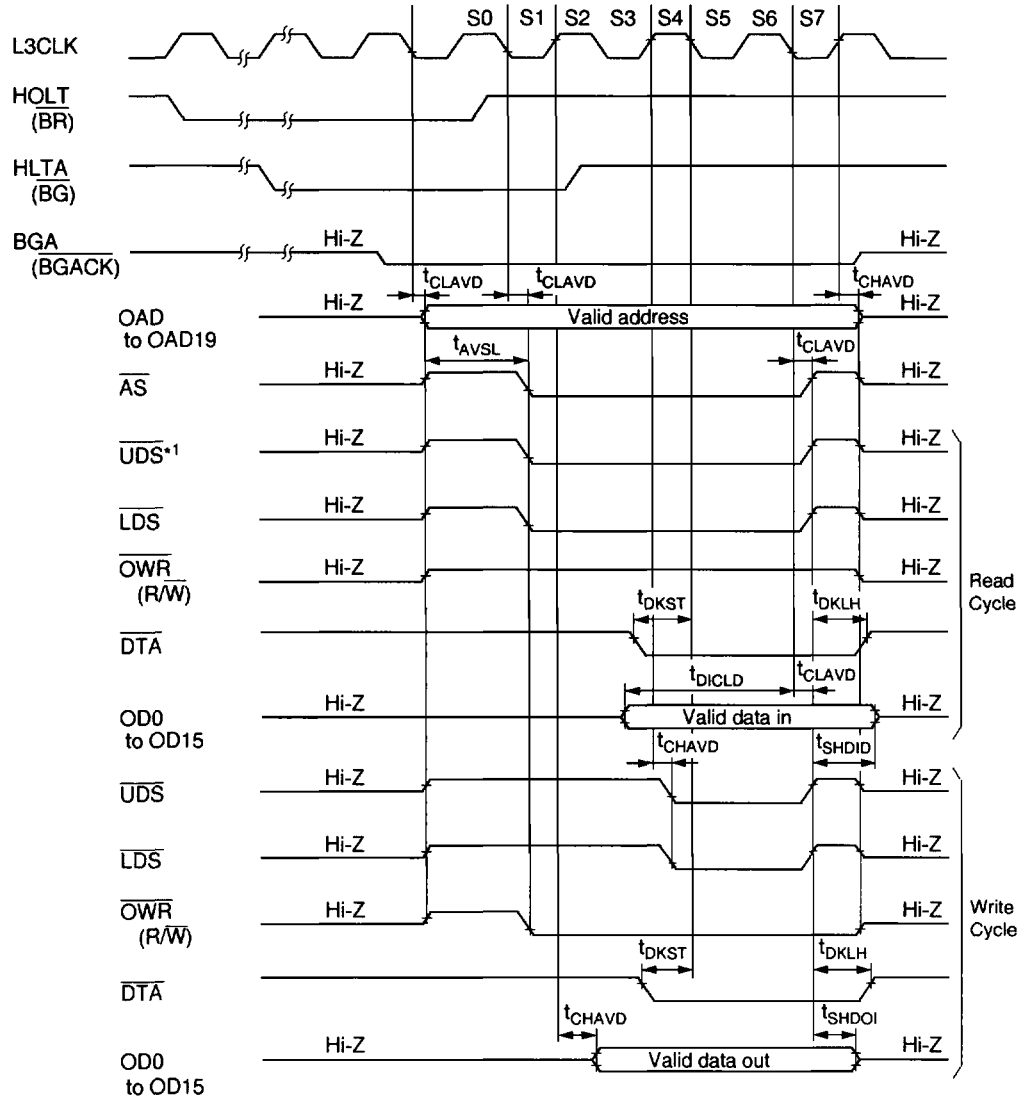
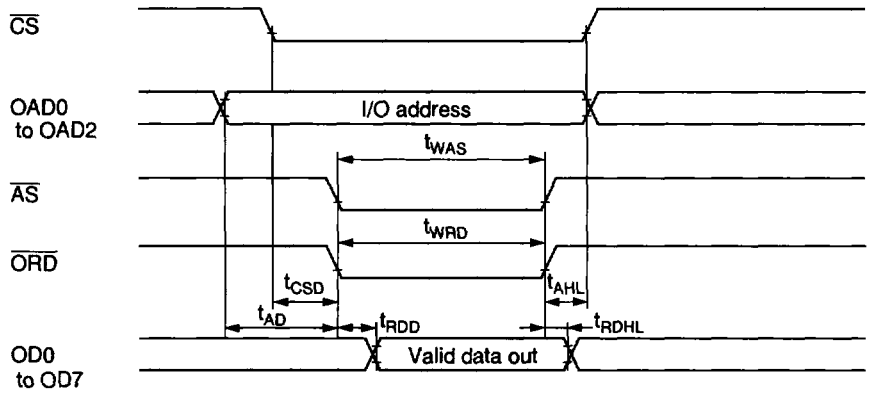
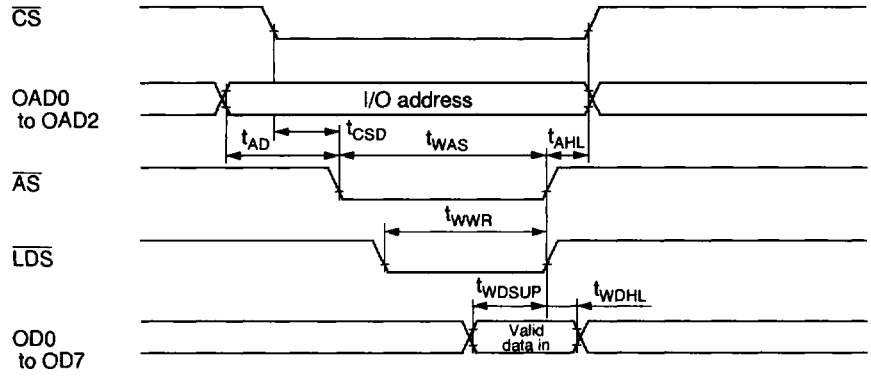


Figure 17 68000 Type DMA Mode Timing

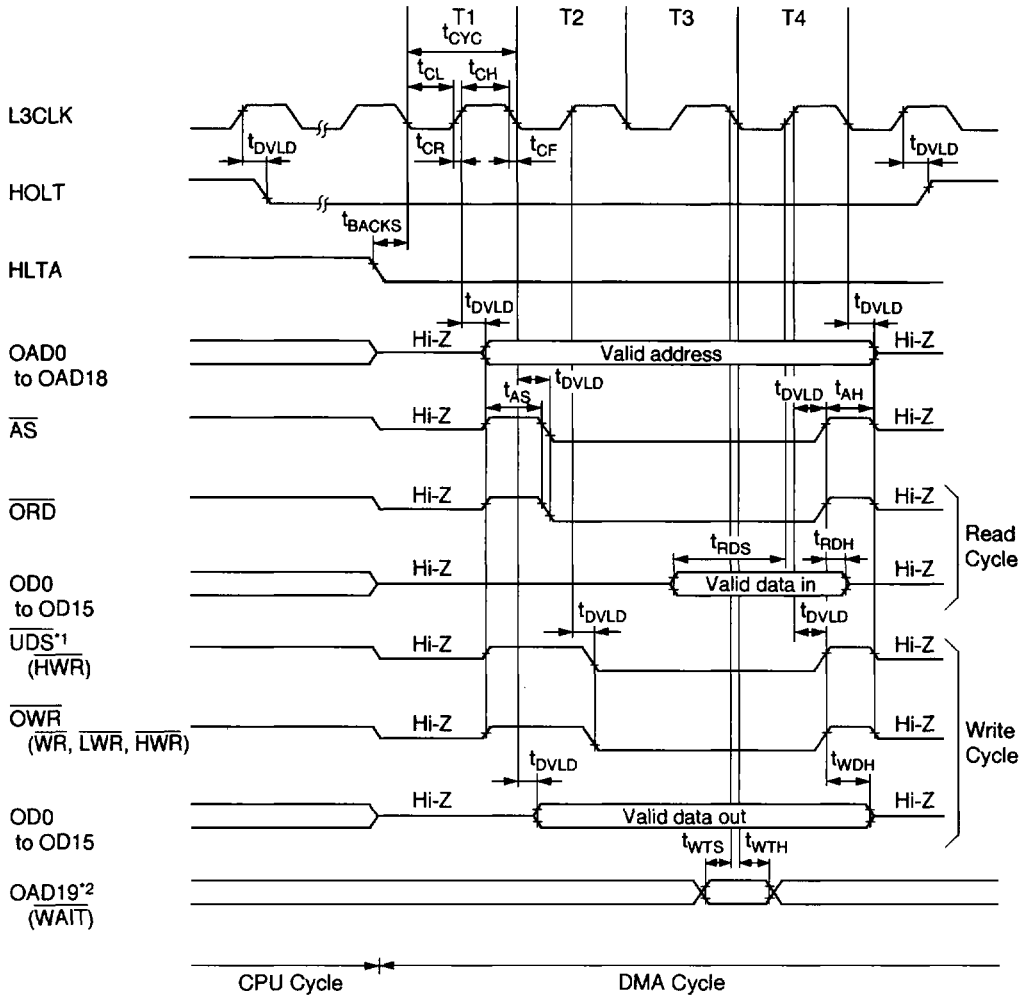


(1) Read Cycle



(2) Write Cycle

Figure 18 H8 Type I/O Mode Timing



Notes: 1. At 16-bit bus width mode (B/W = "0"). At 8-bit data width, this goes "HIGH" during DMA transfer.
2. OAD19 pin turns to $\overline{\text{WAIT}}$ input.

Figure 19 H8 Type DMA Mode Timing

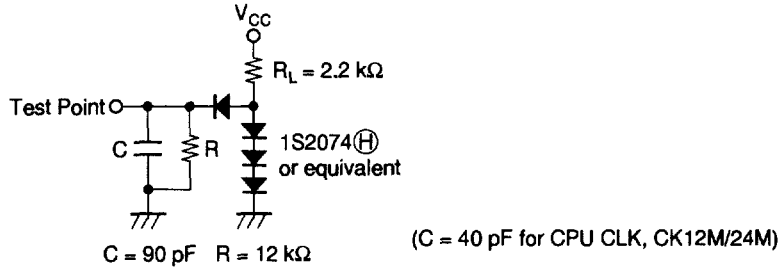


Figure 20 Bus Timing Test Loads (TTL Loads)

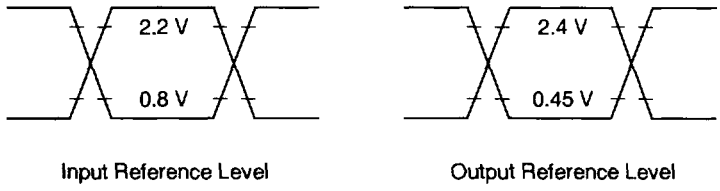
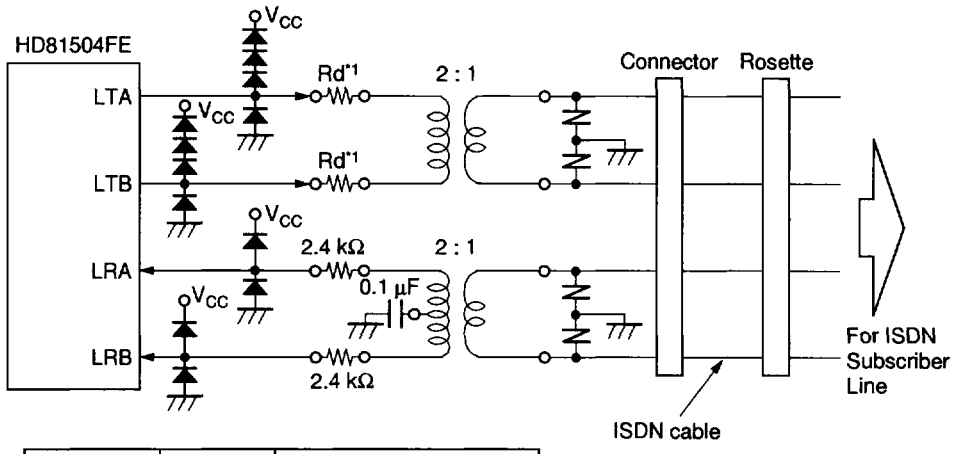


Figure 21 Reference Level

Example of System Glue Logic Diagram

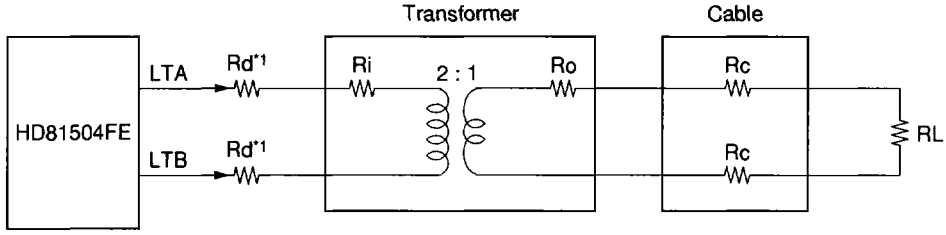


Transformer	Rd*1	Company
AI73HI	15 Ω	Hitachi Ferrite Co.
AI75HI	27 Ω	
AI77HI	12 Ω	
AI84HI	27 Ω	
93-137	22 Ω	Sanrittsu Co.

Note: 1. Rd should be different according to system configration. To define Rd, please reffer to the following formula with considerating glue logic.

$$Rd = \{90\Omega - (Ri + 4Ro + 8Rc)\}/2$$

Ri : Direct current resistance for transformer on LSI side
Rα Direct current resistance for transformer on line side
Rc: Direct current resistance for transformer of cable



Note: Please consider direct current resistance for common choke coil in case of inserting common chooke coil.