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SSI 32P4752/4756
Read Channel with 1,7 ENDEC, 4-burst Servo

January 1995

DESCRIPTION

The SSI 32P4752/4756 devices are high performance BiCMOS single chip read channel ICs that contain all the functions needed to implement a complete zoned recording read channel for hard disk drive systems. Functional blocks include the pulse detector, programmable filter, 4-burst servo capture, time base generator, and data separator with 1,7 RLL ENDEC. Data rates from 18 to 64 Mbit/s can be programmed using an internal DAC whose reference current is set by a single external resistor. For reduced clocking speeds, the 32P4752/4756 employs a dual-bit parallel interface to the controller.

Programmable functions of the SSI 32P4752/4756 devices are controlled through a bi-directional serial port and banks of internal registers. This allows zoned recording applications to be supported without changing external component values from zone to zone.

The SSI 32P4752/4756 utilize an advanced BiCMOS process technology along/ with advanced circuit design techniques which result in high performance devices with low power consumption.

The 32P4752 provides four servo bursts with A, B, C, and D outputs; the 32P4756 also provides four servo bursts with A-B, C-D, and A+B outputs.

FEATURES

GENERAL:

- **DAC controlled programmable data rates from 18 to 64 Mbit/s**
- **Complete zoned recording application support**
- **Low power operation < 600 mW typical at 5V**
- **Bi-directional serial port for register access**
- **Register programmable power management (sleep mode <0.5 mA)**
- **Power supply range (4.5 to 5.5V)**
- **Small footprint 64-lead TQFP package**

PULSE DETECTOR:

- **Fast attack/decay modes for rapid AGC recovery**
- **Dual rate charge pump for fast transient recovery**
- **Low Drift AGC hold circuitry**
- **Temperature compensated, exponential control AGC**
- **Wide bandwidth, high precision full-wave rectifier**

(continued)

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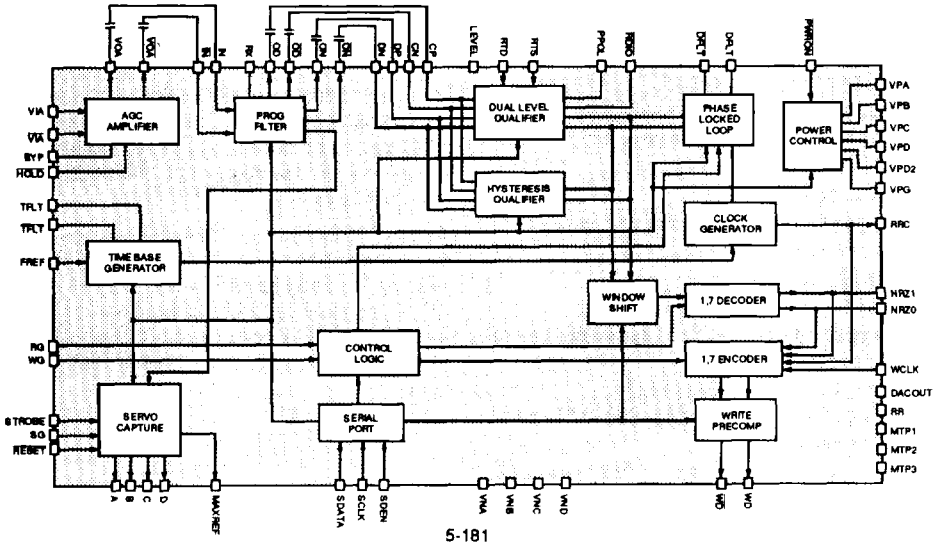
BLOCK DIAGRAM



SSI 32P4752/4756
Read Channel with
1,7 ENDEC, 4-burst Servo

FEATURES (continued)

PULSE DETECTOR: (continued)

- Dual mode pulse qualification circuitry (user selectable)
- CMOS $\overline{\text{RDIO}}$ signal output for servo timing support
- Internal LOW-Z and fast decay timing
- 0.6 ns max. pulse pairing at 64 Mbit/s using a 6 MHz sine wave input

SERVO CAPTURE:

- 4-burst servo capture with A, B, C, D outputs (32P4752)
- 4-burst servo capture with A-B, C-D and A+B outputs (32P4756)
- Internal hold capacitors
- Separate registers for fc and V_{TH} during servo mode
- 4-bit DAC for AGC level control (0.8 to 1.2 Vpp)

PROGRAMMABLE FILTER:

- Programmable cutoff frequency of 9 to 27 MHz
- Programmable group delay equalization with asymmetrical zero
- Programmable boost/equalization of 0 to 13 dB
- Matched normal and differentiated outputs
- ± 15% fc accuracy
- ± 2% maximum group delay variation to fc
- Less than 1.5% total harmonic distortion
- Low-Z input switch
- No external filter components required

TIME BASE GENERATOR:

- Better than 1% frequency resolution
- Up to 96 MHz frequency output
- Independent M and N divide-by registers
- VCO center frequency matched to data synchronizer VCO

DATA SEPARATOR:

- Fast acquisition phase lock loop with zero phase restart technique
- Dual-bit NRZ interface
- Integrated 1,7 RLL Encoder/Decoder
- Programmable decode window symmetry control via serial port
  - Window shift control 33% (4-bit)
  - Includes delayed read data and VCO clock monitor points
- Programmable early/late write precomp (3-Bits each)
- Differential PECL write data output
- Hard sector operation
- VCO and Synchronized Read Data test points

FUNCTIONAL DESCRIPTION

The SSI 32P4752/4756 implement a high performance complete read channel, including pulse detector, 4-burst servo capture, programmable active filter, time base generator, and data separator with 1,7 RLL ENDEC, at data rates up to 64 Mbit/s.

PULSE DETECTOR CIRCUIT DESCRIPTION

The pulse detector, in conjunction with the programmable filter, provides all the data processing functions necessary for detection and qualification of encoded read signals. The signal processing circuits include a wide band variable gain amplifier; a wide bandwidth, high precision fullwave rectifier; and a dual rate charge pump. The entire signal path is fully-differential to minimize external noise pick up.

AGC CIRCUIT

The gain of the AGC amplifier is controlled by the voltage (V_{BYP}) stored on the BYP hold capacitor (C_{BYP}), Figure 1. A dual rate charge pump drives C_{BYP} with currents that depend on the instantaneous differential voltage at the DP/DN pins. Attack currents lower V_{BYP} which reduces the amplifier gain, while decay currents increase V_{BYP} which increases the amplifier gain. When the signal at DP/DN is greater than 100% of the programmed AGC level, the nominal attack current of 0.17 mA is used to reduce the amplifier gain. If the signal is greater than 125% of the programmed AGC level, a fast attack current of eight (8) times nominal is used to reduce the gain. This dual rate approach allows AGC gain to be quickly decreased when it is too high yet minimizes distortion when the proper AGC level has been acquired.

A constant decay current of 4 µA increases the amplifier gain when the signal at DP/DN is less than the programmed AGC level. The large ratio (0.17 mA:4 µA) of the nominal attack and nominal decay currents enables the AGC loop to respond to the peak amplitudes of the incoming read signal rather than the average value.

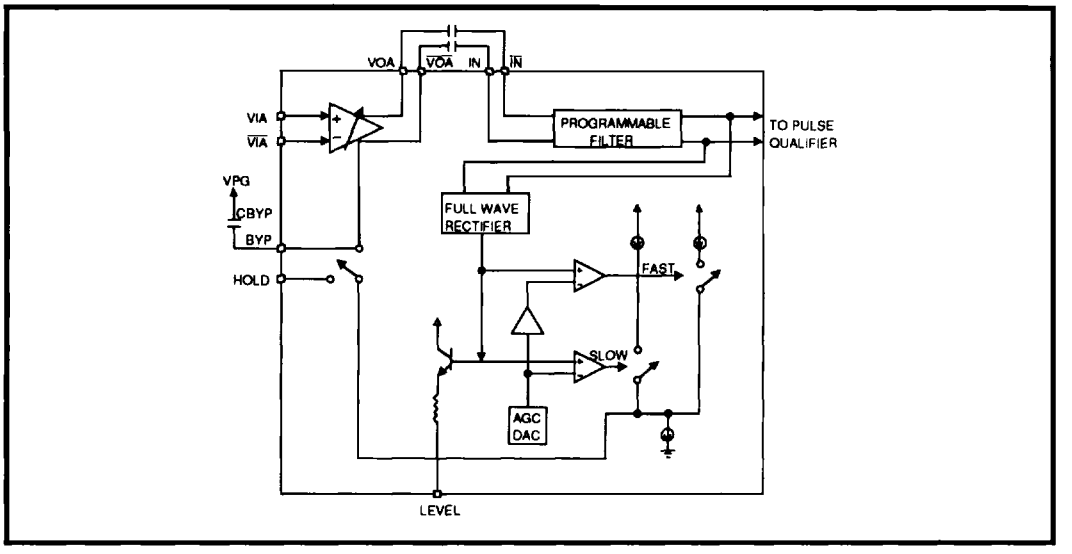


FIGURE 1: AGC Block

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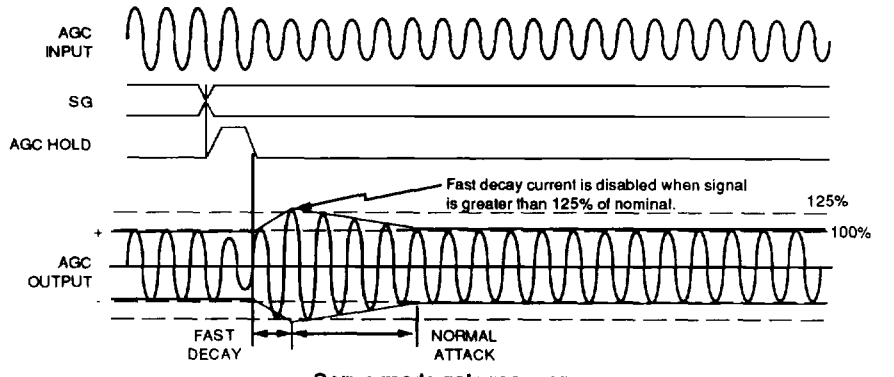
AGC MODE CONTROL

When write gate (WG) is driven high, the dual rate charge pump is disabled causing the AGC amplifier gain to be held constant. The input impedance of both the AGC amplifier and the programmable filter is reduced. When the WG pin transitions from high to low, the Low-Z mode is activated. In this mode, the input impedance at both the AGC amplifier and the programmable filter remain low to allow for quick recovery of the AC coupling capacitors. Directly following the Low-Z mode is the fast decay mode which allows rapid acquisition of the proper AGC level. In fast decay mode, an internal FET is switched on to drive a high current into the BYP pin. The current remains active until the signal at DP/DN is above 125% of the nominal amplitude, or until an internal timer expires. After the fast decay current is disabled, the normal AGC sequence is enabled. The duration of both the Low-Z and fast Decay modes can be set to either 1 µs or 2 µs by programming bit D7 in the write precomp register. A fast decay sequence is also initiated on the edges of servo gate (SG). Each edge of SG triggers a 400 ns (typ.) AGC hold period to allow the filter to settle. The fast decay current is enabled at the end of the HOLD period. When the pulse detector is powered-down, V_{BYP} will be held constant subject to leakage currents only. Upon power-up, the Low-Z/fast decay sequence is executed to rapidly recover from any transients or drift which may have occurred on the BYP hold capacitor, Figure 2.

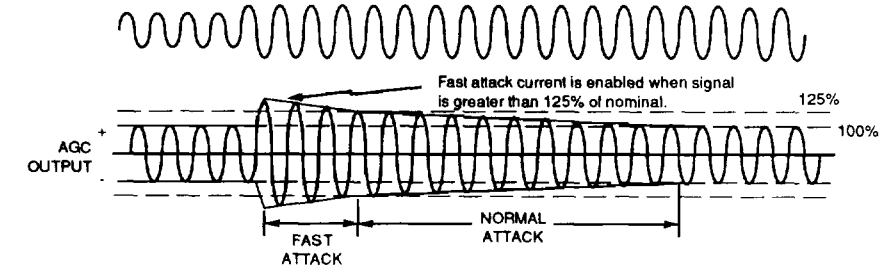
External control for enabling the dual rate charge pump is also provided. Driving the $\overline{HOLD}$ pin low forces the dual rate charge pump output current to zero. In this mode, V_{BYP} will be held constant subject only to leakage currents.

$\overline{RDIO}$ Output Pin

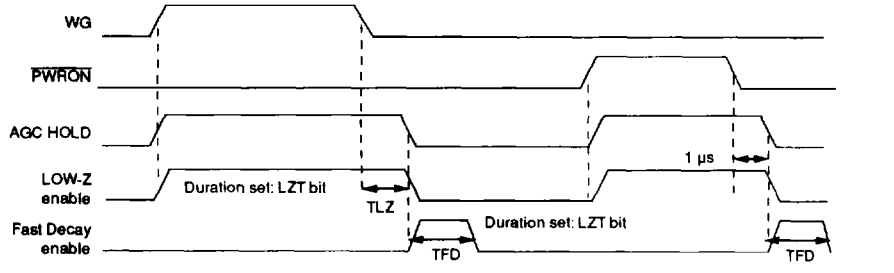
A TTL compatible inverted Read Data I/O ($\overline{RDIO}$) is provided to monitor the pulse detector output. This pin will be held high when SG is low and either RG or WG are high to reduce noise and accompanying jitter during read or write modes. Its falling edge indicates the occurrence of valid data pulse.



Servo mode gain recovery



High gain to low gain recovery



Low-Z timing

FIGURE 2: AGC Timing Diagrams

FUNCTIONAL DESCRIPTION (continued)

QUALIFIER SELECTION

The 32P4752/4756 provide both hysteresis and dual comparator pulse qualification circuits that may be independently selected for read mode and servo mode operation, Figure 3. For read mode operation the pulse qualifier method is selected by setting the MSB in the data threshold control register (DTCR). The lower 7 bits of the DTCR also set the hysteresis level of the comparators for read mode. For servo mode operation the pulse qualifier method is selected by setting the MSB in the servo threshold control register (STCR). The lower 7 bits of the STCR set the hysteresis level of the comparators for servo mode:

Qualification threshold% =
(84.5 x VTHDAC/127) - 2.17% (48 ≤ VTHDAC ≤ 127)

where
VTHDAC = DTCR or STCR value

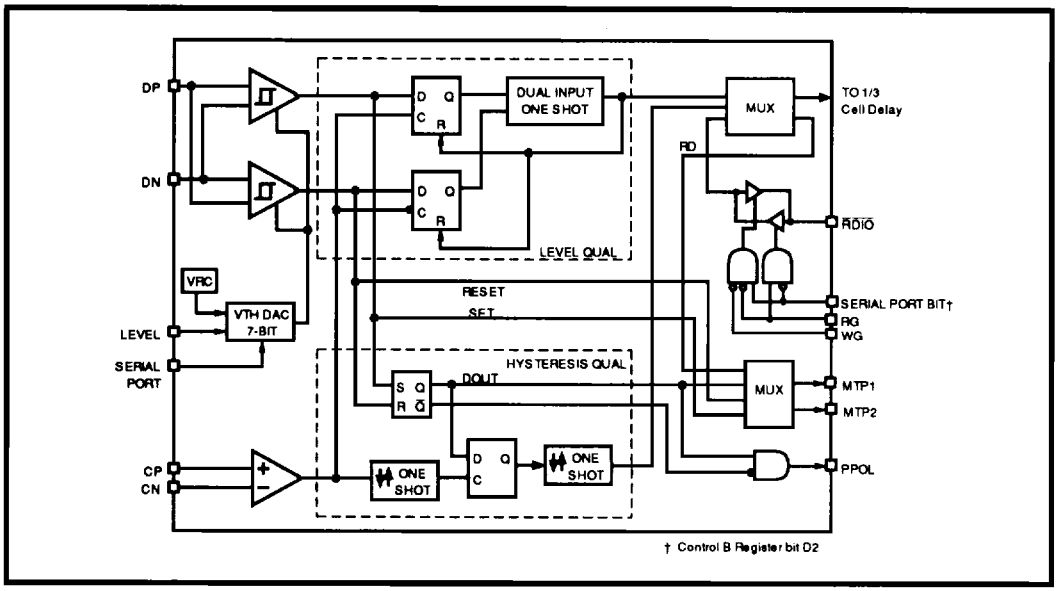


FIGURE 3: Pulse Qualification

FUNCTIONAL DESCRIPTION (continued)

HYSTERESIS COMPARATOR QUALIFICATION

When the Hysteresis Qualification mode is selected, the same threshold qualification comparators and clock comparators are used to implement a polarity checking rule. In this mode, a positive peak that clears the established threshold level will set the SR Flip-Flop and trigger the bidirectional one-shot that creates the read data pulses. In order to get another pulse clocked out, a peak of the opposite polarity must clear the negative threshold level to reset the SR Flip Flop and trigger the bidirectional one-shot, Figure 5.

DUAL COMPARATOR QUALIFICATION

When in Dual Comparator mode, independent positive and negative threshold qualification comparators are used to suppress the error propagation of a positive and negative threshold comparator. However a slight amount of hysteresis is included to increase the comparator output time when a signal that just exceeds the threshold level is detected. This eases the timing with respect to the zero crossing clock comparator. A differential comparator with programmable threshold allows differential signal qualification for noise rejection. The programmable threshold, V_{TH}, is driven by a multiplying DAC which is driven by the LEVEL voltage and referenced to VRC (VRC is the internal bandgap reference). Thresholds from 30 to 80% may be set with a resolution of better than 1%. A parallel R-C network of RTD and CT sets the threshold time constant when not in the servo mode. A qualified signal zero crossing at the CP-CN inputs triggers the output one shot, Figure 4.

SERVO DEMODULATOR CIRCUIT DESCRIPTION

The 32P4752 servo sections capture four separate servo bursts and provide A, B, C, and D burst outputs, Figure 6(a); the 32P4756 provide A+B, A-B and C-D outputs , Figure 6(b). Internal burst hold capacitors are provided to support low leakage burst capture and reduce external component count. To support embedded servo applications, the 32P4752/4756 provide additional programming registers that set the filter cutoff frequency (fc) and the hysteresis threshold level (V_{TH}) for servo mode. When SG is activated or deactivated there is a nominal 0.3 µs settling time for the internal DACs to recover from the register switching.

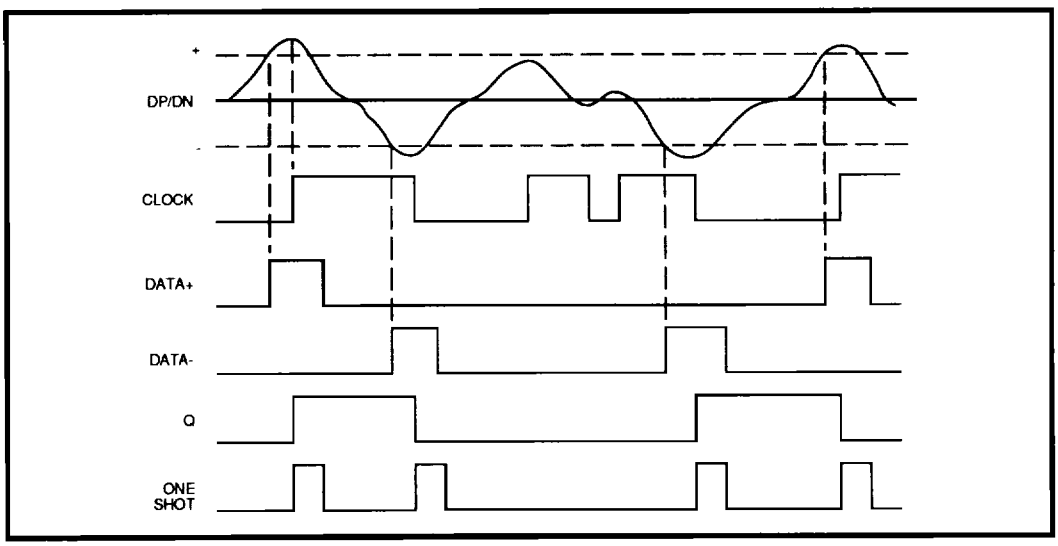


FIGURE 4: Dual Comparator Timing Diagram (Refer to Figure 3: Level Qualification Section)

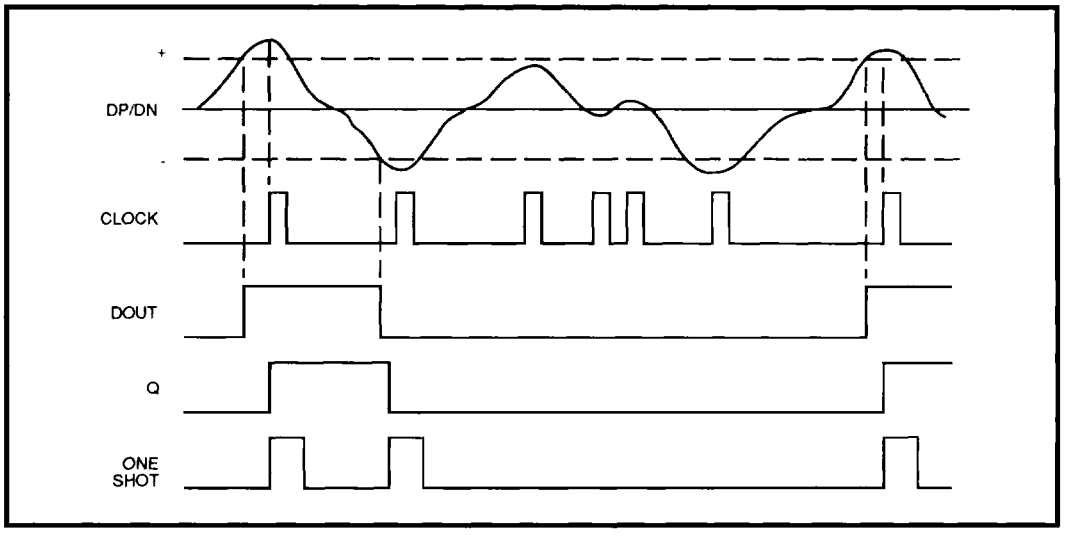


FIGURE 5: Hysteresis Comparator Timing Diagram

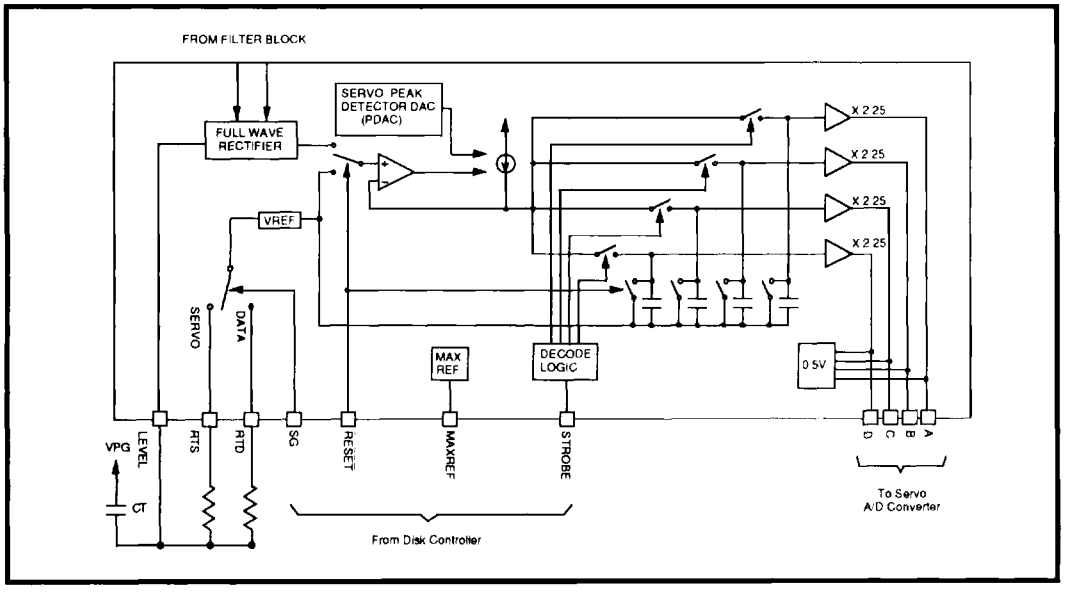


FIGURE 6(a): 32P4752 Servo Capture

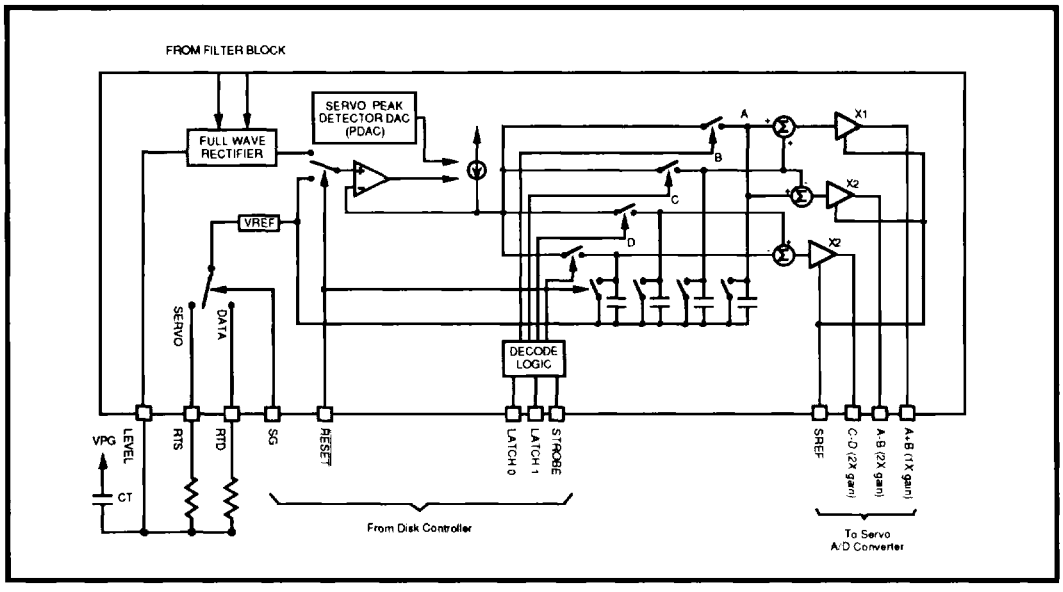


FIGURE 6(b): 32P4756 Servo Capture

FUNCTIONAL DESCRIPTION (continued)

SERVO MODE OPERATION

When the servo gate (SG) is asserted, the control DACs for *fc* and VTH switch from the data mode registers to the servo mode registers and the AGC goes into the HOLD/fast decay mode. In addition, filter boost is disabled (as determined by the boost control bit), the AGC level is adjusted according to the AGC Level DAC and the RTS servo time constant setting resistor is connected to VRC (VRC is the internal bandgap reference.) By disabling the boost and providing the servo control register for *fc* the servo signal to noise ratio can be greatly improved. When SG is activated or deactivated there is a nominal 0.3 µs settling time for the internal DACs to recover from the register switching. During servo mode, the AGC circuit remains active. A 4-bit DAC (DACA) is used to set the AGC level over a range of 0.80 to 1.20 Vp-p as follows:

VAGC = 1.2 - (DACA • 0.02668) Vp-p
where DACA is the value of the AGC Level register

Typically, a servo preamble is used to achieve the desired AGC level and then the $\overline{\text{HOLD}}$ pin is asserted to hold the AGC gain. When SG goes low to terminate the servo mode, the AGC goes into the HOLD (0.4 µs)/ fast decay (1 µs) mode to allow for fast transition into the read or write mode.

BURST CAPTURE

For 32P4752, burst capture is controlled by a single external pin designated STROBE and an internal counter. When SG is active, the first pulse on the STROBE pin gates the output of the servo peak detector to the A burst hold capacitor. The capacitor charges for as long as the STROBE pulse is high. On the falling edge of the STROBE signal, the internal counter is incremented. The next STROBE pulse will then gate the servo peak detector output to the B burst hold capacitor. Again, the capacitor charges for as long as the STROBE pulse is high. On the falling edge of STROBE, the counter is incremented again and the C burst is captured on the next STROBE pulse. On the

next falling edge of STROBE, the counter is incremented again and the D burst is captured on the next STROBE pulse. After the falling edge of the fourth STROBE pulse, the counter is reset to zero and the burst capture process can be repeated. See Figure 7(a) for timing information. The internal counter is also reset when the SG pin is deactivated. The voltage level on each hold capacitor is then provided to buffer amplifiers which generate the servo output signals. A 1 Vp-p differential voltage at the DP/DN pins will result in a 2.15V peak burst amplitude. The servo output signals (A, B, C, D) are referenced above an internal baseline of 0.5V. The output voltage at the MAXREF pin is a nominal 3.1V, and represents the maximum voltage to which the servo signal outputs will swing. It is typically used as the reference voltage for an external A/D converter. MAXREF is internally reduced to a 0.5 volt level, and establishes the servo zero-signal baseline.

For 32P4756, four servo control inputs; LATCH0, LATCH1, STROBE, and $\overline{\text{RESET}}$, control the servo peak sample and hold functions. LATCH0 and LATCH1 are decoded to select one of the four internal burst hold capacitors. Driving the STROBE pin high gates the output of the servo peak detector to the selected internal burst hold capacitor. Reference Figure 7(b) for servo timing information. The voltage level on each hold capacitor is then provided to summing amplifiers which generate the servo output signals. A 1V differential voltage at the DP/DN pins will result in a 2V peak burst amplitude at the A-B and C-D pins, but only 1V at the A+B pin. An input voltage applied to the SREF pin will establish the DC reference voltage for the servo outputs. When A-B = 0, then A-B output will be a SREF.

All four internal burst hold capacitors are discharged when the $\overline{\text{RESET}}$ pin is driven low. The $\overline{\text{RESET}}$ control input overrides the STROBE signals. The 32P4752 has high-resolution, bi-directional current reset in which the capacitor baseline voltage will be equal to the zero-signal baseline voltage.

The drive current of the servo peak detector charge pump is set by a 4-bit word (DACP) addressed through the serial port. The LSB value is 6 µA, and the offset is 1 LSB such that "0000" corresponds to 6 µA and "1111" results in 96 µA. Maximum noise immunity is obtained in the servo peak detector by choosing the smallest value of charge current to charge the internal 10 pF hold capacitor during the burst acquisition time, see Figure 8.

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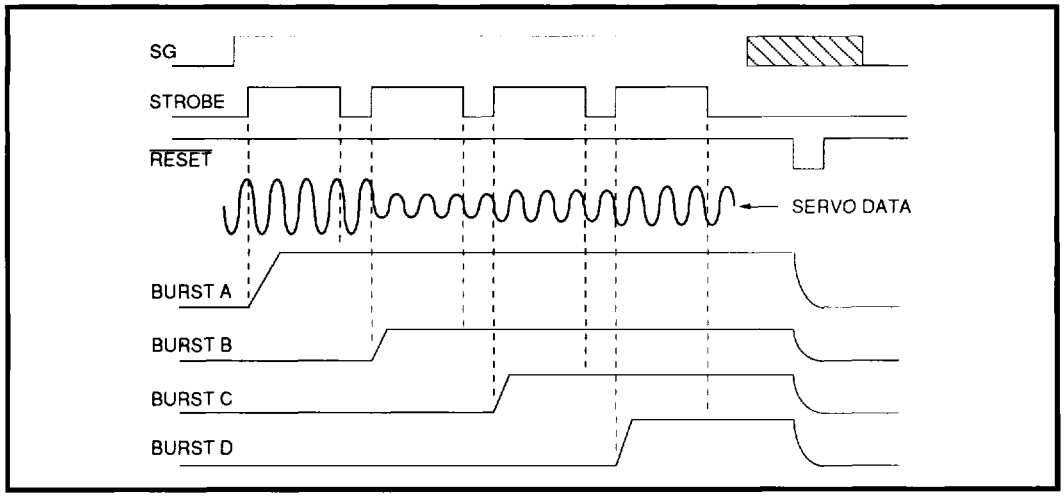

FIGURE 7(a): 32P4752 Servo Capture Timing Diagram

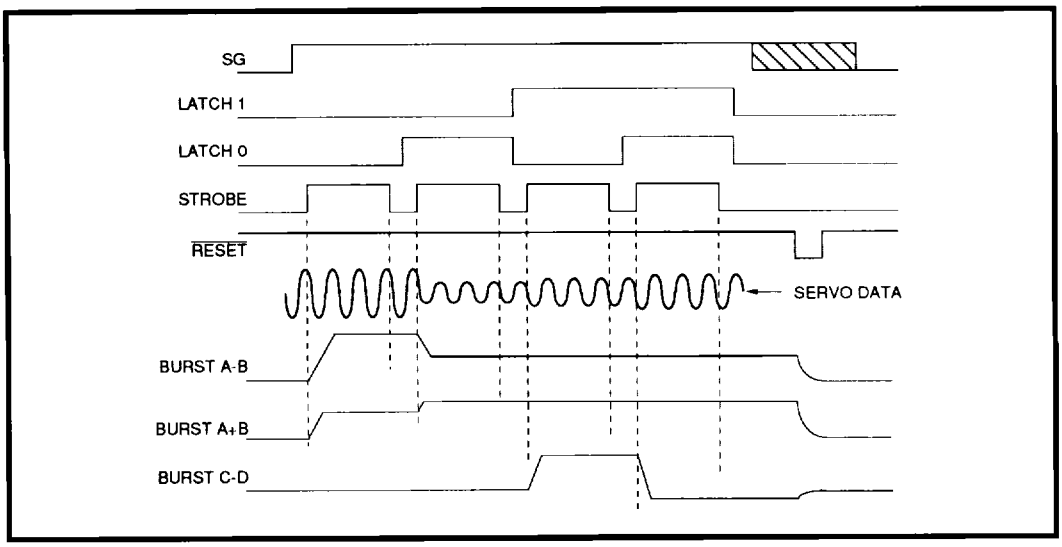

FIGURE 7(b): 32P4756 Servo Capture Timing Diagram

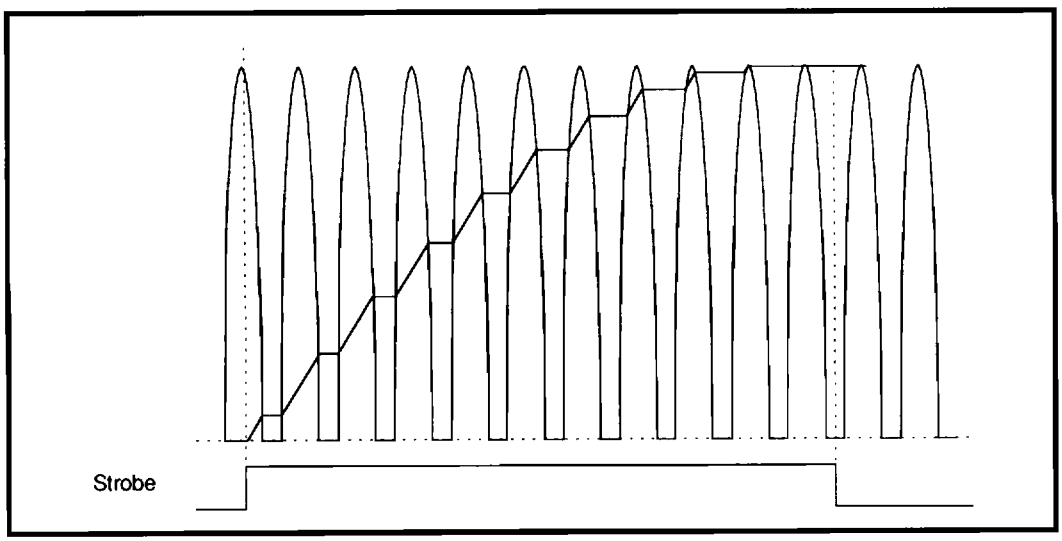

FIGURE 8: Servo Burst Aquisition (SG = $\overline{\text{RESET}}$ = 1)

BURST CAPTURE (continued)

Table 1 shows the recommended IDAC settings as a function of the strobe command duration to achieve acquisition to 99.5% of intended final value. These values are calculated with Fservo = 6.66 MHz at DP/DN.

TABLE 1: IDAC Settings vs Strobe Time

PDAC Word:	0000	00001	0010	0011	0100	0101	0110	0111	1000
Strobe Time (µs):	6.8	4.8	3.4	2.1	1.5	1.2	0.83	0.77	0.74
PDAC Word:	1001	1010	1011	1100	1101	1110	1111		
Strobe Time (µs):	0.71	0.68	0.66	0.64	0.63	0.62	0.61		

The transfer characteristic of the servo demodulator is shown in Figure 9. The peak detector exhibits constant gain for inputs at DP/DN from 0.2 to 1.2 Vp-p with small non-linearities below 0.2V.

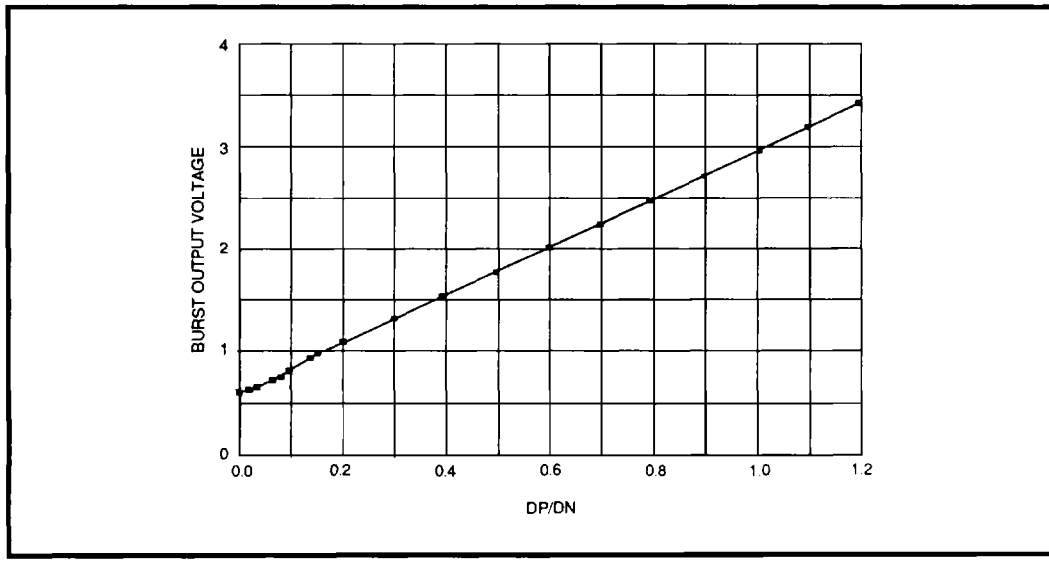

FIGURE 9: Servo Demodulator Transfer Curve

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FUNCTIONAL DESCRIPTION (continued)

TIMING OUTPUTS

To support servo timing recovery, the pulse detector section provides a TTL output of the servo information via the $\overline{RDIO}$ pin. A negative pulse is generated for each servo peak that is qualified through the pulse detector circuitry. Additional servo timing information is supported by the PPOL output. The PPOL pin provides pulse polarity information for the qualified peaks, where a high level TTL output indicates a positive pulse. To reduce noise progagation, $\overline{RDIO}$ will be held high and PPOL will be held low when SG is low and either RG or WG are high.

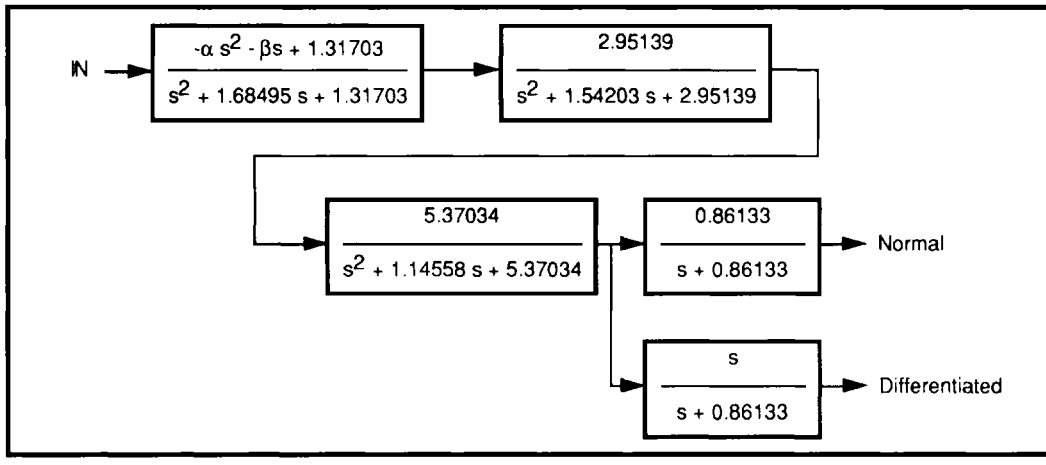
PROGRAMMABLE FILTER CIRCUIT DESCRIPTION

The SSI 32P4752/4756 include a programmable filter which consists of a normal output and a separate time-differentiated output. The normal low-pass output is of a seven-pole two-real-zero type. With a zero placed at the origin, the filter also provides the time-differentiated output to be used in time qualification of the data qualifier circuit. To ease the timing requirement in peak detection of signals slightly above the qualification threshold, the time-differentiated output is purposely delayed by 1.2 ns relative to the normal output. The normalized transfer functions are:

While the cutoff frequency is scaled by replacing s with $s/2\pi fc$, the boost and group delay equalization are controlled by varying the values of a and b. Both outputs have matched group delays (<1 ns typical.) The group delay matching is unaffected by any amount of programmed equalization or bandwidth. Programmable bandwidth and boost/equalization are provided by internal 7-bit control DACs. The programmable characteristics are automatically switched during servo mode to improve signal to noise ratio. Differentiation pulse slimming equalization which does not affect the filter's group delay response, is accomplished by a two-pole low-pass with a two-pole high-pass feed forward section to provide complimentary real axis zeros. A variable attenuator is used to program the zero locations. The filter implements a 0.05 degree equiripple linear phase response.

FILTER OPERATION

AC coupled differential signals from the AGC amplifier are applied to the IN/$\overline{IN}$ inputs of the filter. To improve settling time of the coupling capacitors, the IN/$\overline{IN}$ inputs are placed into a Low-Z state for 1 µs when WG goes inactive or when the $\overline{PWRON}$ pin is brought low. The programmable bandwidth and boost/equalization features are controlled by internal DACs and the registers programmed through the serial port. The current



reference for both DACs is set using a single external resistor connected from pin RX to ground. The voltage at pin RX is proportional to absolute temperature (PTAT), hence the current for the DACs is a PTAT reference current. A 1000 pF capacitor should be connected in parallel with RX to reduce harmonic distortion.

BANDWIDTH CONTROL

The programmable bandwidth is set by the filter cutoff DAC. This DAC has two separate 7-bit registers that can program the DAC value as follows:

$fc = Fc = 0.2223 \times DACF - 1.2348 \quad (46 \leq DACF \leq 127)$

where DACF = DMCR or SMCR value

In the data mode, the Data Mode Cutoff Register (DMCR) is used to determine the filter's unboosted 3 dB cutoff frequency fc. This is the -3 dB frequently with both α and β equal to 0. In the servo mode, the Servo Mode Cutoff Register (SMCR) is used. Switching of the registers is controlled by the servo gate (SG) pin. The filter cutoff set by the internal DAC is the unboosted 3 dB frequency. When boost/equalization is added, the actual -3 dB point will move out. The ratio of the actual -3 dB cutoff frequency to the programmed cutoff frequency as a function of alpha boost and group delay variation Δ% is tabulated in Table 2.

BOOST/EQUALIZATION CONTROL

Boost is defined as the amount of peaking in the magnitude response at the cutoff frequency due to $\alpha \neq 0$ and/ or $\beta \neq 0$.

Alpha boost ($\alpha \neq 0$, $\beta = 0$) does not affect the filter's group delay response. In general, the actual boost with group delay equalization is higher than the alpha boost. However, with alpha boost > 3 dB the difference is minimal. The 7-bit Filter Boost Control Register (FBCR) determines the amount of alpha boost that will be added to the -3 dB cutoff frequency, as follows:

Alpha Boost =

$20 \log [(0.025 \cdot FBCR + 0.000039 \cdot FBCR \cdot DACF) + 1] dB \quad (0 \leq DACS \leq 127)$

where DACF is the filter cutoff register

For example, with the DAC set for maximum output (FBCR = 7F or 127) there will be 13 dB of boost added at the unboosted -3 dB frequency. This will result in +10 dB of signal boost above the 0 dB baseline. When SG is active the boost can be disabled by setting bit 7 in FBCR. When bit 7 is "0" and SG is active the boost will automatically be set to 0 dB. If bit 7 is "1" the boost will remain at its programmed value regardless of the state of SG.

By applying group delay equalization ($\alpha = 0$, $\beta \neq 0$) the group delay response of the filter can be altered. The group delay Δ% is defined as the percentage change in absolute group delay value at DC with respect to that without the equalization applied ($\beta \neq 0$). The group delay Δ% at low frequencies can be programmed between -30% and +30% by the 8-bit Filter Group Delay Control Register (FGCR), with the MSB acting as a sign bit, as follows:

Group Delay $\Delta\% = -0.2362 \cdot DACG \cdot 100\%$
$(0 \leq DACG \leq 127)$, or

Group Delay $\Delta\% = 0.2362 \cdot (DACG - 128) \cdot 100\%$
$(128 \leq DACG \leq 255)$

Where DACG is the FGCR value

When SG is active the beta boost is controlled by setting bit 7 in SMCR. When bit 7 is "0" and SG is active the beta boost will automatically be set to 0 dB. It bit 7 is "1" the beta boost will remain at its programmed value regardless of the state of S.

When both $\alpha \neq 0$, $\beta \neq 0$, the total amount of boost is largely dominated by the alpha only, particularly when alpha boost is ≥ 3 dB. Table 3 lists the actual boost as a function of the applied alpha boost and group delay equalization.

TABLE 2: Ratio of Actual -3 dB Bandwidth to Cutoff Frequency

ALPHA BOOST	Group Delay Δ%						
	±30%	±25%	±20%	±15%	±10%	±5%	0.00
0 DB	1.58	1.45	1.30	1.17	1.07	1.02	1.00
1	1.67	1.57	1.47	1.36	1.27	1.21	1.19
2	1.78	1.71	1.64	1.56	1.50	1.46	1.44
3	1.90	1.85	1.80	1.76	1.72	1.70	1.69
4	2.01	1.98	1.96	1.93	1.91	1.90	1.90
5	2.13	2.11	2.09	2.08	2.07	2.06	2.06
6	2.23	2.22	2.21	2.20	2.20	2.20	2.20
7	2.33	2.32	2.32	2.31	2.31	2.31	2.31
8	2.42	2.41	2.41	2.41	2.41	2.40	2.40
9	2.50	2.50	2.50	2.49	2.49	2.49	2.49
10	2.58	2.58	2.58	2.58	2.57	2.57	2.57
11	2.66	2.65	2.65	2.65	2.65	2.65	2.65
12	2.73	2.73	2.73	2.73	2.73	2.73	2.73
13	2.80	2.80	2.80	2.80	2.80	2.80	2.80

TABLE 3: Actual Boost vs Alpha Boost & Group Delay Change

ALPHA BOOST	Group Delay Δ%						
	±30%	±25%	±20%	±15%	±10%	±5%	0.00
0 DB	2.92	2.21	1.54	0.93	0.44	0.12	0.00
1	3.46	2.84	2.27	1.76	1.35	1.09	1.00
2	4.05	3.52	3.03	2.61	2.28	2.07	2.00
3	4.26	4.25	3.84	3.49	3.23	3.06	3.00
4	5.40	5.02	4.68	4.40	4.18	4.05	4.00
5	6.15	5.83	5.55	5.32	5.15	5.04	5.00
6	6.94	6.67	6.44	6.25	6.12	6.03	6.00
7	7.76	7.54	7.36	7.20	7.09	7.02	7.00
8	8.61	8.44	8.28	8.06	8.07	8.02	8.00
9	9.50	9.35	9.22	9.13	9.06	9.02	9.00
10	10.38	10.27	10.17	10.10	10.04	10.01	10.00
11	11.30	11.21	11.14	11.08	11.03	11.01	11.00
12	12.24	12.17	12.11	12.06	12.03	12.01	12.00
13	13.19	13.14	13.09	13.05	13.02	13.01	13.00

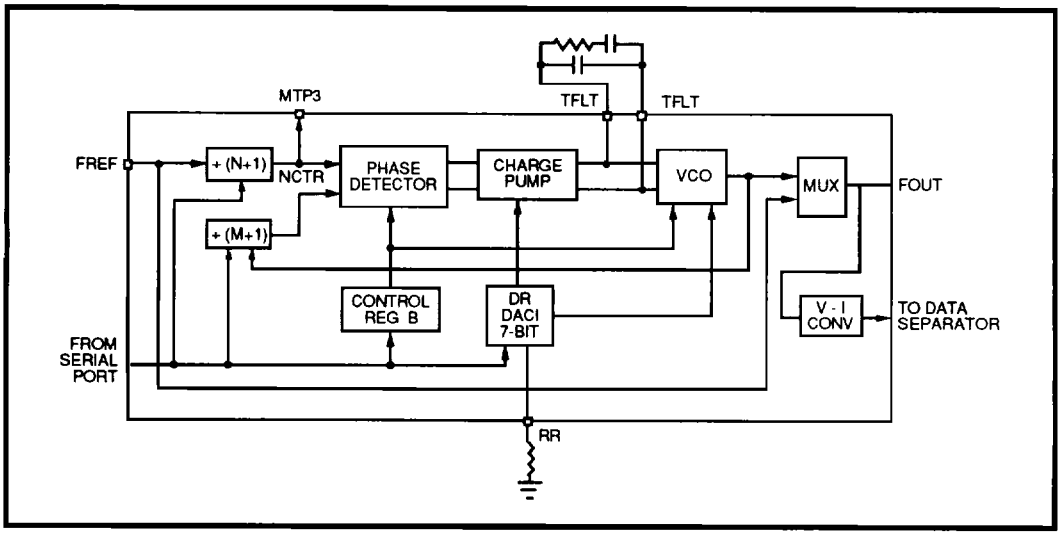


FIGURE 10: Time Base Generator Phase Locked Loop

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FUNCTIONAL DESCRIPTION (continued)

TIME BASE GENERATOR CIRCUIT DESCRIPTION

The time base generator, which is a PLL based circuit, provides programmable reference frequency FOUT, Figure 10. The frequency can be programmed with an accuracy better than 1%. An external passive loop filter is required to control the PLL locking characteristics. The filter is fully-differential and balanced in order to suppress common mode noise.

In read, write and idle modes, the time base generator is programmed to provide a stable reference frequency (FOUT) for the data synchronizer. In write and idle modes, FOUT is the output of the time base generator. In read mode FOUT is disabled after the data synchronizer has achieved lock and switched over to read data as the source for the RRC. This minimizes jitter in the data synchronizer PLL. The reference frequency is programmed using the M and N registers of the time base generator via the serial port, and is related to the external reference clock input, FREF, as follows:

$$FOUT = ((M+1)/(N+1))FREF$$

The VCO center frequency and the phase detector gain of the time base generator are controlled by an internal IDAC addressed through the Data Recovery Control Register (DRCR). To change the FOUT frequency, new values are preloaded into the M and N registers via the serial port. Acquisition of the new frequency begins only after a write operation is completed to the DRCR. To insure precise tracking of the data separator to the time base VCO, the control voltage from the VCO is converted to a current which is provided to the data separator VCO and 1/3 cell delay. The VCO frequency equation is:

$$Fvco = [12.5/(RR + 0.4)] \cdot [(0.715 \cdot IDAC) + 6.8] \text{ MHz}$$
$$= 1.5 \cdot \text{NRZ data rate.} \quad (28 \le IDAC \le 127)$$

where IDAC is the value in the DRCR and RR is the value (kΩ) of the external RR resistor.

DATA SEPARATOR CIRCUIT DESCRIPTION

The data separator circuit provides complete encoding, decoding, and synchronization for RLL 1,7 format data. In the read mode, the circuit performs sync field search and detect, data synchronization and data decoding. In the write mode, the circuit provides data encoding and write precompensation for NRZ data applied to the NRZ0/1 pins. Data rate is established by the internal time base generator and IDAC.

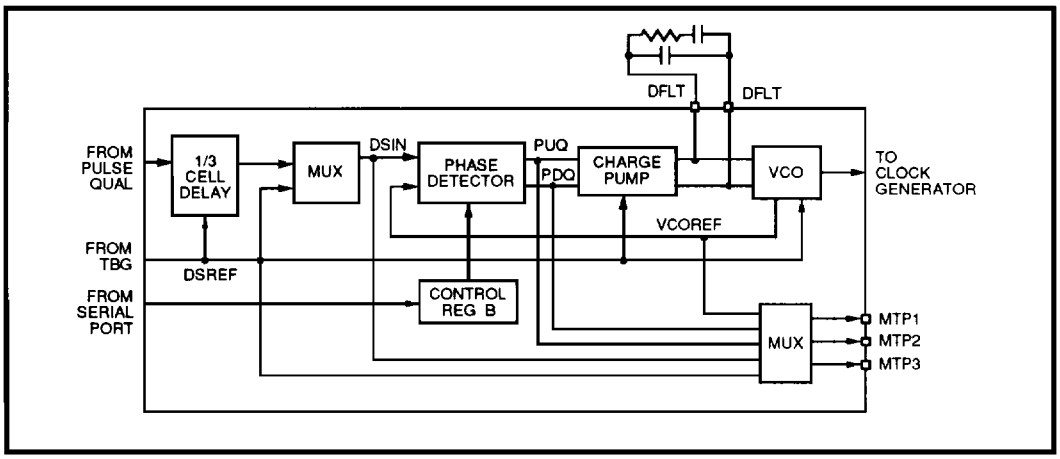

FIGURE 11: Data Separator Phase Locked Loop

FUNCTIONAL DESCRIPTION (continued)

PHASE LOCKED LOOP

The circuit employs a dual mode phase detector; harmonic in the read mode and non-harmonic in the write and idle modes, Figure 11. In the read mode the harmonic phase detector updates the PLL with each occurrence of a DRD pulse. In the write and idle modes the non-harmonic phase detector is continuously enabled, thus maintaining both phase and frequency lock onto the reference frequency of the internal time base generator. By acquiring both phase and frequency lock to the input reference frequency and utilizing a zero phase restart technique, the VCO transient is minimized and false lock to read data is eliminated. The phase detector incorporates a charge pump in order to drive the loop filter directly. The polarity and width of the output current pulses correspond to the direction and magnitude of the phase error.

The data synchronizer also requires an external passive loop filter to control its PLL locking characteristics. This filter is also fully-differential and balanced in order to suppress common mode noise.

READ/WRITE MODE CONTROL

The read gate (RG) and write gate (WG) inputs control device operation in data mode. RG is an asynchronous input that must be initiated at the start of a valid preamble field. It can be terminated at any position on the disk. WG is also an asynchronous input. It can be initiated at any time but should not be terminated prior to the last output write data pulse. To insure that the device will not enter any unknown states, RG overrides WG.

READ MODE

The data synchronizer utilizes a fully integrated fast acquisition PLL to accurately develop the decode window. Read gate (RG) initiates the PLL locking sequence and selects the PLL reference input; a high level (read mode) selects the internal RD input and a low level selects the reference clock. In the read mode the falling edge of $\overline{DRD}$ enables the phase detector while the rising edge is phase compared to the rising edge of the VCO reference (VCOR.) As depicted in Figure 12, $\overline{DRD}$ is a 1/3 NRZ bit cell wide pulse whose leading edge is defined by the falling edge of $\overline{RD}$. A decode window is developed from the VCOR clock.

VCO Lock and Bit Sync Enable

One of two VCO locking modes will be entered depending on the state of the gain shift (GS) bit, or bit 1, in the Control B register. An internal read gate is asserted 3 $\overline{DRD}$ transitions after read gate is asserted, see Figure 13. The phase detector then enters a high gain mode of operation to support fast phase acquisition. After an internal counter counts a total of 14 transitions

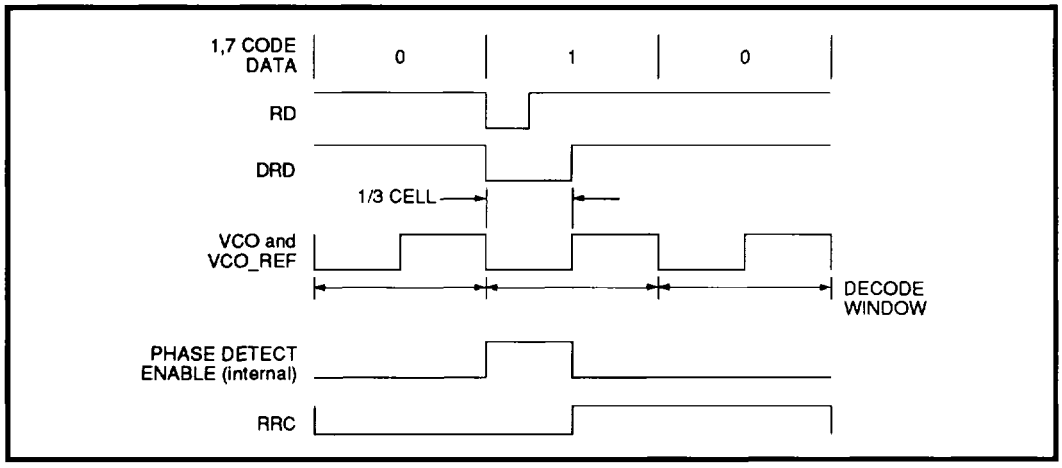

FIGURE 12: Data Synchronization Waveform

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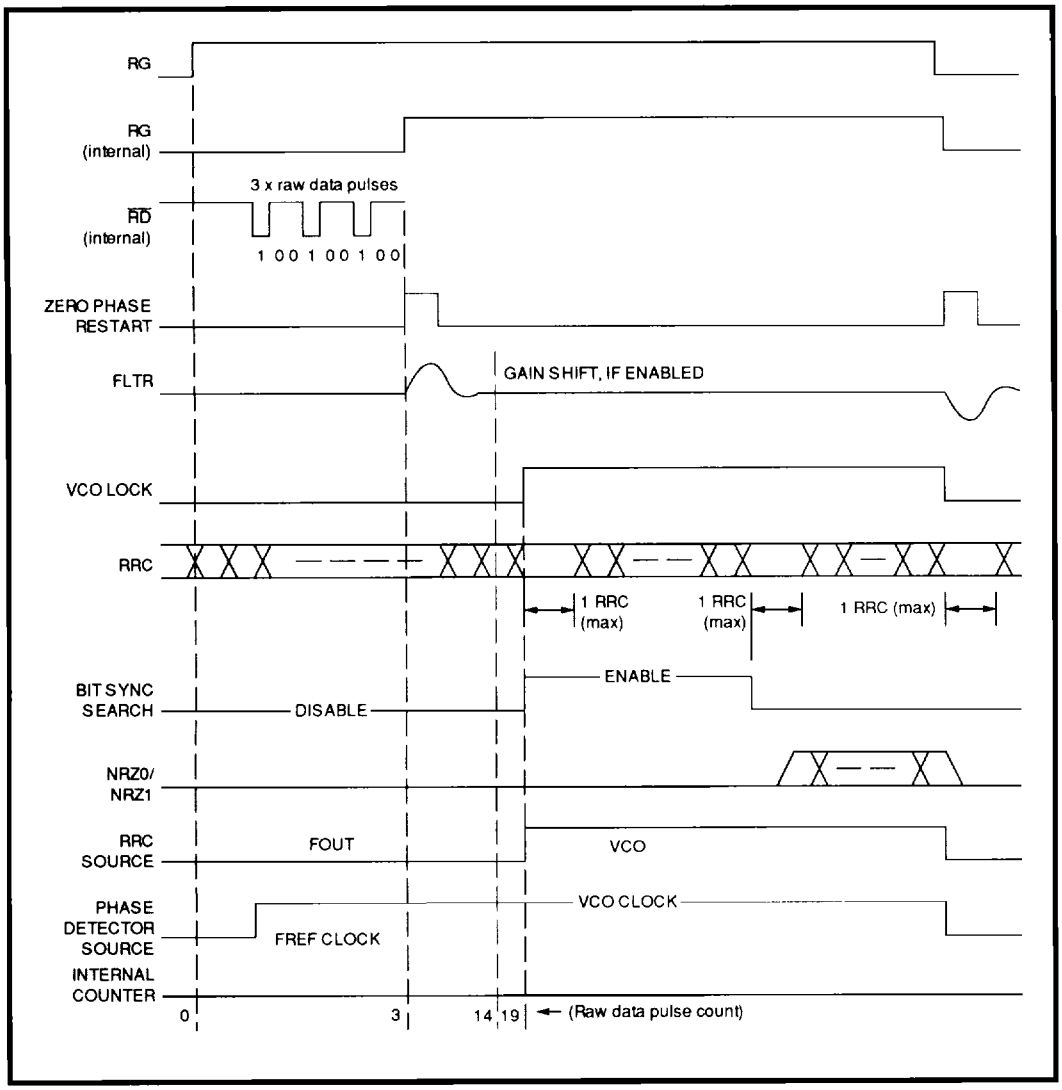

FIGURE 13: Read Mode Locking Sequence

PHASE LOCKED LOOP (continued)

VCO Lock and Bit Sync Enable

of the internal $\overline{DRD}$ signal, including the 3 transitions prior to internal read gate, the gain is reduced by a factor of 3 if GS = 1. If GS = 0 the gain remains constant. This gain shift reduction reduces the bandwidth and damping factor of the loop by $\sqrt{3}$ which provides improved jitter performance in the data follow mode. The counter continues to count the next 5 $\overline{DRD}$ transitions (a total of 19 • 3T from assertion of RG) and then asserts an internal VCO lock signal. The VCO lock signal activates the decoder bit synchronization circuitry to define the proper decode boundries. The next 2 • 3T patterns are used to set the proper decode window so that VCO is in sync with RRC and RRC is in sync with the data. Following this, the NRZ outputs are enabled and the data is toggled through the decoder for the duration of the RG.

When the VCO lock signal is asserted, the internal RRC source is switched from the time base generator output to the VCO output signal that is phase locked to $\overline{DRD}$. During the internal RRC switching period the external RRC signal may be held for a maximum of 1 NRZ clock period, however no short duration glitches will occur.

Window Shift

Shifting the phase of the VCO clock effectively shifts the relative position of the $\overline{DRD}$ pulse within the decode window. Decode window control is provided via the WS control bits of the Window Shift Control Register (WSCR).

The magnitude of the window shift is given by:

% VCO Period = 2.23% • (15 - WSDAC)

where WSDAC is the WSCR value

For example,

0100 ⇒ 24.53% window shift

NON READ MODE

In the non-read modes, the PLL is locked to the reference clock. This forces the VCO to run at a frequency which is very close to that required for tracking actual data. When the reference input to the PLL is switched, the VCO is stopped momentarily, then restarted in an accurate phase alignment with the next PLL reference input pulse. By minimizing the phase alignment error in this manner, the acquisition time is substantially reduced.

WRITE MODE

In the write mode the circuit converts NRZ data from the controller into 1,7 RLL formatted data for storage on the disk. Write mode is entered by asserting the write gate (WG) while the RG and SG are held low. During write mode the VCO and the RRC are referenced to the internal time base generator signal. The write data output is a differential PECL signal. The rising edge of the WD pin is the active edge. External termination of the WD/$\overline{WD}$ pins is required.

Write Mode Operation

Write mode is entered by asserting WG high ("1") while RG and SG are held low ("0"). A preamble pattern of at least 19 '3T' patterns must be generated before any coded data can be written. The 3T preamble is written by holding both NRZ0 and NRZ1 low ("0") while WCLK is toggled. The first non zero NRZ input bits indicate the end of the preamble pattern. After a delay of 3 WCLK time periods, non-preamble data begins to toggle out WD. At the end of the write cycle, 3 WCLK cycles of blank NRZ should be added to insure the encoder is flushed of data before the WG can be transitioned low. WD stops toggling a maximum of 2 WCLK time periods after WG goes low. Reference Figures 14 and 15 for detailed timing information. In Figure 15, note that the NRZ1 bit is shifted into the encoder first and the NRZ0 bit is shifted into the encoder second. Because two bits are clocked into the device on each WCLK pulse, the encoder will always generate a predictable pattern.

Direct Write Function

The 32P4752/4756 include a Direct Write (DW) function that allows the NRZ0 data to bypass the encoder and write precomp circuitry. When the DW bit is set in the CBR, the data applied to NRZ0 will bypass the encoder and write precomp and directly control the WD/ $\overline{WD}$ output buffer. This allows the user to perform DC erase and media tests.

A rising edge at NRZ0 causes a rising edge on $\overline{WD}$ and a falling edge on WD. A falling edge at NRZ0 causes a falling edge on $\overline{WD}$ and a rising edge on WD. The DW bit also overrides SG, RG, and WG.

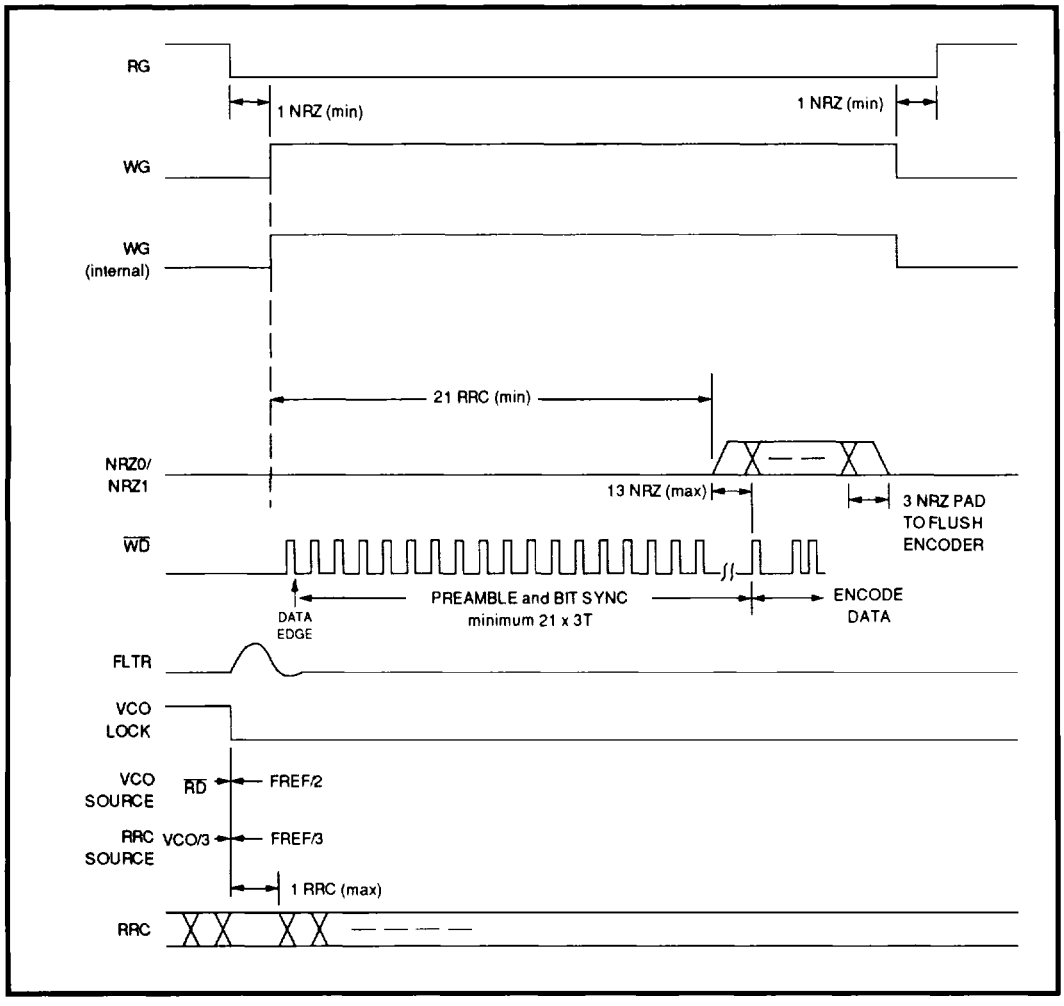

FIGURE 14: Write Data Operation

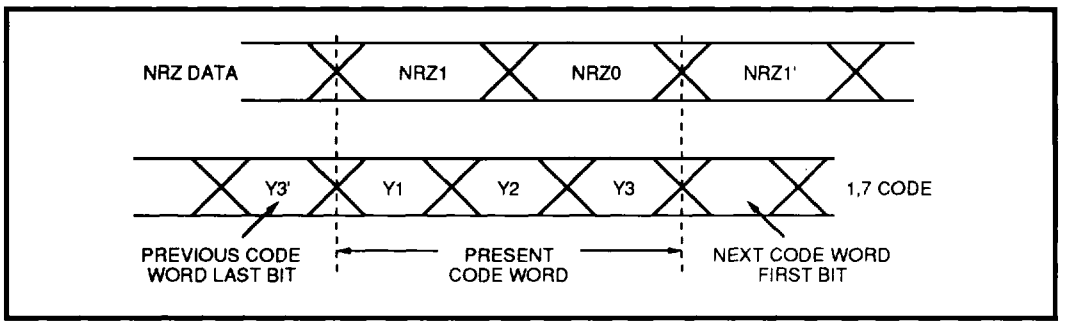

FIGURE 15: NRZ Data Word to 1,7 Code Word Bit Comparison
(Reference Table 7 for decode scheme)

FUNCTIONAL DESCRIPTION (continued)

OPERATING MODES AND CONTROL

The device has several operating modes that support read, write, servo, and power management functions. Mode selection is accomplished by controlling the read gate (RG), write gate (WG), servo gate (SG), and $\overline{\text{PWRON}}$ pins. Additional modes are also controlled by programming the Power Down Control Register (PDCR), the Control A (CAR) register, and the Control B (CBR) register via the serial port.

External Mode Control

All operating modes of the device are controlled by driving the read gate (RG), write gate (WG), servo gate (SG), and $\overline{\text{PWRON}}$ pins with TTL compatible signals (refer to Table 4). For normal operation the $\overline{\text{PWRON}}$ pin is driven low. During normal operation the device is controlled by the read gate (RG), write gate (WG), and servo gate (SG) pins. Servo gate (SG) determines the active mode of the device. When SG is high, the device enters the servo mode, regardless of the state of either RG or WG. When SG is low, RG and WG can be used. When RG is high the device is in read mode regardless of the state of WG. When SG and RG are both low, WG is brought high to enter write mode. If SG, RG, and WG pins are all low the device will be in idle mode.

REGISTER DESCRIPTION

Control Registers

The serial port registers allow the user to configure the device. The register map for the device is shown in Table 5. The bits of these registers are defined as follows:

POWER DOWN CONTROL REGISTER (PDCR)

BIT	NAME	DESCRIPTION
0	PD/SVO	Pulse detector/servo power enable: Determines the state of the pulse detector and servo circuits when $\overline{\text{PWRON}}$ pin is low. 0 = Circuits enabled 1 = Circuits powered down
1	NA	Not used. Set to zero
2	FLTR	Filter power enable: Determines the state of the filter when $\overline{\text{PWRON}}$ pin is low. 0 = Filter enabled 1 = Filter powered down
3	DS	Data separator power enable: Determines the state of the data separator circuit when $\overline{\text{PWRON}}$ pin is low. 0 = Data separator enabled 1 = Data separator powered down
4	TBG	Time base generator power enable: Determines the state of the Time base generator circuit when $\overline{\text{PWRON}}$ pin is low. 0 = Time base generator enabled 1 = Time base generator powered down
5-7	N/A	Device ID: These bits are a read only ID code for the device.

REGISTER DESCRIPTION (continued)

DATA MODE CUTOFF (DACF)

BIT	NAME	DESCRIPTION
0-6	DMC	Filter cutoff setting for data mode. Substitute this value for DACF into the cutoff calculation for the filter in data mode operation.
7	OSC ON	Enable oscillator: 0 = disabled 1 = enabled

SERVO MODE CUTOFF (DACF)

0-6	DMC	Filter cutoff setting for servo mode. Substitute this value for DACF into the cutoff calculation for the filter in servo mode operation.
7	GDE	Group delay enabled in servo mode. 0 = disabled 1 = enabled

FILTER BOOST REGISTER (DACS)

0-6	FBC	Filter boost setting. Substitute this value for DACS into filter calculations.
7	SBE	Servo boost enable: Determines if boost is enabled when SG is high. 0 = Boost disabled when SG is high 1 = Boost enabled when SG is high

FILTER GROUP DELAY REGISTER (DACG)

0-6	GDM	Filter group delay magnitude. Substitute this value for DACG into group delay calculation.
7	GDS	Group delay sign. 0 = negative 1 = positive

DATA THRESHOLD REGISTER (VTHDAC)

0-6	DTH	Data threshold setting. Substitute this value for VTHDAC into the threshold calculation for data mode operation.
7	DQ	Qualifier select: Determines the type of qualifier used in data mode. 0 = Hysteresis qualifier 1 = Dual comparator qualifier

SERVO THRESHOLD REGISTER (VTHDAC)

0-6	STH	Servo threshold setting. Substitute this value for VTHDAC into the threshold calculation for servo mode operation.
7	SQ	Qualifier select: Determines the type of qualifier used in servo mode. 0 = Hysteresis qualifier 1 = Dual comparator qualifier

REGISTER DESCRIPTION (continued)

CONTROL A REGISTER (CAR)

BIT	NAME	DESCRIPTION
0	EPDT	Enable Phase Detector (Time Base Generator): This bit disables the output of the phase detector to the VCO. An external voltage applied across the TFLT pins drives the VCO to a fixed frequency. 0 = Phase detector disabled 1 = Phase detector enabled (normal operation)
1	UT	Enable Pump Up Current (Time Base Generator): This bit enables a test mode for checking the charge pump output current. The charge pump will source a fixed DC current from TFLT and sink the current at $\overline{\text{TFLT}}$. 0 = Not in pump up test mode. 1 = continuous pump up, for test use only.
2	DT	Enable Pump Down Current (Time Base Generator): This bit enables a test mode for checking the charge pump output current. The charge pump will source a fixed DC current from $\overline{\text{TFLT}}$ and sink the current at TFLT. 0 = Not in pump down test mode 1 = continuous pump down, for test use only.
3	MTP3E	This bit enables the MTP3 test point output buffer. 0 = Test point disabled 1 = Test point enabled
4	BYPT	This bit enables a time base generator bypass mode where the FREF input is connected to the data separator phase detector input. 0 = Time base generator in use 1 = Time base generator bypassed
5/6	TMS0/1	These bits select the test point signal sources (ref Table 9)
7	FDTM	This bit continuously enables the AGC fast decay current. 0 = Fast decay current always on 1 = Normal fast decay operation Set to 1 for normal operation.

CONTROL B REGISTER (CBR)

BIT	NAME	DESCRIPTION
0	DW	This bit enables the direct write (Bypass Endec) function. 0 = ENDEC in use. 1 = Bypass encoder, NRZ0 buffered to $\overline{WD}$/WD.
1	GS	This enables the data separator phase detector gain switch in read mode. 0 = Gain remains high for the entire read cycle. 1 = 14 • 3T (read mode only) following RG01 transition. Switches from high to low after gain.
2	RDIO	This bit enables the $\overline{RDIO}$ pin as an input or output. 0 = $\overline{RDIO}$ is an output 1 = $\overline{RDIO}$ is an input
3	EPDD	Enable Phase Detector (Data Separator): This bit disables the output of the phase detector to the VCO. An external voltage applied across the DFLT pins drives the VCO to a fixed frequency. 0 = Phase detector charge pump disabled 1 = Phase detector active
4	UD	Enable Pump Up Current (Data Separator): This bit enables a test mode for checking the charge pump output current. The charge pump will source a fixed DC current from DFLT and sink the current at $\overline{DFLT}$. 0 = not in pump up test mode 1 = continuous pump up, for test use only
5	DD	Enable Pump Down Current (Data Separator): This bit enables a test mode for checking the charge pump output current. The charge pump will source a fixed DC current from $\overline{DFLT}$ and sink the current at DFLT. 0 = Not in pump down test mode. 1 = Continuous pump down, for test use only
6	MTPEN	This bit enables the multiplexed test points (MTP1, 2, 3) 0 = Test points disabled 1 = Test points enabled
7	TM	Test mode bit: SSi use only. Set to 0 for normal operation.

N COUNTER REGISTER

0-6	N	N counter value.
7	TBG KD	Determines the phase detector gain of the TBG. 0 = KD is 1 • nominal value 1 = KD is 3 • nominal value

M COUNTER REGISTER

0-7	M	M counter value.

REGISTER DESCRIPTION (continued)

DATA RECOVERY REGISTER (DRCR)

BIT	NAME	DESCRIPTION
0-6	IDAC	Center frequency DAC value. Sets the center frequency for the data synchronizer VCO and the TBG VCO.
7	NSYC	This bit enables synchronization between STROBE and FWR output. 0 = in sync. 1 = no sync.

WINDOW SHIFT REGISTER (WSR)

0-3	WS	Window shift DAC magnitude.
4	WSD	Window shift direction. 0 = Early 1 = Late
5	WSE	Window shift enable. 0 = Disable 1 = Enable
6-7	TDAC0/1	DACOUT test point select: Selects the DAC output to be provided on the DACOUT test point. The preferred setting when DACOUT is not being monitored is to set TDAC0 = 1 and TDAC1 = 0:

TDAC1	TDAC0	DAC MONITORED
0	0	Filter Fc DAC
0	1	Qualifier threshold DAC (VTH)
1	0	Window shift DAC
1	1	Write precomp DAC; the selection of the early or late DAC is controlled by the WPE bit. WPE = 0 — Late WPE = 1 — Early

WRITE PRECOMP REGISTER (WPR)

0-2	WPE	Write precomp early/magnitude.
3	WPE	Write precomp enable. 0 = Disable 1 = Enable
4-6	WPL	Write precomp late magnitude.
7	LZT	Low-Z time period: Determines the time period for the low-Z and fast decay one-shots. 0 = 1 µs nominal (0.4 µs hold on SG edges) 1 = 2 µs nominal (0.5 µs hold on SG edges)

AGC LEVEL REGISTER (ALR)

BIT	NAME	DESCRIPTION
0-3	ADAC	AGC level DAC value. Sets AGC level in servo mode.
		0000 = 1.2 Vp-p 1111 = 0.8 Vp-p
4-7	PDAC	Servo peak detector current DAC value. Sets the servo peak detector current in 6 µA steps. 0000 = 6 µA charge current 1111 = 96 µA charge current

Power Down Control

For power management, the $\overline{\text{PWRON}}$ pin can be used in conjunction with the Power Down Control Register (PDCR) to set the operating mode of the device. The PDCR provides a control bit for each of the functional blocks. When the $\overline{\text{PWRON}}$ pin is brought high ("1") the device is placed into sleep mode (<0.5 mA) and all circuits are powered down except the serial port. This allows the user to program the serial port registers while still conserving power. Register information is retained during the sleep mode so it is not necessary to reprogram the serial port registers after returning to an active mode. When the $\overline{\text{PWRON}}$ pin is low ("0"), the contents of the PDCR determine which blocks will be active. Register mapping for the PDCR is shown in Table 5. To improve recovery time from the sleep mode, the inputs to the filter and AGC circuits are placed into a Low-Z mode.

TABLE 4: Mode Control Table

CONTROL LINE				DEVICE MODE	DAC CONTROL			
$\overline{PWRON}$	RG	SG	WG		VTH	FC	BOOST	HYSTERESIS
1	X	X	X	**SLEEP MODE:** All functions are powered down. The serial port registers remain active and register programming data is saved.	off	off	off	off
0	0	0	1	**WRITE MODE:** The pulse detector is inactive. The data synchronizer VCO is locked to the internal time base generator. Write precomp circuit is clocked by internal time base.	DR	DR	DR	DR
0	1	0	X	**READ MODE:** The pulse detector is active. The data synchronizer begins the preamble lock sequence.	DR	DR	DR	DR
0	X	1	X	**SERVO MODE:** The pulse detector is active and the servo control registers are enabled for the Fc DAC and the VTH DAC. $\overline{RDIO}$ is also active. The data synchronizer and time base generator can be disabled using the PDCR.	SR	SR	off (On if SBE = 1)	SR
0	0	0	0	**IDLE MODE:** The contents of the PDCR determine which blocks are powered-up. In normal operation with all blocks powered-up, the pulse detector is active, the data synchronizer VCO is locked to the time base generator, and the data control registers are used for VTH and FC.	DR	DR	DR	DR
				If multiple control signals are active, the priority order will be $\overline{PWRON}$, SG, RG, and WG. For example, if SG and RG are both "1", the Servo mode will be active.				

DAC Control Key: DR = data register, SR = servo register, off = disabled

DAC Control Key: DR = data register, SR = servo register, off = disabled

TABLE 5: Serial Port Register Mapping

REGISTER NAME	A6						A0	R/W	D7							D0
	ADDRESS								DATA BIT MAP							
POWER DOWN CONTROL	0	0	0	0	0	1	0	0	--	--	--	TBG 1 = Disable 0 = Enable	DATA SEP 1 = Disable 0 = Enable	FILTER 1 = Disable 0 = Enable	N/C	PD/SERVO 1 = Disable 0 = Enable
DATA MODE CUTOFF	0	0	0	0	0	1	1	0	OSC ON 1 = OSC ON 0 = OSC OFF	F_{CO}DACF BIT 6	F_{CO}DACF BIT 5	F_{CO}DACF BIT 4	F_{CO}DACF BIT 3	F_{CO}DACF BIT 2	F_{CO}DACF BIT 1	F_{CO}DACF BIT 0
SERVO MODE CUTOFF	0	0	1	0	0	1	1	0	GDE Boost 1 = Enable 0 = Disable	F_{CS}DACF BIT 6	F_{CS}DACF BIT 5	F_{CS}DACF BIT 4	F_{CS}DACF BIT 3	F_{CS}DACF BIT 2	F_{CS}DACF BIT 1	F_{CS}DACF BIT 0
FILTER BOOST	0	0	0	1	0	1	1	0	Servo Boost 1 = Enable 0 = Disable	DACS BIT 6	DACS BIT 5	DACS BIT 4	DACS BIT 3	DACS BIT 2	DACS BIT 1	DACS BIT 0
DATA THRESHOLD	0	0	0	1	0	1	0	0	Data Qual. 1 = Dual 0 = Hys	T_{DO}DAC BIT 6	T_{DO}DAC BIT 5	T_{DO}DAC BIT 4	T_{DO}DAC BIT 3	T_{DO}DAC BIT 2	T_{DO}DAC BIT 1	T_{DO}DAC BIT 0
SERVO THRESHOLD	0	0	1	0	0	1	0	0	Servo Qual. 1 = Dual 0 = Hys	T_{SO}DAC BIT 6	T_{SO}DAC BIT 5	T_{SO}DAC BIT 4	T_{SO}DAC BIT 3	T_{SO}DAC BIT 2	T_{SO}DAC BIT 1	T_{SO}DAC BIT 0
CONTROL A	0	0	1	1	0	1	0	0	FD Test 1 = Disable 0 = Enable	TMS1	TMS0	TBG 1 = Bypass 0 = Normal	MTP3 1 = Enable 0 = Disable	PUMP DWN 1 = ON 0 = OFF	PUMP UP 1 = ON 0 = OFF	PHASE DET 1 = Enable 0 = Disable
CONTROL B	0	0	0	1	1	0	0	0	TEST MODE 1 = RESET 0 = NORMAL	MTPEN 1 = Enable 0 = Disable	PUMP DWN 1 = ON 0 = OFF	PUMP UP 1 = ON 0 = OFF	PHASE DET 1 = Enable 0 = Disable	RDIO 1 = Input 0 = Output	GAIN SHFT 1 = ON 0 = OFF	DIR WRITE 1 = ON 0 = OFF
N COUNTER	0	0	0	0	1	1	0	0	TBG KD 1 = 1x KD 0 = 3 x KD	N COUNT BIT 6	N COUNT BIT 5	N COUNT BIT 4	N COUNT BIT 3	N COUNT BIT 2	N COUNT BIT 1	N COUNT BIT 0
M COUNTER	0	0	0	1	1	1	0	0	M COUNT BIT 7	M COUNT BIT 6	M COUNT BIT 5	M COUNT BIT 4	M COUNT BIT 3	M COUNT BIT 2	M COUNT BIT 1	M COUNT BIT 0
DATA RECOVERY	0	0	0	0	1	0	0	0	NO_SYNC SET TO 0	DAC BIT 6	DAC BIT 5	DAC BIT 4	DAC BIT 3	DAC BIT 2	DAC BIT 1	DAC BIT 0
WINDOW SHIFT	0	0	0	0	1	0	1	0	TDAC 1	TDAC 0	WIN SHFT 1 = Enable 0 = Disable	WS DIR 1 = Late 0 = Early	$\overline{WS3}$	$\overline{WS2}$	$\overline{WS1}$	$\overline{WS0}$
WRITE PRECOMP	0	0	0	1	1	0	1	0	Low-Z Time 1 = 2 µs 0 = 1 µs	$\overline{WL2}$	$\overline{WL1}$	$\overline{WL0}$	WR PRCMP 1 = Enable 0 = Disable	$\overline{WE2}$	$\overline{WE1}$	$\overline{WE0}$
AGC LEVEL	0	1	0	0	0	1	0	0	PDAC BIT 3	PDAC BIT 2	PDAC BIT 1	PDAC BIT 0	ADAC BIT 3	ADAC BIT 2	ADAC BIT 1	ADAC BIT 0
GDE BOOST	0	0	1	1	0	1	1	0	GD DIR 1 = POS 0 = NEG	GD DAC BIT 6	GD DAC BIT 5	GD DAC BIT 4	GD DAC BIT 3	GD DAC BIT 2	GD DAC BIT 1	GD DAC BIT 0

* Denotes SSi internal test bits. These bits should be set to 0 in normal operation.

REGISTER DESCRIPTION (continued)

SERIAL INTERFACE OPERATION

The serial interface is a bi-directional port for reading and writing programming data from/to the internal registers of the 32P4752/4756. For data transfers SDEN is brought high, serial data is presented at the SDATA pin, and a serial clock is applied to the SCLK pin. After the SDEN goes high, the first 16 pulses applied to the SCLK pin will shift the data presented at the SDATA pin into an internal shift register on the rising edge of each clock. An internal counter prevents more than 16 bits from being shifted into the register. The data in the shift register is latched when SDEN goes low. If less than 16 clock pulses are provided before SDEN goes low, the data transfer is aborted.

All transfers are shifted into the serial port LSB first. The first byte of the transfer is address and instruction information. The LSB of this byte is the R/W bit which determines if the transfer is a read (1) or a write (0). The remaining 7-bits determine the internal register to be accessed. Table 5 provides register mapping information. The second byte contains the programming data. In read mode (R/W=1) the 32P4752/4756 will output the register contents of the selected address. In write mode the device will load the selected register with data presented on the SDATA pin. At initial power-up, the contents of the internal registers will be in an unknown state and they must be programmed prior to operation. During power down modes, the serial port remains active and register programming data is retained.

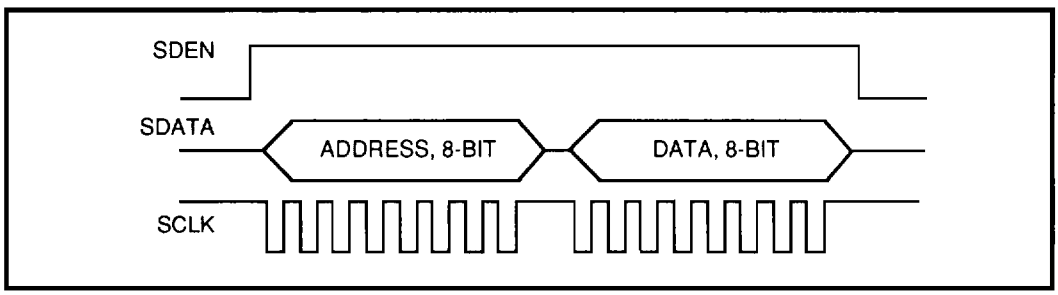

FIGURE 16(a): Serial Port Transfer Format

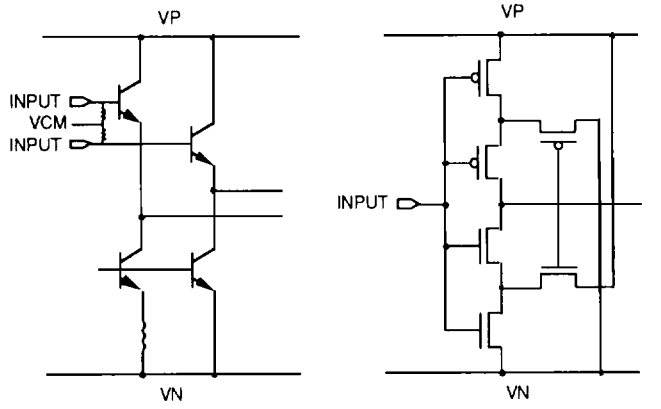

FIGURE 17(a): Input Structures

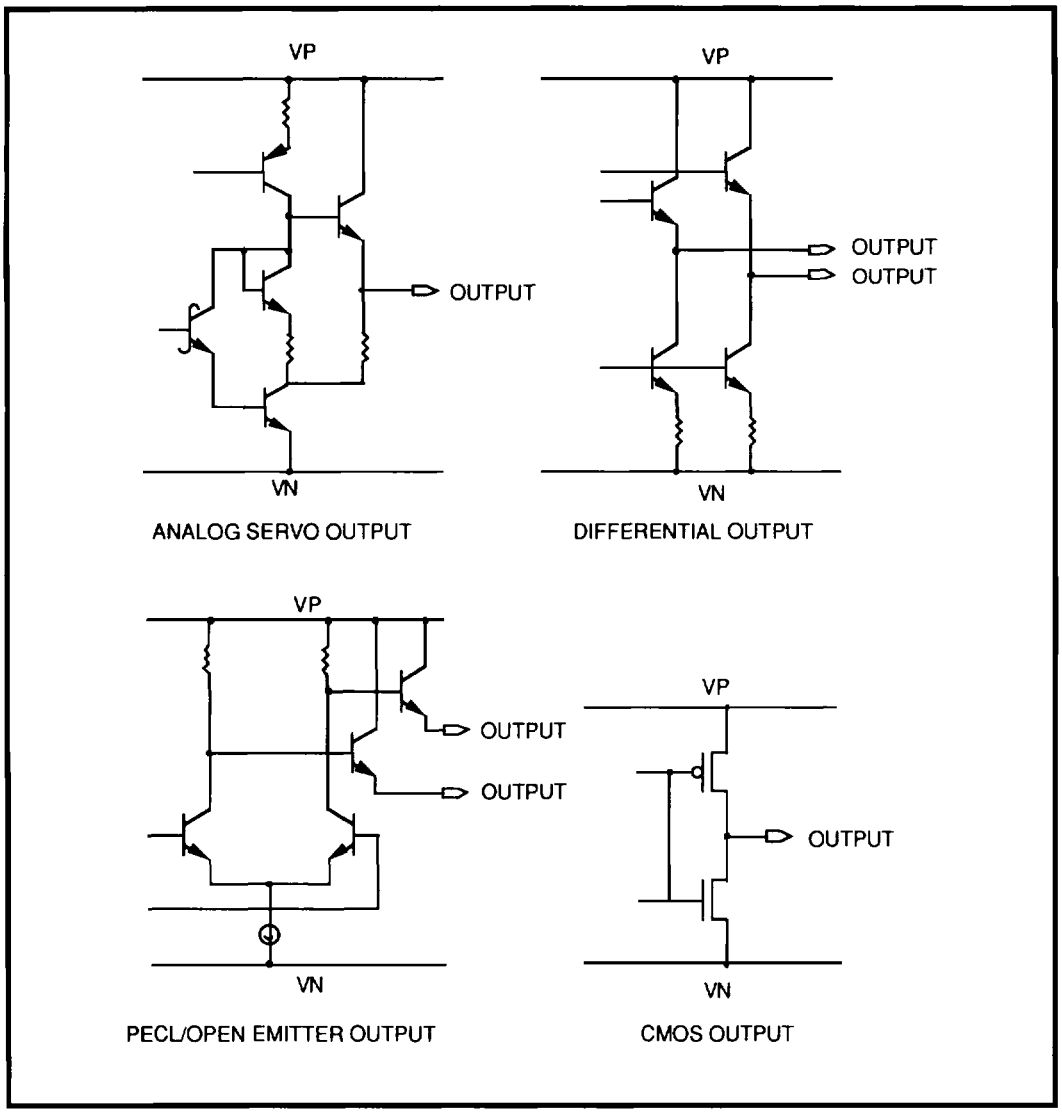

FIGURE 17(b): Output Structures

PIN DESCRIPTION

POWER SUPPLY PINS

NAME	TYPE	DESCRIPTION
VPA		Data separator PLL analog power supply pin
VPB		Time base generator PLL analog power supply pin
VPC		Internal ECL, CMOS logic power supply pin
VPE		WD/$\overline{WD}$ buffer digital power supply pin
VPD		TTL buffer I/O digital power supply pin
VPG		Pulse detector, filter, servo analog power supply pin
VNA		Data separator PLL analog ground pin
VNB		Time base generator PLL analog ground pin
VNC		Internal ECL, CMOS logic ground pin
VND		TTL buffer I/O digital ground pin
VNG		Pulse detector, filter, servo analog ground pin
VNE		WD/$\overline{WD}$ buffer digital ground pin

INPUT PINS

VIA, $\overline{VIA}$	I	AGC AMPLIFIER INPUTS: Differential AGC amplifier input pins.
DP, DN	I	ANALOG INPUTS FOR DATA PATH: Differential analog inputs to data comparators, full-wave rectifier.
CP, CN	I	ANALOG INPUTS FOR CLOCK PATH: Differential analog inputs to the clock comparator.
$\overline{PWRON}$	I	Power Enable: TTL compatible CMOS power control input. A low level CMOS input enables power to circuitry according to the contents of the PDCR. A high level CMOS input shuts down all circuitry.
$\overline{HOLD}$	I	HOLD CONTROL: TTL compatible CMOS control pin which, when pulled low, disables the AGC charge pump and holds the AGC amplifier gain at its present value.
STROBE	I	BURST STROBE: TTL compatible CMOS burst strobe input. A high level TTL input will enable the servo peak detector to charge one of the burst capacitors. The falling edge of STROBE increments an internal counter that determines which burst capacitor will charge on the next STROBE pulse (reference Figure 7(a), 7(b) for timing.)
$\overline{RESET}$	I	RESET CONTROL INPUT: TTL compatible CMOS reset input. A low level TTL input will discharge the internal servo burst hold capacitors on channels A-D.
IN, $\overline{IN}$	I	FILTER SIGNAL INPUTS: The AGC output signals must be AC coupled into these pins.

PIN DESCRIPTION (continued)

INPUT PINS (continued)

NAME	TYPE	DESCRIPTION
FREF	I	REFERENCE FREQUENCY INPUT: Frequency reference input for the time base generator. FREF should be driven either by a direct coupled TTL signal or by an AC coupled ECL signal.
NRZ0/1	I/O	NRZ I/O PORT: TTL compatible CMOS NRZ data port. In read mode, valid data is output on these pins with each cycle of RRC. In write mode, data input on these pins is clocked into the device by WCLK.
RG	I	READ GATE: TTL compatible CMOS read gate input. A high level TTL input selects the RD input and enables the read mode/address detect sequences. A low level selects the FREF input.
SG	I	SERVO GATE: TTL compatible CMOS servo gate input. A high level TTL input activates the servo mode by selecting the servo control registers, the $\overline{RDIO}$ pin active in idle mode, the PPOL pin also active in idle mode, and the RTS resistor.
WCLK	I	WRITE CLOCK: TTL compatible CMOS write clock input. Must be synchronous with the write data NRZ0/1 input. For short cable delays, WCLK may be connected directly to pin RRC.For long cable delays, WCLK should be connected to an RRC return line matched to the NRZ data bus line delay.
WG	I	WRITE GATE: TTL compatible CMOS write gate input. A high level input enables the write mode.

OUTPUT PINS

MTP1,2,3	O	MULTIPLEXED TEST POINTS: Open emitter ECL output test points. Internal test signals are routed to these test points as determined by the CAR and CBR. Two pull up and down resistors are required to use this pin. They should be removed during normal operation to reduce power dissipation. (Reference Table 9)
OD, $\overline{OD}$	O	FILTER DIFFERENTIATED OUTPUTS: Filter differentiated outputs. These outputs are AC coupled into the CP/CN inputs.
ON, $\overline{ON}$	O	FILTER NORMAL OUTPUTS: Filter normal low pass output signals. These outputs are AC coupled into the DP/DN inputs.
PPOL	O	PULSE POLARITY: Pulse polarity CMOS compatible output. The output is high when the pulse being qualified is positive and it is low when the pulse being qualified is negative.
$\overline{RDIO}$	O	READ DATA I/O: Bi-directional TTL compatible CMOS pin. $\overline{RDIO}$ outputs $\overline{RD}$ pulses when in idle or servo modes of operation. $\overline{RDIO}$ is an input when the RDIO bit is enabled in the CBR.
RRC	O	READ REFERENCE CLOCK: Read clock CMOS compatible output. During a mode change, no glitches are generated and no more than one lost clock pulse will occur. When RG goes high, RRC initially remains synchronized to FOUT. When the Sync Bits are detected, RRC is synchronized to the $\overline{DRD}$. When RG goes low, RRC is synchronized back to the FOUT.

OUTPUT PINS (continued)

NAME	TYPE	DESCRIPTION
VOA, $\overline{VOA}$	O	AGC AMPLIFIER OUTPUT: Differential AGC amplifier output pins. These outputs are ac coupled into the filter inputs (IN/$\overline{IN}$).
WD/$\overline{WD}$	O	WRITE DATA: Differential PECL encoded write data. The rising edge of the WD pin represents the data bit (precomped edge). These are open emitter outputs, and an external pull-down resistor is required.

ANALOG PINS

A, B, C, D 32P4752	O	SERVO OUTPUTS: These outputs are processed versions of the voltages captured on the servo hold capacitors. They are referenced to an internally generated, 0.5V baseline.
A-B, C-D, A+B 32P4756	O	SERVO OUTPUTS: These outputs are processed versions of the voltages captured on the servo hold capacitors. They are referenced to SREF.
BYP	O	The AGC integrating capacitor CA, is connected between BYP and VPG.
TFLT/$\overline{TFLT}$	O	PLL LOOP FILTER: These pins are the connection points for the time base generator loop filter.
DACOUT	O	DAC VOLTAGE TEST POINT: This test point monitors the outputs of the internal DACs. The source DAC is selected by programming the two MSBs of the WSCR register.
DFLT/$\overline{DFLT}$	O	PLL LOOP FILTER: These pins are the connection points for the data separator loop filter.
LEVEL	O	An NPN emitter output that provides a full-wave rectified signal from the DP, DN inputs. An external capacitor should be connected from LEVEL to VPG to set the hysteresis threshold time constant in conjunction with RTS and RTD. An internal current source provides 60 µA of pull-down current at this pin.
RR	O	REFERENCE RESISTOR INPUT: An external 1% resistor is connected from this pin to VNA to establish a precise internal reference current for the data separator and time base generator.
RTS	O	SERVO TIME CONSTANT RESISTOR INPUT: An external resistor is connected from this pin to LEVEL to establish the hysteresis threshold time constant when in servo mode.
RTD	O	DATA TIME CONSTANT RESISTOR INPUT: An external resistor is connected from this pin to LEVEL to establish the hysteresis threshold time constant when not in servo mode.

PIN DESCRIPTION (continued)

ANALOG PINS (continued)

NAME	TYPE	DESCRIPTION
RX	O	REFERENCE RESISTOR INPUT: An external 1% resistor is connected from this pin to VNG to establish a precise PTAT (proportional to absolute temperature) reference current for the filter. A 1000 pF capacitor should be placed in parallel with this resistor.
SREF 32P4756	I	SERVO REFERENCE: An external reference is applied to this pin to set the A-B = 0 voltage. The external voltage should be Vcc • 0.4.
MAXREF 32P4752	O	SERVO REFERENCE: An external voltage output that can be used as the reference for an external A/D converter. This represents the maximum output voltage for the A, B, C, and D outputs.

SERIAL PORT PINS

SDEN	I	SERIAL DATA ENABLE: Serial enable CMOS input. A high level input enables the serial port.
SDATA	I	SERIAL DATA: Serial data CMOS input. NRZ programming data for the internal registers is applied to this input.
SCLK	I	SERIAL CLOCK: Serial clock CMOS input. The clock applied to this pin is synchronized with the data applied to SDATA.

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, the recommended operating conditions are as follows: 4.5V < POSITIVE SUPPLY VOLTAGE < 5.5V, 0°C < T (ambient) < 70°C, and 25°C < T(junction) < 135°C. Currents flowing into the chip are positive. Current maximums are currents with the highest absolute value.

ABSOLUTE MAXIMUM RATINGS

Operation beyond the maximum ratings may damage the device

PARAMETER	RATING
Storage temperature	-65 to 150°
Positive supply voltage (Vp)	-0.5 to 7V
Voltage applied to any pin	-0.5V to Vp+0.5V

POWER SUPPLY CURRENT AND POWER DISSIPATION

Unless otherwise specified, Ta = 26°C and data rate = max. All test points and outputs are open. The test points are disabled.

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
ICC	$\overline{PWRON}$ = 0 All blocks enabled		110	160	mA
PWR Power Dissipation	$\overline{PWRON}$ = 0 All blocks enabled		550	745	mW
Sleep Mode Current	$\overline{PWRON}$ = 1 SG, RG, WG, STROBE, $\overline{RESET}$, WCLK = 0 All other CMOS inputs = 1		0.4	1.5	mA
Servo Mode Current	$\overline{PWRON}$ = 0 SG = 1 Power Reg. = 5 hex		55	85	mA

DIGITAL INPUTS AND OUTPUTS

TTL COMPATIBLE INPUTS

Inputs will float high "1" if left open.

Input low voltage	VIL				0.8	V
Input high voltage	VIH		2			V
Input low current	IIL	VIL = 0.4V			-100	µA
Input high current	IIH	VIH = 2.4V			100	µA

CMOS COMPATIBLE INPUTS

Schmitt trigger type, do not leave open. Nominal 1V hysteresis around VPD.

Input low voltage	VPC = 5V			1.5	V
Input high voltage	VPC = 5V	3.5			V

CMOS COMPATIBLE OUTPUTS

Output low voltage	IOL = 4 mA, VPD = 5V			0.5	V
Output high voltage	IOH = -4 mA, VPD = 5V	4.5			V
Rise time	0.8 to 2V CL ≤ 15 pF			5	ns
Fall time	2 to 0.8V CL ≤ 15 pF			5	ns

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ELECTRICAL SPECIFICATIONS (continued)

FREF INPUT

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Recommended input level	AC-coupled	1.2		2	Vp-p
Input resistance	Ref. only		11		kΩ

TEST POINT OUTPUT LEVELS (MTP1, MTP2, MTP3)

Output high level	402Ω to VND 261Ω to VPD for reference use only	VPD - 1.25			V
Output low level	402Ω to VND 261Ω to VPD for reference use only			VPD - 1.39	V

PECL OUTPUT LEVELS (WD,$\overline{WD}$)

Output high level	261Ω to VPD 402Ω to VND	VPD - 1.1			V
Output low level	261Ω to VPD 402Ω to VND			VPD - 1.39	V

SERIAL PORT TIMING

SCLK Data Clock period		read from serial port	140			ns
		write to serial port	100			ns
SCLK low time	TCKL	read from serial port	60			ns
		write to serial port	40			ns
SCLK high time	TCKH	read from serial port	60			ns
		write to serial port	40			ns
Enable to SCLK	TSENS		35			ns
SCLK to disable	TSENH		100			ns
Data set-up time	TDS		15			ns
Data hold time	TDH		15			ns
SDATA tri-state delay	TSENDL				50	ns
SDATA turnaround time	TTRN		70			ns
SCLK falls to Valid Data	TDSKEW	cload ≤ 15 pF	0		50	ns
SDEN low time	TSL		200			ns

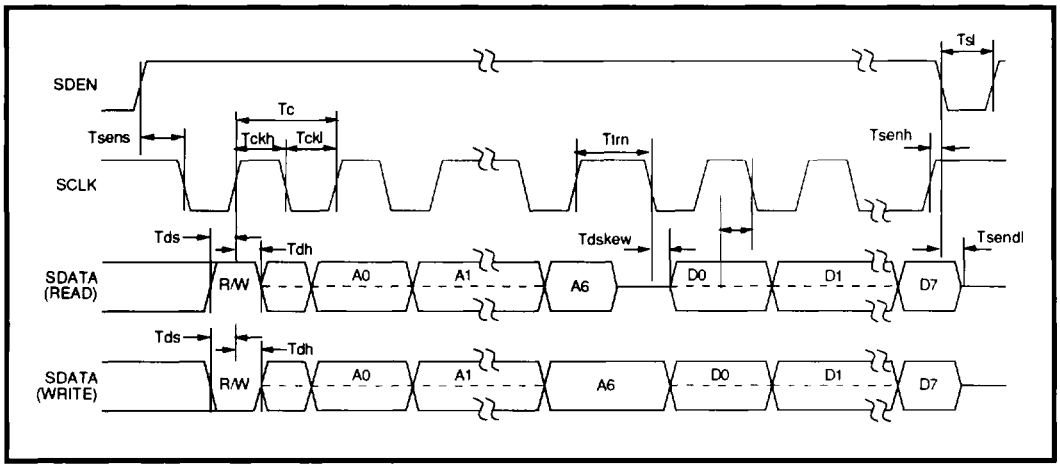

FIGURE 16(b): Serial Port Timing

PULSE DETECTOR CHARACTERISTICS

AGC AMPLIFIER

Input signals are AC coupled to VIA/$\overline{\text{VIA}}$, VOA/$\overline{\text{VOA}}$ outputs are AC coupled to IN/$\overline{\text{IN}}$, and ON/$\overline{\text{ON}}$ are AC coupled to DP/DN. A 1000 pF capacitor (CBYP) is connected from BYP to VPG. Unless otherwise specified, outputs are measured differentially at VOA/$\overline{\text{VOA}}$, FIN = 8 MHz, and filter boost = 0 dB.

PARAMETER	CONDITION		MIN	NOM	MAX	UNIT
Input range	Fin = Fc	0 dB boost	22		240	mVp-p
		13 dB boost	20		100	mVp-p
DP-DN voltage	22 ≤ VIA-$\overline{\text{VIA}}$ ≤ 240 mVp-p $\overline{\text{HOLD}}$ = 1, boost = 0 dB		0.85		1.15	Vp-p
	20 ≤ VIA-$\overline{\text{VIA}}$ ≤ 100 mVp-p $\overline{\text{HOLD}}$ = 1, boost = 13 dB		0.85		1.15	Vp-p
DP-DN voltage (servo)	SG = 1, DACA = 0000		1	1.2	1.4	Vp-p
	SG = 1, DACA = 1111		0.6	0.8	1	Vp-p
Differential input impedance	WG = low		4.7	6	8.4	kΩ
	WG = high; or Low-Z		100	350	600	Ω
Single-ended input impedance	WG = low		2.5	3.6	5	kΩ
	WG = high; or Low-Z		20	150	400	Ω
Input noise voltage	Gain = 22, VIA/$\overline{\text{VIA}}$ are shorted			8	15	nV/√Hz
CMRR	Gain = 22, F = 5 MHz		40			dB
PSRR	Gain = 22, Fc = 5MHz		45			dB
Single-ended output resistance				65	275	Ω

ELECTRICAL SPECIFICATIONS (continued)

AGC CONTROL

The input signals are AC coupled into DN/DP, CBYP = 1000 pF to VPA. CT = 10000 pF, RTS = RTD = open.

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Decay current	VBYP = VPG - 2.3V, DP-DN = 0V Normal decay (ID)	-3	-4	-7	µA
	Fast decay mode (IDF)	-0.8	-1.2	-1.7	mA
Attack current	VBYP = VPG - 2.3V Normal attack (ICH) DP-DN = 0.55V	0.12	0.17	0.29	mA
	Fast attack mode (ICHF) DP-DN = 0.675V	7 • ICH	8 • ICH	11 • ICH	mA
BYP leakage current	$\overline{HOLD}$ = 0, 1 ≤ Gain ≤ 22	-100		+100	nA
Low-Z duration	WG 1 to 0 Low-Z bit = 0	0.5	1	1.5	µs
	Low-Z bit = 1		2		µs
Fast decay duration	Low-Z bit = 0	0.5	1	1.5	µs
	Low-Z bit = 1		2		µs
LEVEL output voltage (with respect to RTD/RTS)	FIN = 6 to 18 MHz |DP-DN| = 0.5	0.28	0.33	0.38	V/Vp-p
	|DP-DN| = 1	0.60	0.67	0.74	V/Vp-p
	|DP-DN| = 1.5	0.85	1	1.1	V/Vp-p
LEVEL pull-down current	Vlevel = VPG - 2.3V	35	60	85	µA

DATA COMPARATOR

The input signals are AC coupled into DP/DN.

Differential input resistance	WG = 0	3	5	7	kΩ
Single-ended input resistance	WG = 1	250	600	1200	Ω
Threshold (T%) accuracy	48 < VTHDAC < 127 0.3 ≤ VLEVEL - VRTD ≤ 0.75 T% = (84.5 x VTHDAC/127) -2.17%	T% - 5		T% + 5	%

CLOCK SECTION

The input signals are AC coupled into CP/CN.

Differential input resistance		3	5	7	kΩ
Pulse pairing	Data threshold register = 196 and 63. Measured at the falling edge of $\overline{RDIO}$ Fc = 9 MHz, 0 dB boost VIA = 100 mVp-p @6 MHz			0.6	ns

SERVO CAPTURE CHARACTERISTICS

Unless otherwise specified: a 4 MHz sine wave is AC-coupled into DP/DN inputs; STROBE and $\overline{\text{RESET}}$ durations are 1 µs; and DACP is set to "1000."

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
MAXREF output voltage 32P4752	ISOURCE = 1 mA	2.9	3.1	3.3	V
MAXREF load regulation 32P4752	ISOURCE = -1 to -4 mA			40	mV
A, B, C, D output low voltage 32P4752	ISINK = 0.2 mA $\overline{\text{RESET}}$ = 0	0.14 x MAXREF	0.17 x MAXREF	0.18 x MAXREF + 0.15	V
MAXREF + A,B,C,D high voltage 32P4752	ISOURCE = 0 mA	0		VPG - 2	V
A, B, C, D output resistance 32P4752	ISOURCE/SINK = 0.2 mA			50	Ω
A, B, C, D gain 32P4752	0.2 Vp-p < (DP - DN) ≤ 1 Vp-p	2	2.15	2.35	V/V
A, B, C, D offset voltage		0		100	mV
SREF input range 32P4756		0.35 x VPG	0.4 x VPG	0.55 x VPG	V
SREF input bias current 32P4756	0.35 • VPG ≤ SREF ≤ 0.55 • VPG		0.2	1	µA
A-B, C-D, A+B high voltage 32P4756		VPG - 0.75			V
A-B, C-D, A+B low voltage 32P4756				0.5	V
A-B, C-D gain	0.2 Vp-p < (DP - DN) ≤ 1 Vp-p	1.8	2	2.2	V/V
32P4756	0 Vp-p ≤ (DP - DN) ≤ 0.2 Vp-p	0		2.2	V/V
A+B gain	0.2 Vp-p < (DP - DN) ≤ 1 Vp-p	0.9	1	1.1	V/V
32P4756	0 Vp-p ≤ (DP - DN) ≤ 0.2 Vp-p	0		1.1	V/V
A-B, C-D, offset voltage 32P4756	DP/DN = 0.5 Vp-p Offset = |output ($\overline{\text{RESET}}$ = 0) - output ($\overline{\text{RESET}}$ = 1)|			30	mV
Burst capture time 32P4752/4756	DP - DN = 1 Vp-p Output ≥ 95% of final value			1	µs
Burst reset time 32P4752/4756	DP - DN = 1 Vp-p Output ≤ 5% of final value			1	µs
$\overline{\text{RESET}}$ on/off delay	From $\overline{\text{RESET}}$ 1.4V crossing			150	ns
$\overline{\text{RDIO}}$ pulse width	CL = 15 pF Measured at 1.5V crossing	20	26	50	ns
PPOL to $\overline{\text{RDIO}}$ setup time	PPOL rise/fall to $\overline{\text{RDIO}}$ fall measured @ 1.5V crossing, CL ≤ 15 pF	8			ns

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ELECTRICAL SPECIFICATIONS (continued)

PROGRAMMABLE FILTER CHARACTERISTICS

Unless otherwise specified: Rx = 12.1 kΩ, Cx = 1000 pF from Rx pin to VNG. Input signals are AC-coupled into IN/$\overline{IN}$.

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Filter cutoff range	Fc @ -3 dB point Fc = 0.2223 • FC -1.2348 MHz 46 ≤ FC ≤ 127 Boost = 0 dB, i.e. FB = 0	9		27	MHz
Filter cutoff accuracy	9 ≤ Fc ≤ 27 MHz	-15		+15	%
Normal Gain (ON/IN)	Fin = 0.67 Fc, 0 dB boost 9 ≤ Fc ≤ 27 MHz	1.5	2	2.4	V/V
Differentiated Gain Ratio (OD/ON)	Fin = 0.67 Fc, 0 dB boost 9 ≤ Fc ≤ 27 MHz	0.8		1.2	V/V
Boost @ Fc	0 ≤ FBDAC ≤ 127	0		13	dB
Boost accuracy (See Boost Formula)	@ 6 dB @ 9 dB @ 13 dB	-1.25 -1.5 -2		+1.25 +1.5 +2	dB dB dB
Differentiated Output THD	Fin = 0.67 Fc, 0 dB boost Rload = 10 kΩ differential ODP/ODN = 1 Vp-pd			1.5	%
Output noise voltage differentiated output	BW = 100 MHz, Rs = 50Ω Fc = 27 MHz boost = 0 dB		4	6.5	mVrms
	boost = 13 dB		10	17	mVrms
normal output	boost = 0 dB		2.9	3.5	mVrms
	boost = 13 dB		4	7	mVrms
Filter output sink current		0.5			mA
Filter differential input resistance	WG = low	3	5	7	kΩ
	WG = high	0.8	1.1	1.6	kΩ
Filter output resistance	single ended		100	200	Ω
Rx pin voltage*	Ta = 27°C, for reference use only		680		mV
Filter output offset voltage (Normal, Differentiated outputs)	Fc = 9 - 27 MHz Boost = 0 - 13 dB IN and $\overline{IN}$ shorted	-115		+115	mV
Group Delay Variation Δ % = 0% (FG = 0)	Fc = 27 MHz 0.2 Fc ≤ Fin ≤ Fc	-850		850	ps
Δ % = 0% (FG = 0)	Fc = 9 to 27 MHz 0.2 Fc ≤ Fin ≤ Fc	-2		+2	%
Δ % = 0% (FG = 0)	Fc = 9 to 27 MHz Fc ≤ Fin ≤ 1.75 Fc	-3		+3	%

PROGRAMMABLE FILTER CHARACTERISTICS (continued)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Group Delay Variation Δ % = 30% (FG = 255)	Fc = 27 MHz Fin = 1 MHz	25	30	35	%
Δ % = -30% (FG = 127)	Fc = 27 MHz Fin = 1 MHz	-35	-30	-25	%
Δ % = 30% (FG = 255)	Fc = 9 MHz Fin = 1 MHz	25	30	35	%
Δ % = -30% (FG = 127)	Fc = 9 MHz Fin = 1 MHz	-35	-30	-25	%
Δ % = 15% (FG = 192)	Fc = 27 MHz Fin = 1 MHz	10	15	20	%
Δ % = -15% (FG = 64)	Fc = 27 MHz Fin = 1 MHz	-20	-15	-10	%
Δ % = 15% (FG = 192)	Fc = 9 MHz Fin = 1 MHz	10	15	20	%
Δ % = -15% (FG = 64)	Fc = 9 MHz Fin = 1 MHz	-20	-15	-10	%

TIME BASE GENERATOR CHARACTERISTICS

Unless otherwise specified: RR = 12.1 kΩ. Loop filter values are R = 1.8k, C1 = 10,000 pF, and C2 = 1,000 pF. Clock source is AC coupled into FREF, 1.5 ≤ VREF ≤ 2 Vp-p

FREF input range	TRISE/TFALL ≤ 5 ns	8		25	MHz
FREF input low time		20			ns
FREF input high time		20			ns
M counter range	Reference only	2		255	
N counter range	Reference only	2		127	
Output frequency	FREF = 20 MHz	96			MHz
Output jitter	≥ 10K samples		180		psec(RMS)
VCO center frequency FTBG	TFLT - $\overline{\text{TFLT}}$ = 0V FTBG = [12.5/(RR + 0.4)] [(0.715 • IDAC) + 6.8] MHz	0.85 • FTBG		1.15 • FTBG	MHz
VCO dynamic range	-2V < TFLT - $\overline{\text{TFLT}}$ < +2V FVCO = 96 MHz MAX	±25		±45	%

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ELECTRICAL SPECIFICATIONS (continued)

TIME BASE GENERATOR CHARACTERISTICS

Unless otherwise specified: RR = 12.1 kΩ. Loop filter values are R = 1.8k, C1 = 10,000 pF, and C2 = 1,000 pF. Clock source is AC coupled into FREF, 1.5 ≤ VREF ≤ 2 Vp-p

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
VCO control gain	KVCO	$\omega i = 2\pi \cdot FVCO$ $-1V \leq TFLT - \overline{TFLT} \leq +1V$	0.12 ωi	0.175 ωi	0.24 ωi	rad/(V-S)
Phase detector gain	KD	KD = [12.5/(RR + 0.4)] • [0.636 • IDAC + 0.875] NCTR D7 = 1, KD = 1x NCTR D7 = 0, KD = 3x	0.82 • KD		1.18 • KD	µA/rad
KVCO • KD product accuracy			-25		+25	%

DATA SEPARATOR CHARACTERISTICS

Unless otherwise specified, RR = 12.1 kΩ. Loop filter components are R = 1.82k, C1 = 1000 pF, and C2 = 100 pF. Data Rate = 64 Mbit/s.

READ MODE

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
Read clock rise time	TRRC	0.8 to 2V, CL ≤ 15 pF			5	ns
Read clock fall time	TFRC	2 to 0.8V, CL ≤ 15 pF			5	ns
RRC duty cycle	TRD	1.5V - 1.5V, CL ≤ 15 pF	40		70	%
NRZ set-up/hold	TNS/TNH		10			ns
NRZ propagation delay	TPNRZ	From RRC to NRZ out		3		ns
Phase Window Centering		At 18 and 64 Mbit/s Difference between early, late phase reversal points / phase window	-20		+20	%

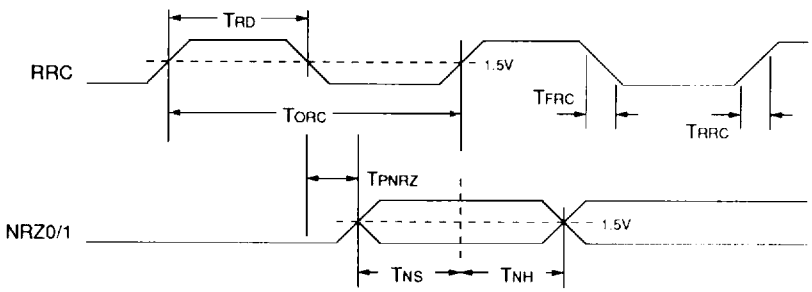

FIGURE 18: NRZ Read Timing

DATA SEPARATOR CHARACTERISTICS (continued)

WRITE MODE

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
WD/$\overline{WD}$ rise time	TRWD	20% to 80%, CL ≤ 15 pF			5	ns
WD/$\overline{WD}$ fall time	TFWD	80% to 20%, CL ≤ 15 pF			5	ns
Write Data jitter		WD out = fixed 2T pattern			500	psec
Required WCLK rise time	TRWC	0.8 to 2V			10	ns
Required WCLK fall time	TFWC	2 to 0.8V			8	ns
NRZ set-up time	TSNRZ		5			ns
NRZ hold time	THNRZ		5			ns
WD/$\overline{WD}$ pulse width	TWD	Without precomp, TW = 1/FTBG CL ≤ 15 pF	0.82 • TW		1.18 • TW	ns
Write Precomp magnitude shift accuracy		TPCO = 0.0459/FTBG + 0.003 TPC = n • TPCO 0 ≤ n ≤ 7	0.8 • TPC - 1.5		1.2 • TPC + 1.5	ns

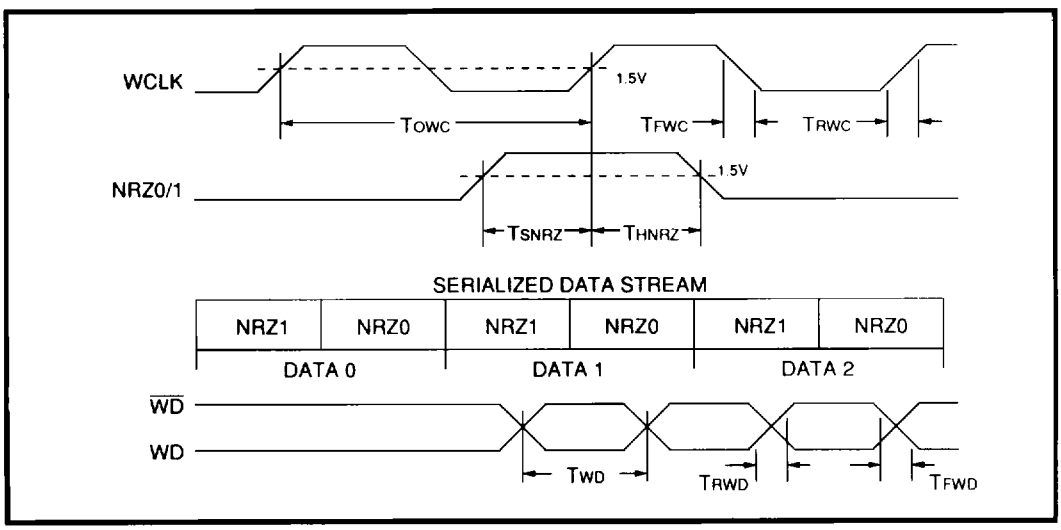

FIGURE 19: $\overline{WD}$ and NRZ Write Timing

DATA SYNCHRONIZATION

Unless otherwise specified: RR = 12.1 kΩ. Loop filter values are R = 1.82k, C1 = 1000 pF, and C2 = 100 pF. Clock source is AC coupled into FREF, 1.5 ≤ VFREF ≤ 2 Vp-p.

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
VCO center frequency FVCO	DFLT - $\overline{\text{DFLT}}$ = 0V FVCO = [12.5/(RR+0.4)] [(0.715 • IDAC) + 6.8] MHz	0.85 • FVCO		1.15 x FVCO	MHz
VCO dynamic range	-2V < DFLT - $\overline{\text{DFLT}}$ < +2V at 96 MHz MAX	±25		±45	%
VCO control gain KVCO	ωi = 2π/TVCO -1V < DFLT- $\overline{\text{DFLT}}$ < +1V	0.12 ωi	0.175 ωi	0.24 ωi	rad/(V-S)
Phase detector gain KD	KD = [12.5/(RR + 0.4)] • [0.636 • IDAC + 0.875] RG = 1, gain shift: KD = 1x RG = 1, no gain shift: KD = 3x RG = 0: KD = 1x	0.82 • KD		1.18 • KD	µA/rad
KVCO • KD product accuracy		-28		+28	%
VCO phase restart error		-1		1	ns
Decode window center accuracy	Based on 50% error points at 64 Mbit/s	-0.5		+1.5	ns
Decode window loss	Based on 15% and 50% error rate Data rate = 64 Mbit/s			750	ps
Decode window skew		-1		+1	ns
Decode window shift magnitude accuracy	TWSO = 0.0223/FVCO TWS = n • TWSO 0 ≤ n ≤ 15	0.8 • TWS - 1.5		1.2 • TWS + 1.5	ns

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ELECTRICAL SPECIFICATIONS (continued)

WINDOW SHIFT CONTROL

Window shift magnitude is set by the value in the Window Shift (WS) register. The WS register bits are as follows:

BIT	NAME	FUNCTION
0	$\overline{WS0}$	
1	$\overline{WS1}$	
2	$\overline{WS2}$	
3	$\overline{WS3}$	
4	WSD	Window shift direction. 0 = early, 1 = late
5	WSE	Window shift enable
6	TDAC0	Used to route signals to DAC test point
7	TDAC1	Used to route signals to DAC test point

The window shift magnitude is set as a percentage of the decode window, in 2.23% steps. Window shift should be set during non-read mode.

$\overline{WS3}$	$\overline{WS2}$	$\overline{WS1}$	$\overline{WS0}$	SHIFT MAGNITUDE
1	1	1	1	No shift
1	1	1	0	2.23% (minimum shift)
1	1	0	1	4.46%
1	1	0	0	6.69%
1	0	1	1	8.92%
1	0	1	0	11.15%
1	0	0	1	13.38%
1	0	0	0	15.61%
0	1	1	1	17.84%
0	1	1	0	20.07%
0	1	0	1	22.3%
0	1	0	0	24.53%
0	0	1	1	26.76%
0	0	1	0	28.99%
0	0	0	1	31.22%
0	0	0	0	33.45% (maximum shift)

WRITE PRECOMP CONTROL

Write precomp magnitude is set by the value in the write precomp (WP) register. The WP register bits are as follows:

BIT	NAME	FUNCTION	BIT	NAME	FUNCTION
0	$\overline{WE0}$	Early bit 0	4	$\overline{WL0}$	Late bit 0
1	$\overline{WE1}$	Early bit 1	5	$\overline{WL1}$	Late bit 1
2	$\overline{WE2}$	Early bit 2	6	$\overline{WL2}$	Late bit 2
3	WPE	Write precomp enable			

The write precomp magnitude is calculated as:

$$TPC = n \cdot 0.0459 \cdot T_{TBG} + 0.003$$

or $$TPC = (7 - \overline{WL}) \cdot 0.0459 \cdot T_{TBG} + 0.003$$

$$(7 - \overline{WE}) \cdot 0.0459 \cdot T_{TBG} + 0.003$$

where n = precomp magnitude scaling factor as shown below. T_{TBG} is the period of the TBG output.

$\overline{W2}$	$\overline{W1}$	$\overline{W0}$	PRECOMP MAGNITUDE SCALING FACTOR
1	1	1	No precomp
1	1	0	1X
1	0	1	2X
1	0	0	3X
0	1	1	4X
0	1	0	5X
0	0	1	6X
0	0	0	7X (maximum)

BIT N-2	BIT N-1	BIT N	BIT N+1	BIT N+2	BIT N COMPENSATION
1	0	1	0	1	None
0	0	1	0	0	None
1	0	1	0	0	Early
0	0	1	0	1	Late

Late = Bit N is time shifted toward the N+1 bit by the programmed magnitude
Early = Bit N is time shifted toward the N-1 bit by the programmed magnitude

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ELECTRICAL SPECIFICATIONS (continued)

TABLE 6: 1,7 RLL ENCODE TABLE (X = Don't care)

NRZ DATA				ENCODED WRITE DATA			
Present Bits		Next Bits	Previous		Present		
NRZ1	NRZ0	NRZ1'	NRZ0'	Y3	Y1	Y2	Y3
0	0	0	X	X	0	0	1
0	0	1	X	0	0	0	0
0	0	1	X	1	0	1	0
1	0	0	X	X	1	0	1
1	0	1	X	X	0	1	0
0	1	0	0	0	0	0	1
0	1	0	0	1	0	1	0
0	1	1	0	X	0	0	0
0	1	0	1	0	0	0	1
0	1	0	1	1	0	0	0
0	1	1	1	X	0	0	0
1	1	0	0	0	0	1	0
1	1	1	0	0	1	0	0
1	1	0	1	0	1	0	0
1	1	1	1	0	1	0	0

TABLE 7: 1,7 RLL DECODE TABLE (X = Don't care)

ENCODED READ DATA					DECODED DATA				
Previous		Present		Next					
Y2'	Y3'	Y1	Y2	Y3	Y1	Y2	NRZ1	NRZ0	
0	0	0	0	0	X	X	0	1	
1	0	0	0	0	X	X	0	0	
0	1	0	0	0	X	X	0	1	
X	X	1	0	0	X	X	1	1	
X	0	0	1	0	0	0	1		
X	0	0	1	0	1	0	1	0	
X	0	0	1	0	0	1	1	0	
X	1	0	1	0	0	0	0	1	
X	1	0	1	0	1	0	0	0	
X	1	0	1	0	0	1	0	0	
0	0	0	0	1	X	X	0	1	
1	0	0	0	1	X	X	0	0	
0	1	0	0	1	X	X	0	0	(Preamble)
X	X	1	0	1	X	X	1	0	

TABLE 8: CLOCK SOURCE AND FREQUENCY VS. MODE

WG	RG	VCO REF	RCLK	DECODE CLOCK	ENCODE CLOCK	MODE
0	0	FOUT	2FOUT/3	FOUT	FOUT	IDLE
0	1	$\overline{DRD}$	2VCO/3	VCO	FOUT	READ
1	0	FOUT	2FOUT/3	FOUT	FOUT	WRITE

NOTE 1: Until the VCO locks to the new source, the VCO entries will be FOUT.

NOTE 2: Until the VCO locks to the new source, the 2VCO/3 entries will be 2FOUT/3.

TABLE 9: MULTIPLEXED TEST POINT SIGNAL SELECTION

MTPEn	TMS1	TMS0	MTP1	MTP2	MTP3	(MTP4)*
0	X	X	OFF	OFF	OFF	OFF
1	0	0	VCOREF	DSIN	SRD	N/C
1	0	1	RD	DOUT	DSREF	MCTR
1	1	0	PDQ	PUQ	SRD	N/C
1	1	1	SET	RESET	NCTR	MCTR

DOUT = Output of the pulse qualifier data comparators

DSIN = Input to the data synchronizer phase detector: delayed read data output (read mode) TBG output (non-read mode)

DSREF = Output of the time base generator

MCTR = M counter output of TBG

NCTR = N counter output of the time base generator

PDQ = Data separator phase detector pump down edge

PUQ = Data separator phase detector pump up edge

RD = Read data output from the pulse qualifier

RESET = Output of the negative threshold comparator

SET = Output of the positive threshold comparator

SRD = Synchronized read data

VCOREF = Data separator VCO reference clock

* Internal test point

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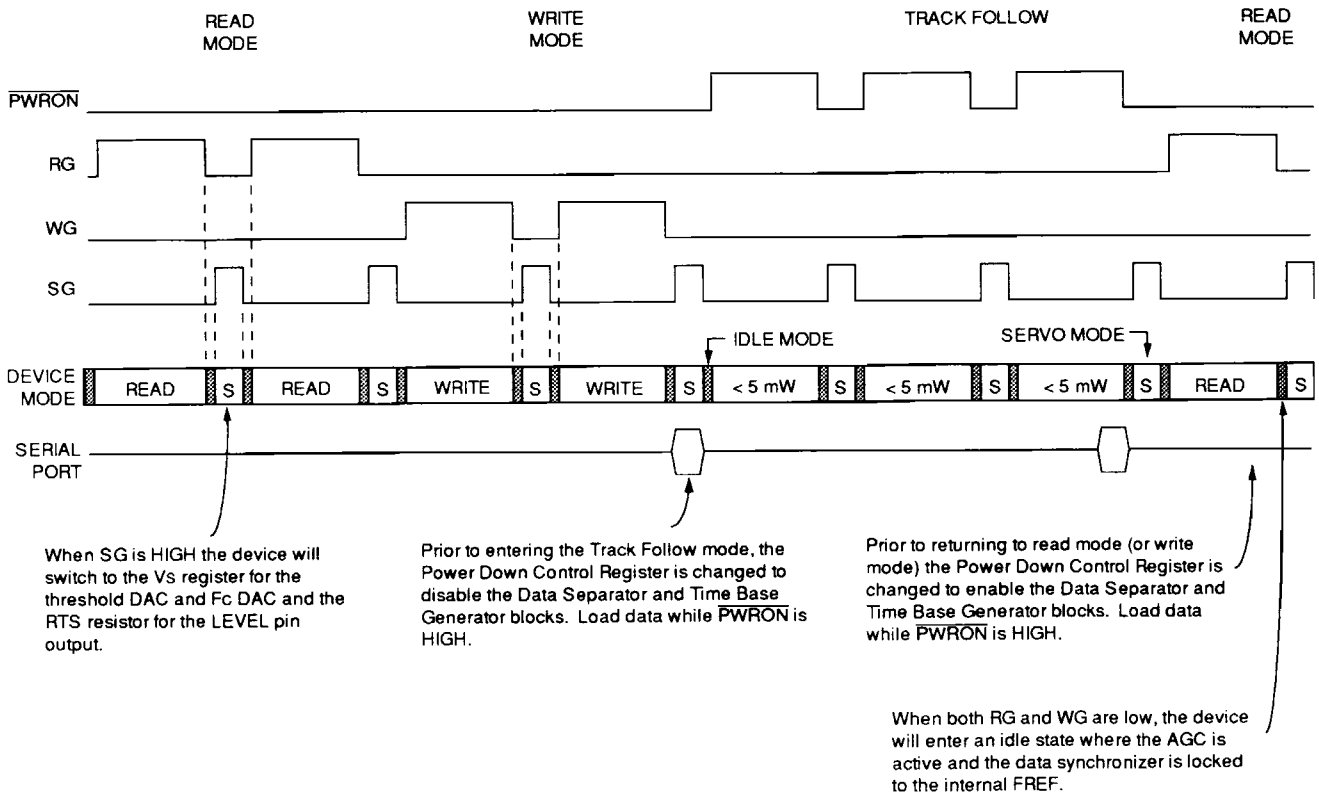

NOTES:

1) When the PWRON pin is LOW ("0") the Power Down Control Register is active. All blocks that have their control bit set to "1" will be powered down. When the PWRON pin is HIGH ("1") the device goes into a sleep mode with all blocks powered down except the serial port.

2) When the threshold DAC reference is switched, there is a maximum settling time of 1.5 µs for the DAC.

FIGURE 20: Power Control Timing

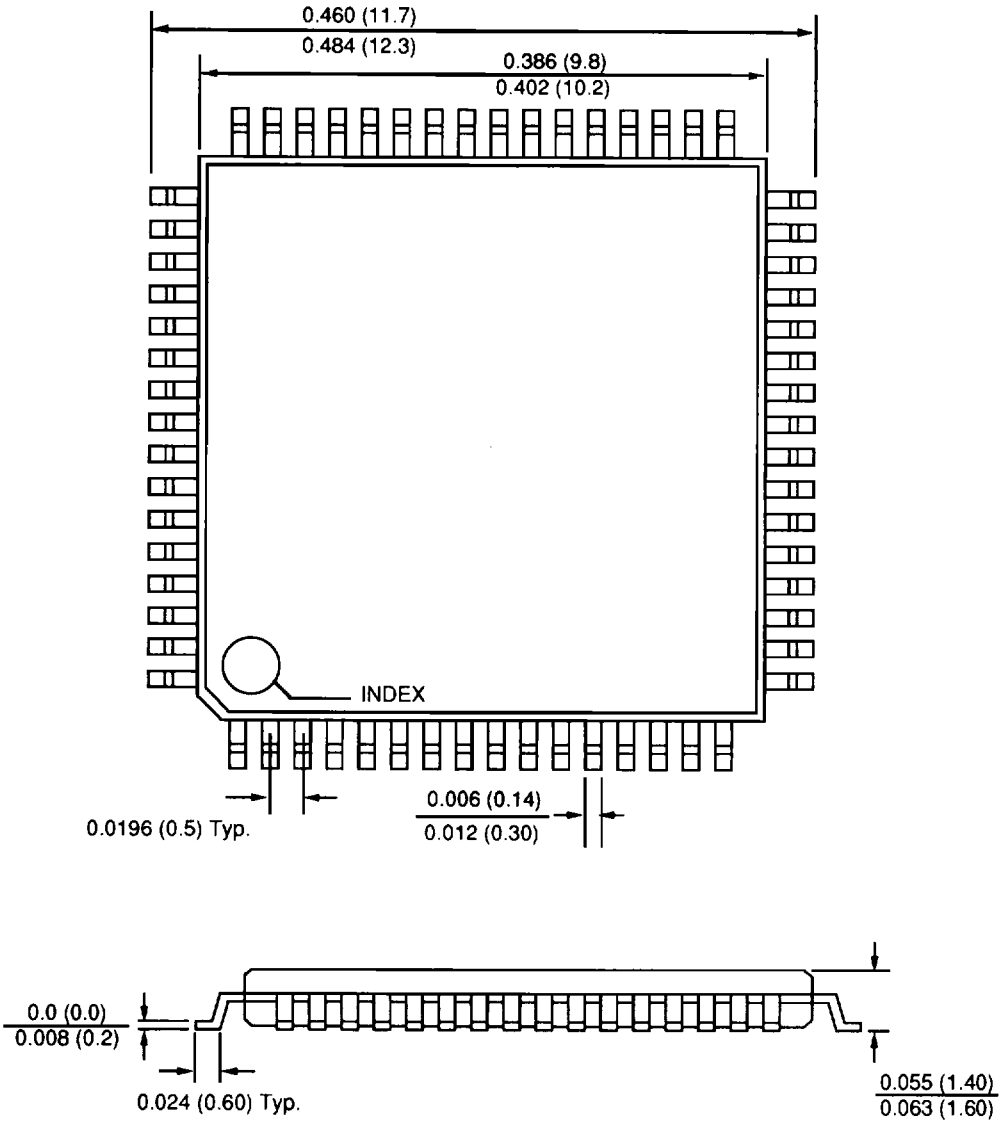

FIGURE 21: Package Information
64-Lead Thin Quad Flatpack (TQFP)

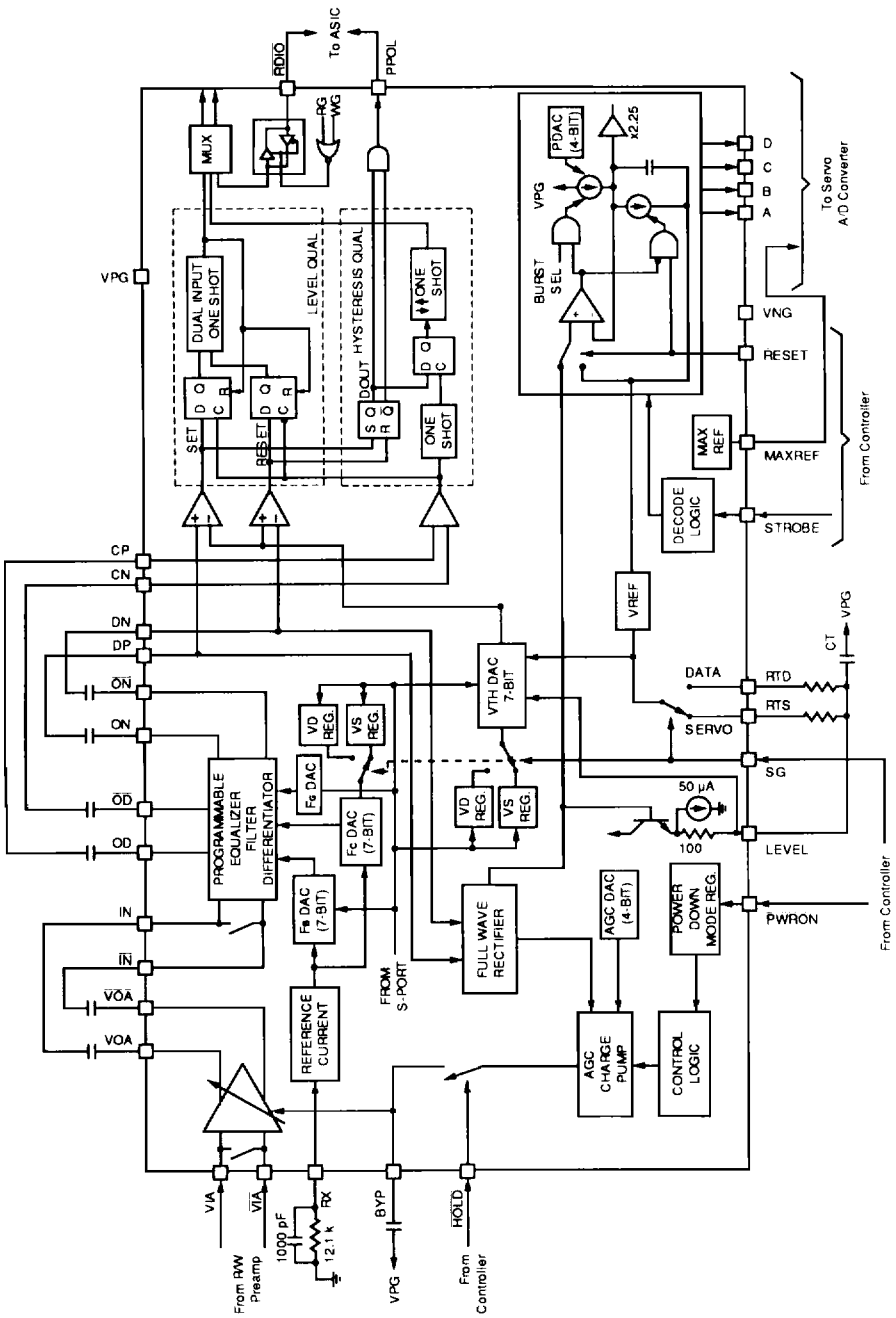

FIGURE 22(a): 32P4752 Application Diagram

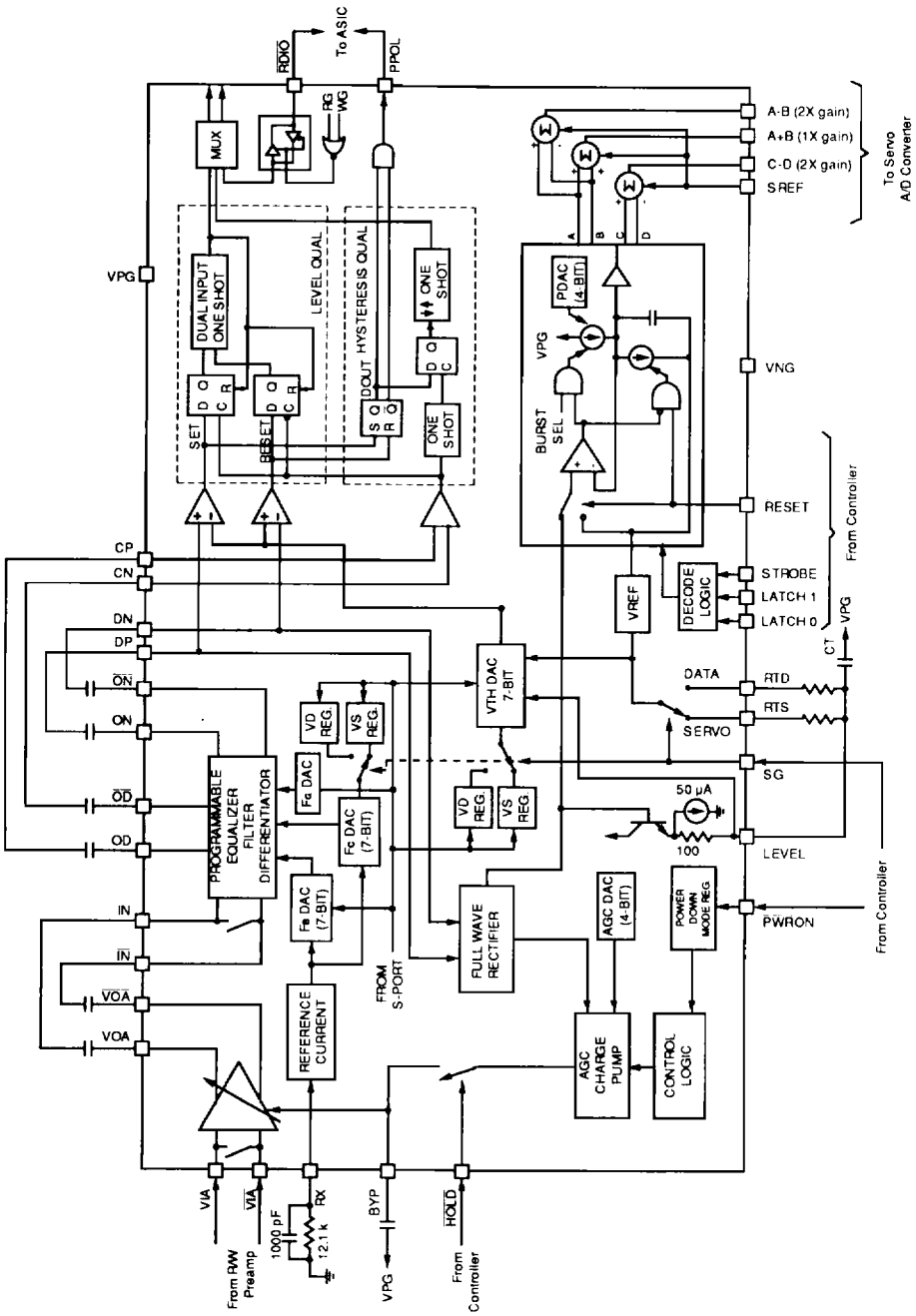

FIGURE 22(b): 32P4756 Application Diagram

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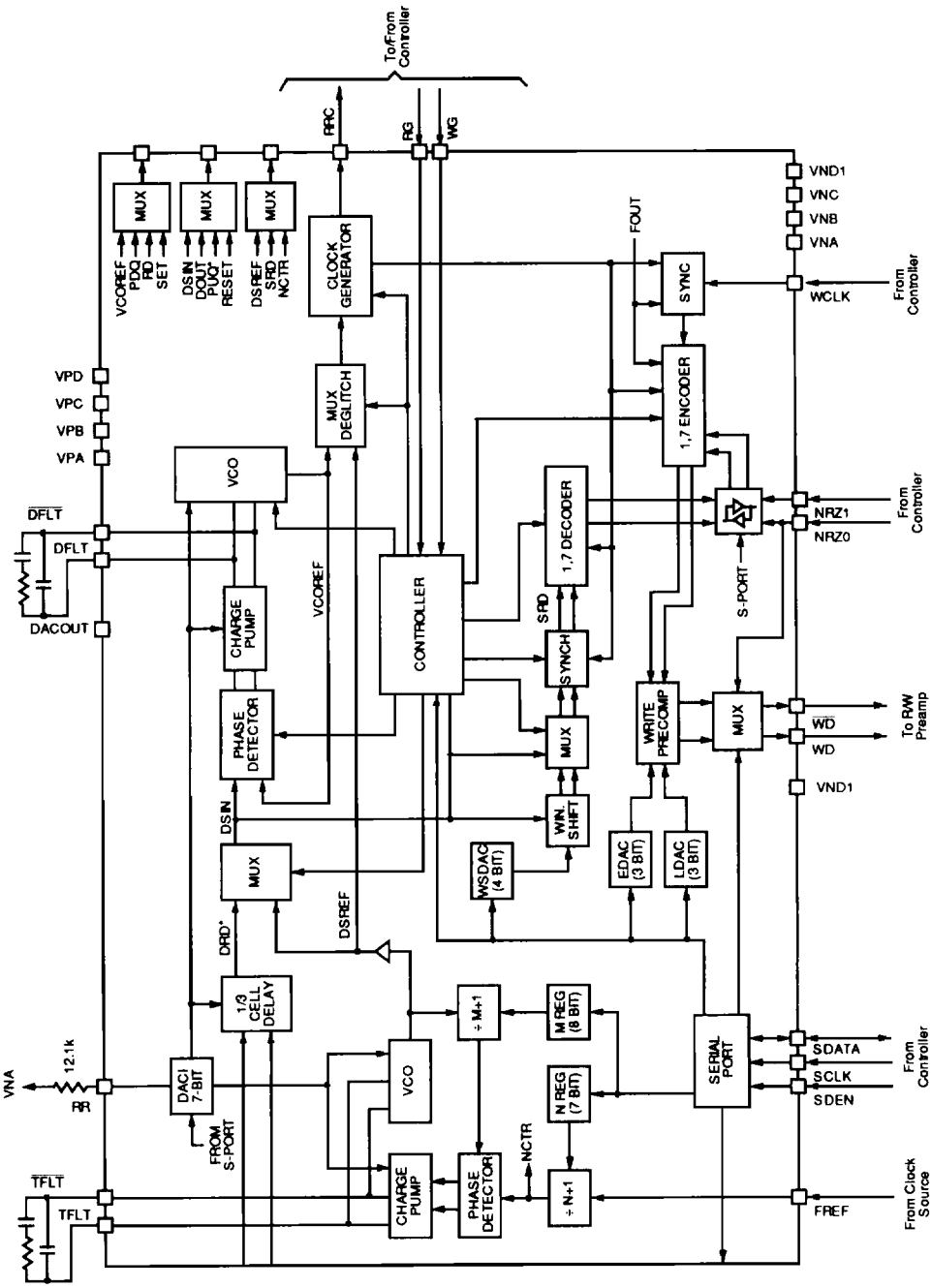
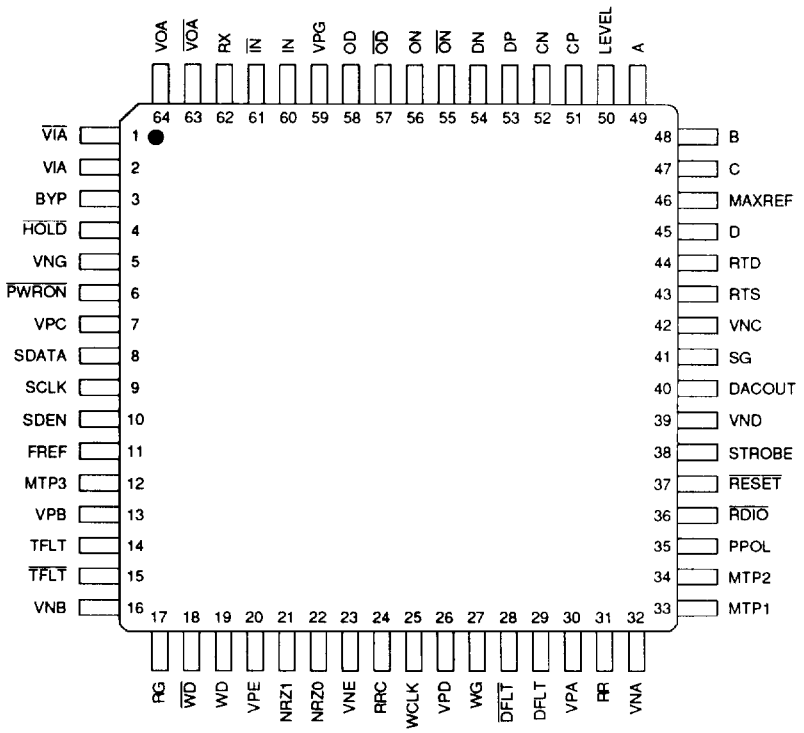


FIGURE 22(c): 32P4752/4756 Application Diagram

PACKAGE PIN DESIGNATIONS
(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.



32P4752
64-Lead TQFP

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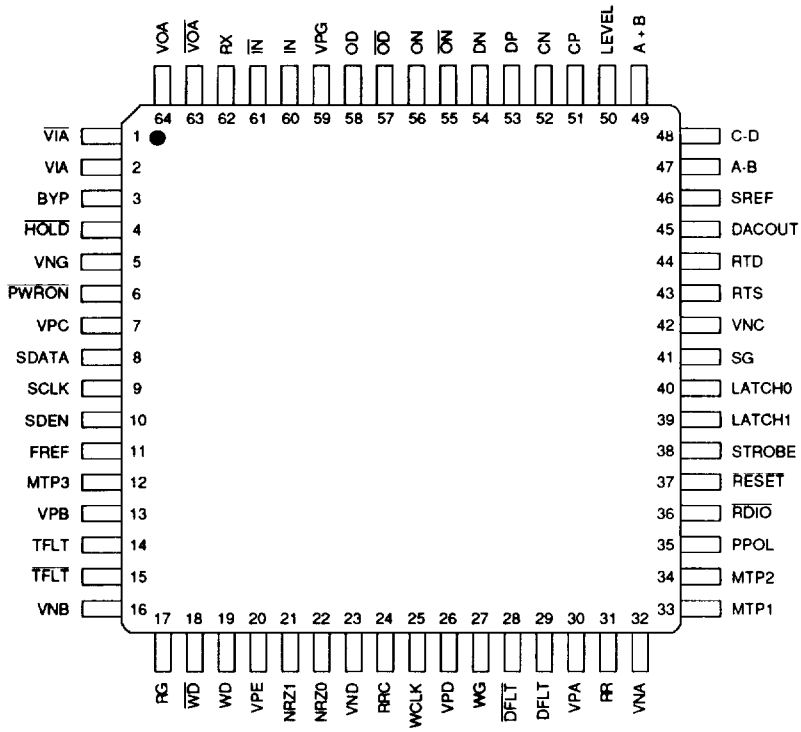
SSI 32P4752/4756
Read Channel with
1,7 ENDEC, 4-burst Servo

PACKAGE PIN DESIGNATIONS
(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.



32P4756
64-Lead TQFP

ORDERING INFORMATION

PART DESCRIPTION		ORDER NUMBER	PACKAGE MARK
SSI 32P4752	64-Lead TQFP	32P4752-CGT	32P4752-CGT
SSI 32P4756	64-Lead TQFP	32P4756-CGT	32P4756-CGT

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