

FAST 74F1894, 1895, 1896, 1897 Transceiver with Parity Error

FAST Products

FEATURES

- Similar to 74F657 functions except:
 - continuously checks A port Parity
 - has internal parity error latch/reg
 - has parity bit carry through
- Error output continuously checks A port Parity
- High Impedance NPN base input for reduced loading (70µA In High and Low states)
- Ideal in applications where High output drive and light bus loading are required (I_{IL} is 70µA vs FAST std of 600µA)
- 3-state B Port outputs sink 64mA
- Input diodes for termination effects
- 28 pin plastic Slim Dip (300mil) package

DESCRIPTION

The 74F1894-97 are 9-bit transceivers featuring non-inverting buffers with 3-state outputs [F1894, F1896] or open collector outputs [F1895, F1897] and a latched [F1894, F1895] or registered [F1896, F1897] 8-bit even parity error generator, and are intended for bus-oriented applications. The B port outputs are all capable of sinking 64mA and sourcing up to 15mA, producing very good capacitive drive characteristics. The A port outputs have a guaranteed current sinking capability of 24mA and source 3mA. The Direc-

F1894 - 9-Bit Transceiver With Latched 8-Bit Parity Error (OC)

F1895 - 9-Bit Transceiver With Latched 8-Bit Parity Error (3-State)

F1896 - 9-Bit Transceiver With Registered 8-Bit Parity Error (OC)

F1897 - 9-Bit Transceiver With Registered 8-Bit Parity Error (3-State)

Preliminary Specification

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F1894,95,96,97	8.0ns	100mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0^\circ C$ to $+70^\circ C$
28-Pin Plastic Slim DIP (300 mil)	N74F1894N,95N,96N,97N
28-Pin Plastic SOL ¹	N74F1894D,95D,96D,97D

NOTE 1: Thermal mounting techniques are recommended. See SMD Process Applications (page 17) for a discussion of thermal consideration for surface mounted devices.

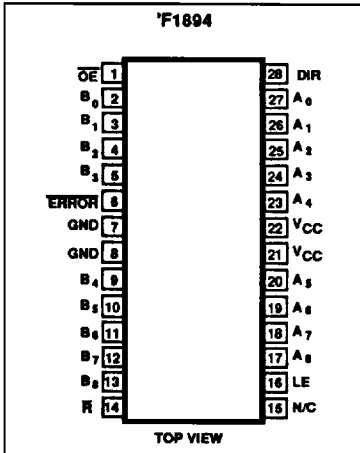
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$A_0 - A_7$	A port 3-state inputs	3.5/0.117	70µA/70µA
$B_0 - B_7$	B port 3-state inputs	3.5/0.117	70µA/70µA
\bar{R}	ERROR Latch/Register Reset input	1.0/0.033	20µA/20µA
LE	Latch Enable input (F1894, 95 only)	1.0/0.033	20µA/20µA
CP	Register Clock input (F1896, 97 only)	1.0/0.033	20µA/20µA
DIR	A-to-B, B-to-A Direction input	2.0/0.066	40µA/40µA
\bar{OE}	A/B Output Enable input (active Low)	2.0/0.066	40µA/40µA
\bar{EOE}	Error Output Enable input (F1895, 97 only)	1.0/0.033	20µA/20µA
$A_0 - A_7$	A port 3-state outputs	150/40	3.0mA/24mA
$B_0 - B_7$	B port 3-state outputs	750/106.7	15mA/64mA
ERROR	Even Parity Error output (3-state*or OC)	750*/106.7	15mA*/64mA

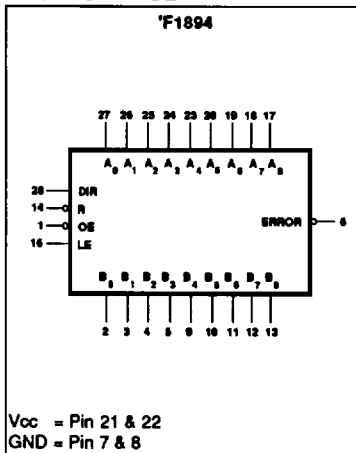
NOTE:

One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION

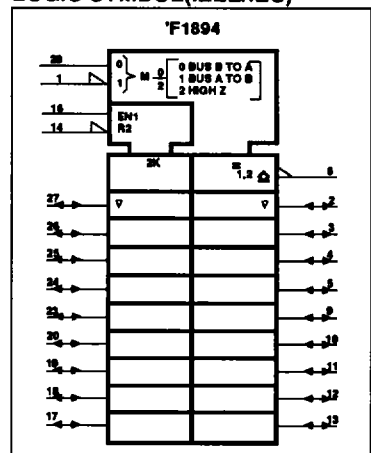


LOGIC SYMBOL



V_{CC} = Pin 21 & 22
GND = Pin 7 & 8

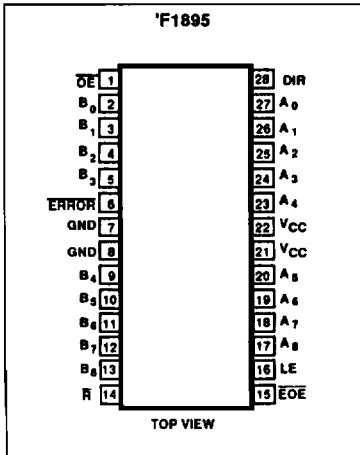
LOGIC SYMBOL (IEEE/IEC)



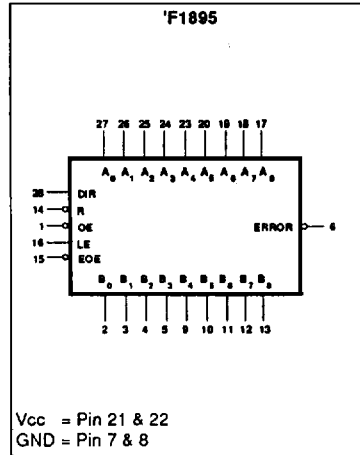
Transceiver with Parity Error

FAST 74F1894, F1895, F1896, F1897

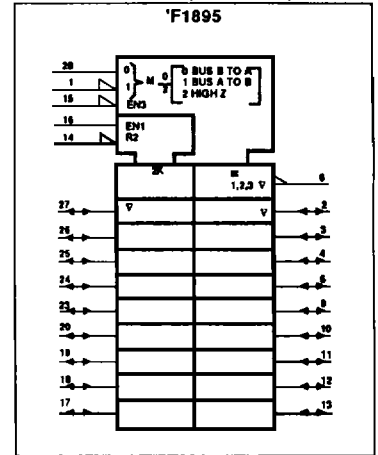
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



tion [DIR] input determines the direction of data flow through the bidirectional transceivers. Active-Low enables data from A ports to B ports; Active-High enables data from B ports to A ports.

The error (ERROR) pin is an output from the even parity checker connected to port A. If the number of High bits on port A is odd, then the error (ERROR) output will be Low, indicating bad (or odd) parity. If the number of High bits on port A is even, then the error (ERROR) output will be High, indicating even parity.

The F1894 & F1895 have a transparent latch on the error (ERROR) output. The latch is transparent (data passes through) when the latch enable (LE) pin is High. The data is latched on the error (ERROR) output when the latch enable (LE) pin is Low. If an error has occurred and is latched, the error (ERROR) output will remain Low until the latch becomes transparent or is cleared with a Low on the reset input (R) pin.

The F1896 & F1897 have a D flip-flop

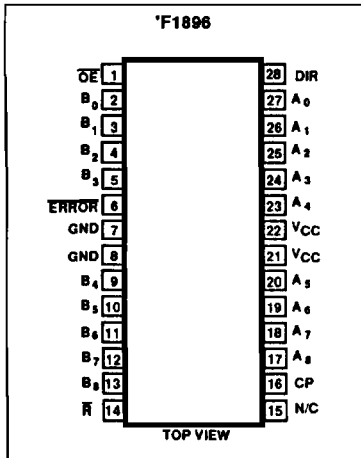
register on the error (ERROR) output. The data is entered into the register on the rising edge of the register clock input (CP) pin. If an error has occurred, the error (ERROR) output will remain Low until the register is cleared with a Low on the reset (R) input.

The F1895 & F1897 also have an error output enable (EOE) pin. When error output enable (EOE) is Low, the error (ERROR) output is enabled. When error output enable (EOE) is High, the error (ERROR) output is in 3-State.

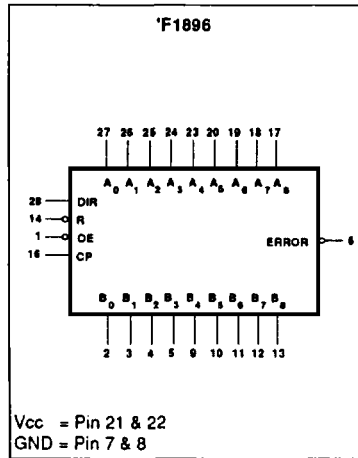
Transceiver with Parity Error

FAST 74F1894, F1895, F1896, F1897

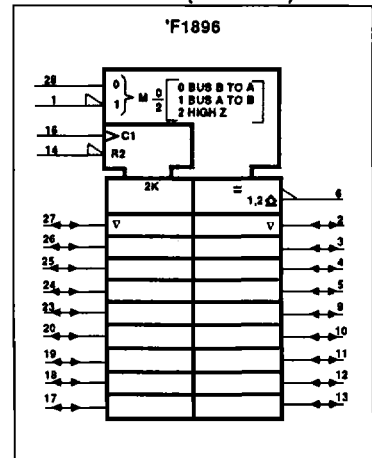
PIN CONFIGURATION



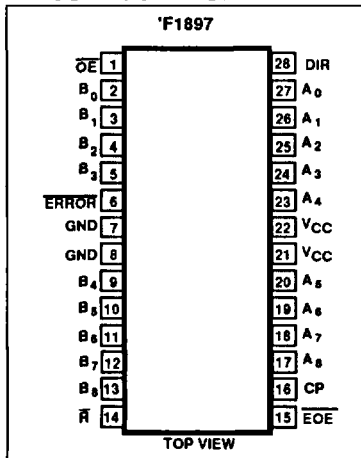
LOGIC SYMBOL



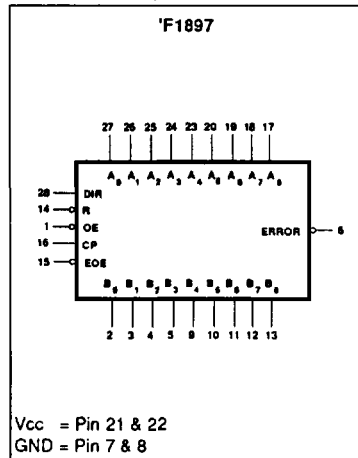
LOGIC SYMBOL (IEEE/IEC)



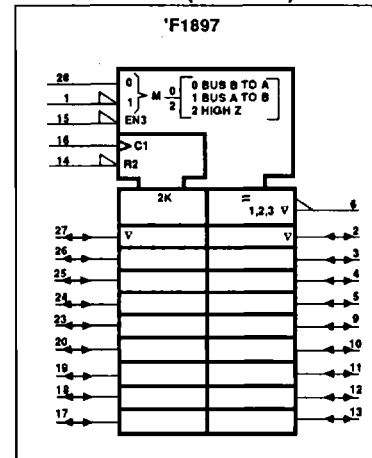
PIN CONFIGURATION



LOGIC SYMBOL



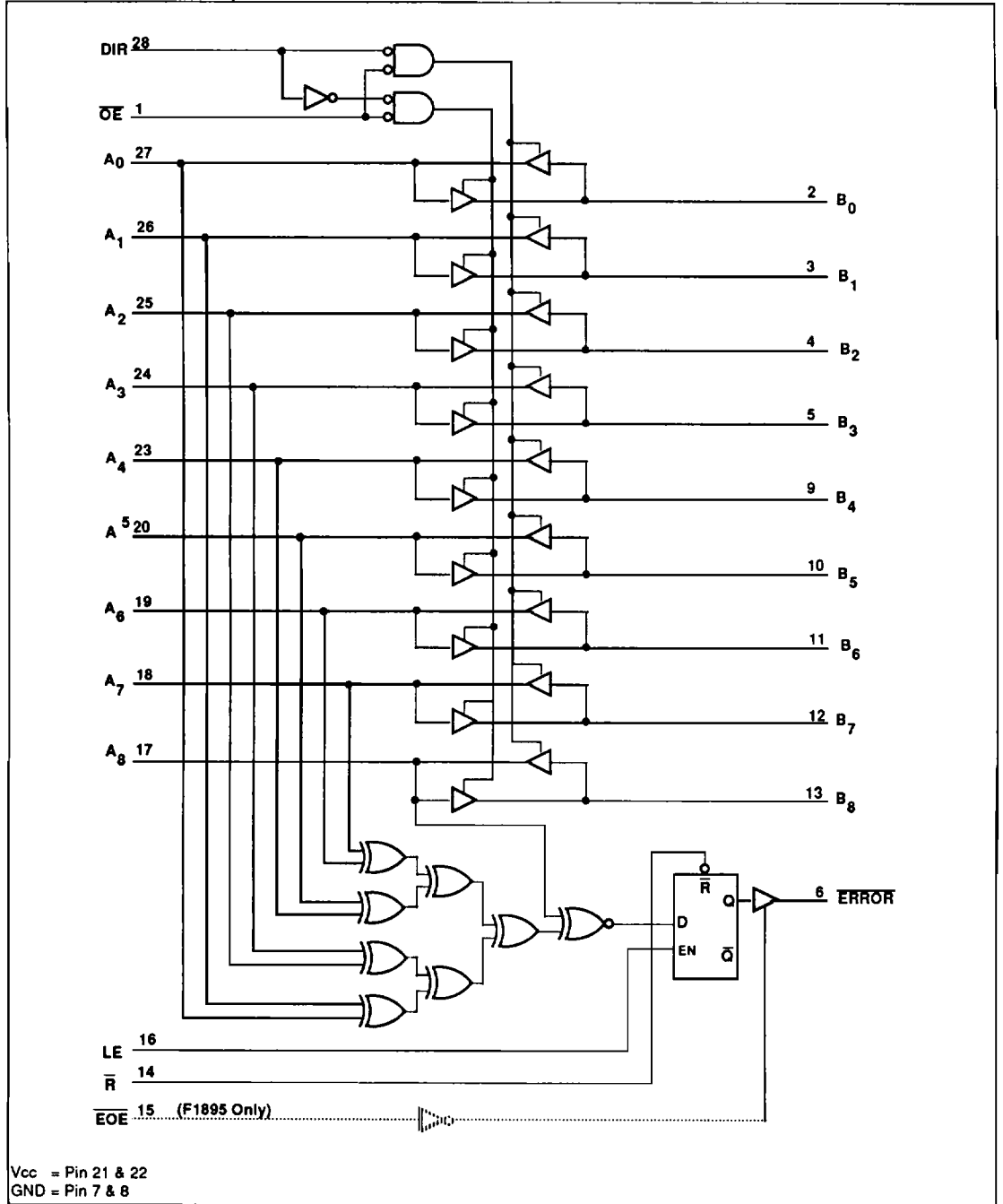
LOGIC SYMBOL (IEEE/IEC)



Transceiver with Parity Error

FAST 74F1894, F1895, F1896, F1897

LOGIC DIAGRAM FOR 'F1894, 'F1895

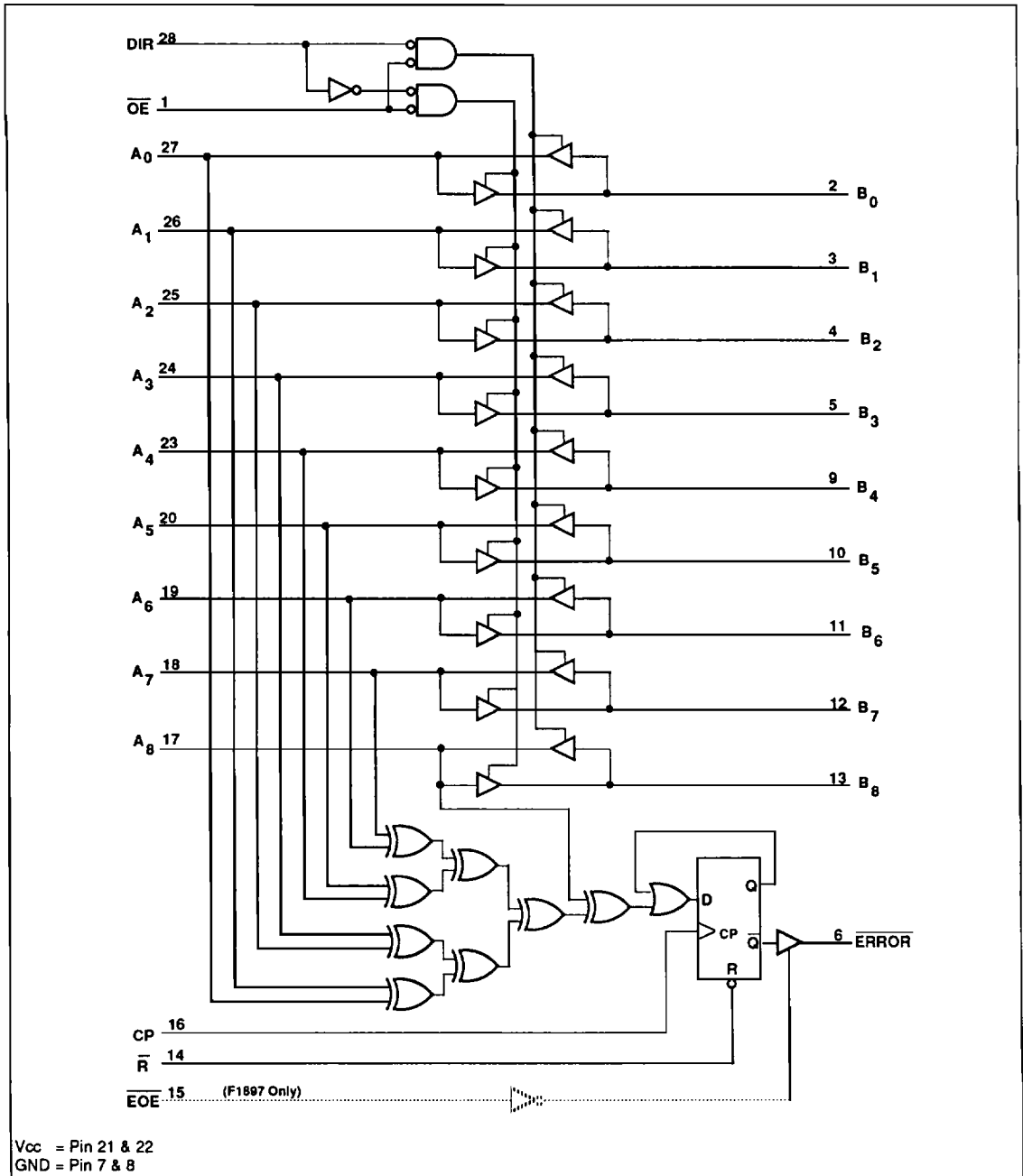


Vcc = Pin 21 & 22
 GND = Pin 7 & 8

Transceiver with Parity Error

FAST 74F1894, F1895, F1896, F1897

LOGIC DIAGRAM FOR 'F1896, 'F1897



Transceiver with Parity Error

FAST 74F1894, F1895, F1896, F1897

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT	
V_{CC}	Supply voltage	-0.5 to +7.0	V	
V_{IN}	Input voltage	-0.5 to +7.0	V	
I_{IN}	Input current	-30 to +5	mA	
V_{OUT}	Voltage applied to output in High output state	-0.5 to +5.5	V	
I_{OUT}	Current applied to output in Low output state	A_0-A_7	48	mA
		$B_0-B_7, \text{ ERROR}$	128	mA
T_A	Operating free-air temperature range	0 to +70	°C	
T_{STG}	Storage temperature	-65 to +150	°C	

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current	A_0-A_7		-3	mA
		$B_0-B_7, \text{ ERROR}$		-15	mA
I_{OL}	Low-level output current	A_0-A_7		24	mA
		$B_0-B_7, \text{ ERROR}$		64	mA
T_A	Operating free-air temperature	0		70	°C

Transceiver with Parity Error

FAST 74F1894, F1895, F1896, F1897

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS ¹			LIMITS			UNIT	
						Min	Typ ²	Max		
V _{OH}	High-level output voltage	A ₀ -A ₇	V _{CC} = MIN, V _{IL} = MAX, V _{IH} = MIN	I _{OH} = -3mA	±10%V _{CC}	2.4			V	
					±5%V _{CC}	2.7	3.4	V		
		B ₀ -B ₇ , ERROR			I _{OH} = -15mA	±10%V _{CC}	2.0			V
						±5%V _{CC}	2.0			V
V _{OL}	Low-level output voltage	A ₀ -A ₇	V _{CC} = MIN, V _{IL} = MAX, V _{IH} = MIN	I _{OL} = 24mA	±10%V _{CC}		0.35	0.50	V	
					±5%V _{CC}		0.35	0.50	V	
		B ₀ -B ₇ , ERROR			I _{OL} = 48mA	±10%V _{CC}		0.30	0.55	V
						±5%V _{CC}		0.42	0.55	V
V _{IK}	Input clamp voltage		V _{CC} = MIN, I _I = I _{IK}			-0.73	-1.2	V		
I _I	Input current at maximum input voltage	R, LE, CP, DIR, OE, EOE	V _{CC} = 0.0V, V _I = 7.0V				100	μA		
		A ₀ -A ₇	V _{CC} = MAX, V _I = 5.5V				2	mA		
		B ₀ -B ₇					1	mA		
I _{IH}	High-level input current	R, LE, CP, EOE	V _{CC} = MAX, V _I = 2.7V				20	μA		
		DIR, OE					40	μA		
I _{IL}	Low-level input current	R, LE, CP, EOE	V _{CC} = MAX, V _I = 0.5V				-20	μA		
		DIR, OE					-40	μA		
I _{OZH} + I _{IH}	Off-state output current, High-level voltage applied	A ₀ -A ₇ , B ₀ -B ₇	V _{CC} = MAX, V _O = 2.7V				70	μA		
I _{OZH} + I _{IL}	Off-state output current, Low-level voltage applied	ERROR(3S)	V _{CC} = MAX, V _O = 0.5V				-70	μA		
I _{OZH}	Off-state output current, High-level voltage applied	ERROR(OC)	V _{CC} = MAX, V _O = 2.7V				50	μA		
I _{OZL}	Off-state output current, Low-level voltage applied		V _{CC} = MAX, V _O = 2.7V				-50	μA		
I _{OS}	Short-circuit output current ³	A ₀ -A ₇	V _{CC} = MAX			-60		-150	mA	
		B ₀ -B ₇				-100		-225	mA	
I _{CC}	Supply current (total)	I _{CCH}	V _{CC} = MAX			90	125	mA		
		I _{CCL}				106	150	mA		
		I _{CCZ}				99	145	mA		

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Transceiver with Parity Error

FAST 74F1894, F1895, F1896, F1897

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			$T_A = +25^\circ\text{C}$ $V_{CC} = 5\text{V}$ $C_L = 50\text{pF}$ $R_L = 500\Omega$			$T_A = 0^\circ\text{C to } +70^\circ\text{C}$ $V_{CC} = 5\text{V} \pm 10\%$ $C_L = 50\text{pF}$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to B_n or B_n to A_n	Waveform 2	2.5 2.5	5.5 5.5	7.5 7.5	2.5 2.5	8.0 8.0	ns
t_{PLH} t_{PHL}	Propagation delay A_n to ERROR	Waveform 1, 2	7.0 7.0	10.0 10.0	14.0 14.0	7.0 7.0	16.0 16.0	ns
t_{PLH} t_{PHL}	Propagation delay R to ERROR	Waveform 1, 2	4.5 4.5	7.5 7.5	11.0 11.0	4.5 4.5	12.0 12.0	ns
t_{PLH} t_{PHL}	Propagation delay LE to ERROR (F1894,95 ONLY)	Waveform 1, 2	4.5 4.5	7.5 7.5	11.0 11.0	4.5 4.5	12.0 12.0	ns
t_{PLH} t_{PHL}	Propagation delay CP to ERROR (F1896,97 ONLY)	Waveform 1, 2	4.5 4.5	7.5 7.5	11.0 11.0	4.5 4.5	12.0 12.0	ns
t_{PZH} t_{PZL}	Output Enable time ¹ to High or Low level	Waveform 4 Waveform 5	3.0 4.0	5.5 7.0	8.0 9.5	3.0 4.0	9.0 11.0	ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low level	Waveform 4 Waveform 5	2.0 2.0	4.5 4.0	7.5 6.0	2.0 2.0	8.0 6.5	ns

NOTE:

1. These delay times reflect the 3-state recovery time only and not the signal through the buffers or the parity check circuitry. To assure VALID information at the ERROR pin, time must be allowed for the signal to propagate through the drivers (B to A), through the parity check circuitry to the ERROR output (same as A to ERROR) after the ERROR pin has been enabled (Output Enable time). VALID data at the ERROR pin is (B to A) + (A to ERROR) + (Output Enable time).

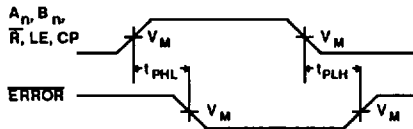
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			$T_A = +25^\circ\text{C}$ $V_{CC} = 5\text{V}$ $C_L = 50\text{pF}$ $R_L = 500\Omega$			$T_A = 0^\circ\text{C to } +70^\circ\text{C}$ $V_{CC} = 5\text{V} \pm 10\%$ $C_L = 50\text{pF}$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low A_n to CP	Waveform 3	7.0 7.0			14.0 14.0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low A_n to LE	Waveform 3	7.0 7.0			14.0 14.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low A_n to CP	Waveform 3	0.0 0.0			0.0 0.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low A_n to LE	Waveform 3	0.0 0.0			0.0 0.0		ns
$t_w(H)$ $t_w(L)$	Pulse width, High or Low CP	Waveform 3	7.0 7.0			8.0 8.0		ns
$t_w(H)$ $t_w(L)$	Pulse width, High or Low LE	Waveform 3	7.0 7.0			8.0 8.0		ns
$t_w(H)$ $t_w(L)$	Pulse width, High or Low R	Waveform 3	7.0 7.0			8.0 8.0		ns

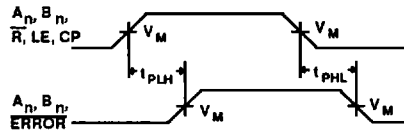
Transceiver with Parity Error

FAST 74F1894, F1895, F1896, F1897

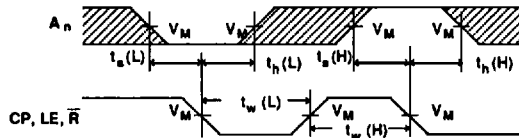
AC WAVEFORMS



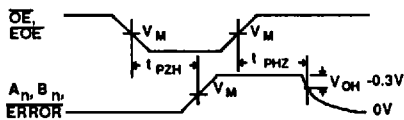
Waveform 1. Propagation Delay for Inverting Outputs



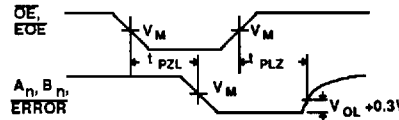
Waveform 2. Propagation Delay for Non-inverting Outputs



Waveform 3. Data Setup And Hold Times And CP, LE, and R-bar Pulse Widths



Waveform 4. 3-State Output Enable Time To High Level And Output Disable Time From High Level

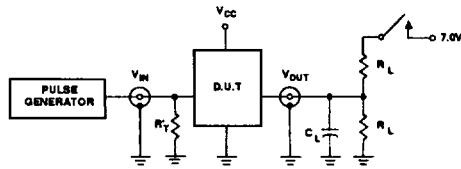


Waveform 5. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, $V_M = 1.5V$.

The shaded area indicate when the input is permitted to change for predictable output

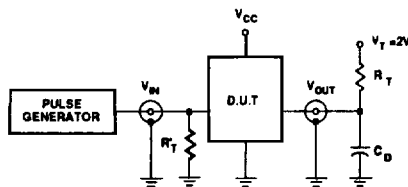
TEST CIRCUIT AND WAVEFORMS



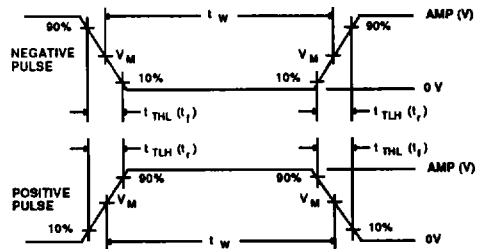
Test Circuit For 3-State Outputs

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZH}	closed
All other	open



Test Circuit For Open Collector Outputs



$V_M = 1.5V$

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

- R_L = Load resistor; see AC CHARACTERISTICS for value.
- C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
- R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

- C_D = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
- R_T = Termination resistor; see AC CHARACTERISTICS for value.