Chapter 1

Introduction

The TMS320 family of 16/32-bit single-chip digital signal processors combines the flexibility of a high-speed controller with the numerical capability of an array processor, offering an inexpensive alternative to custom VLSI and multichip bit-slice processors for signal processing.

The TMS32010, the first digital signal processor in the TMS320 family, was introduced in 1982. Since that time, the TMS320 family has established itself as the industry standard for digital signal processing. The powerful instruction set, inherent flexibility, high-speed number-crunching capabilities, and innovative architecture make these high-performance, cost-effective processors ideal for many telecommunications, computer, commercial, industrial, and military applications.

Note:

Throughout this document, TMS320C2x refers to the TMS320C25, TMS320C25-33, TMS320C25-50, TMS320E25, TMS320C26, and TMS320C28 unless stated otherwise. Where applicable, ROM includes the on-chip EPROM of the TMS320E25.

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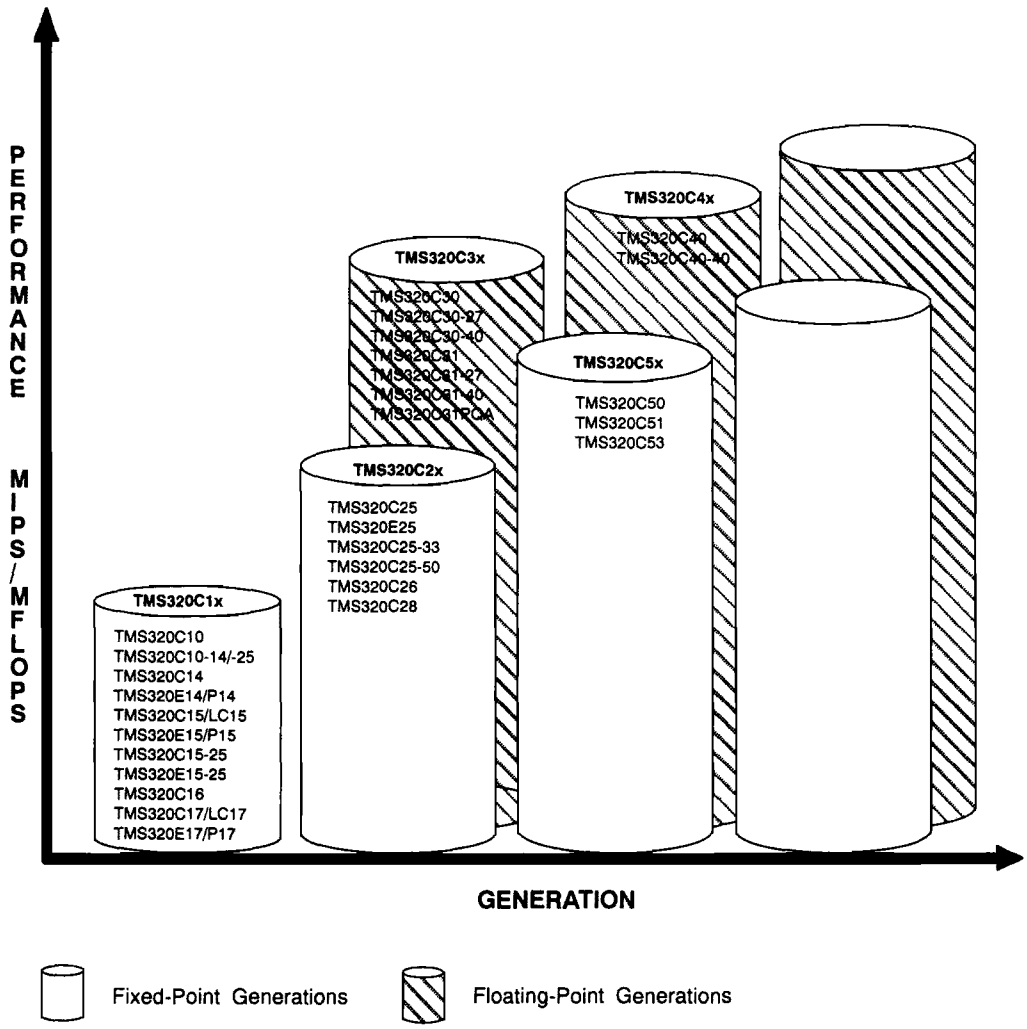
1.1 General Description

The TMS320 family currently consists of five generations: TMS320C1x, TMS320C2x, TMS320C3x, TMS320C4x, and TMS320C5x (see Figure 1–1). The family expansion includes enhancements of existing generations and more powerful new generations of digital signal processors. Many features are common among these generations. Some specific features are added in each processor to provide different cost/performance tradeoffs. Software compatibility is maintained throughout the family to protect the user's investment in architecture. Each processor has software and hardware tools to facilitate rapid design.

This document discusses the TMS320C2x devices:

- TMS320C25, a CMOS 40-MHz digital signal processor capable of twice the performance of the TMS320C1x devices
- TMS320C25-33 a CMOS 33-MHz version of the TMS32025
- TMS320C25-50, a CMOS enhanced-speed (50-MHz) version of the TMS320C25
- TMS320E25, a version of the TMS320C25 (40-MHz) with on-chip ROM replaced by secure, on-chip EPROM
- TMS320C26, a version of the TMS320C25 (40-MHz) with expanded configurable program/data RAM
- The TMS320C28, a version of the TMS320C25 (40-MHz) with expanded 8K-word on-chip ROM and an added power-down mode.

Figure 1–1. TMS320 Device Evolution



Plans for expansion of the TMS320 family include more spinoffs of the existing generations as well as more powerful future generations of digital signal processors.

The TMS320 family combines the high performance and specialized features necessary in digital signal processing (DSP) applications with an extensive program of development support, including hardware and software development tools, product documentation, textbooks, newsletters, DSP design workshops, and a variety of application reports. See Appendix K for a discussion of the wide range of development tools available.

The combination of the TMS320's Harvard-type architecture (separate program and data buses) and its special digital signal processing instruction set provide speed and flexibility to execute 12.8 MIPS (million instructions per second). The TMS320 family optimizes speed by implementing functions in hardware that other processors implement through software or microcode. This hardware-intensive approach provides the design engineer with power previously unavailable on a single chip.

The TMS320C2x generation includes six members: TMS320C25, TMS320C25-33, TMS320C25-50, TMS320E25, TMS320C26, and TMS320C28. Table 1–1 provides an overview of the TMS320C2x generation of processors with comparisons of memory, I/O, cycle timing, and package type.

Table 1–1. TMS320C2x Processors Overview

Device	On-chip RAM	Memory ROM/ EPROM	Off-chip Prog Data		I/O Ports †			Cycle Time (ns)	Package Type*			
					Ser	Par	DMA		PGA	PLCC	CER	QFP
TMS320C25‡	544	4K	64K	64K	Yes	16 × 16	Con	100	68	68	—	—
TMS320C25-33	544	4K	64K	64K	Yes	16 × 16	Con	120	—	68	—	—
TMS320C25-50§	544	4K	64K	64K	Yes	16 × 16	Con	80	—	68	—	—
TMS320E25§	544	4K	64K	64K	Yes	16 × 16	Con	100	—	—	68	80
TMS320C26	1568	256	64K	64K	Yes	16 × 16	Con	100	—	68	—	—
TMS320C28	544	8K	64K	64K	Yes	16 × 16	Con	100	—	68	—	80

†Ser = serial; Par = parallel; DMA = direct memory access; Con = concurrent DMA.
‡Military version available; contact nearest TI Field Sales Office for availability.
§Military version planned; contact nearest TI Field Sales Office for details.
*PGA = 68-pin grid array; PLCC = plastic-leaded chip carrier; CER = surface mount ceramic-leaded chip carrier (CER-QUAD); QFP = plastic quad flat package

The **TMS320C25**, like all members of the TMS320C2x generation, is processed in CMOS technology. The TMS320C25 is capable of executing 10 million instructions per second. Enhanced features such as 24 additional instructions (133 total), eight auxiliary registers, an eight-level hardware stack, 4K words of on-chip program ROM, a bit-reversed indexed addressing mode, and the low power dissipation inherent to the CMOS process contribute to the high performance.

The **TMS320C25-33** is a 33-MHz version of the TMS320C25. It is capable of an instruction cycle of 120 ns. It is architecturally identical to the 40-MHz version of the TMS320C25 and is pin-for-pin and object-code compatible with the TMS320C25.

The **TMS320C25-50** is a high-speed version of the TMS320C25. It is capable of an instruction cycle time of 80 ns. It is architecturally identical to the 40-MHz version of the TMS320C25 and is pin-for-pin and object-code compatible with the TMS320C25.

The **TMS320E25** is identical to the TMS320C25, except that the on-chip 4K-word program ROM is replaced with a 4K-word on-chip program EPROM. On-chip EPROM allows realtime code development and modification for immediate evaluation of system performance.

The **TMS320C26** is pin-for-pin and object-code compatible (except for RAM configuration instructions) with the TMS320C25. It is capable of an instruction cycle time of 100 ns. The enhancement over the TMS320C25 consists of a larger, configurable, on-chip RAM divided into 4 blocks, for a total 1568-word program/data space. The TMS320C26 is similar to the TMS320C25 except for its internal memory configuration. This is discussed in Section NO TAG and in Appendix NO TAG.

The **TMS320C28** is object code-compatible with the TMS320C25. It is capable of an instruction cycle time of 100 ns. The TMS320C28 contains an expanded 8K words of on-chip program ROM and an added power-down mode, which conserves power while saving the contents of on-chip SRAM (B0, B1, and B2).

1.2 Key Features

Key features of the TMS320C2x devices are listed below. Those that pertain to a particular device are followed by the device name within parentheses.

- ❑ Instruction cycle timing:

  80-ns (TMS320C25-50)
  100-ns (TMS320C25, TMS320E25, TMS320C26, and TMS320C28)
  120-ns (TMS320C25-33)

- ❑ 544-word programmable on-chip data RAM
- ❑ 1568-word configurable program/data RAM (TMS320C26 only)
- ❑ 4K-word on-chip program ROM (TMS320C25, TMS302C25-33, and TMS320C25-50)
- ❑ 8K-word on-chip program ROM (TMS320C28 only)
- ❑ Secure 4K-word on-chip program EPROM (TMS320E25)
- ❑ 128K-word total data/program memory space
- ❑ 32-bit ALU/accumulator
- ❑ 16- ×16-bit parallel multiplier with a 32-bit product
- ❑ Single-cycle multiply/accumulate instructions
- ❑ Repeat instructions for efficient use of program space and enhanced execution
- ❑ Block moves for data/program management
- ❑ On-chip timer for control operations
- ❑ Up to eight auxiliary registers with dedicated arithmetic unit
- ❑ Up to eight-level hardware stack
- ❑ Sixteen input and sixteen output channels
- ❑ 16-bit parallel shifter
- ❑ Wait states for communication to slower off-chip memories/peripherals
- ❑ Serial port for direct codec interface
- ❑ Synchronization input for synchronous multiprocessor configurations

- ❑ Global data memory interface
- ❑ TMS320C1x source-code upward compatibility
- ❑ Concurrent DMA using an extended hold operation
- ❑ Instructions for adaptive filtering, FFT, and extended-precision arithmetic
- ❑ Bit-reversed indexed-addressing mode for radix-2 FFT
- ❑ On-chip clock generator
- ❑ Single 5-V supply
- ❑ Power-down mode (TMS320C28 only)
- ❑ Device packaging:

  68-pin PGA (TMS320C25)
  68-lead PLCC (TMS320C25, TMS320C26, and TMS320C28)
  68-lead CER-QUAD (TMS320E25)
  80-pin QFP (TMS320C28)

- ❑ Commercial and military versions available

1.3 Typical Applications

The TMS320 family's unique versatility and realtime performance offer flexible design approaches in a variety of applications. In addition, TMS320 devices can simultaneously provide the multiple functions often required in those complex applications. Table 1–2 lists typical TMS320 family applications.

Table 1–2. Typical Applications of the TMS320 Family

General-Purpose DSP	Graphics/Imaging	Instrumentation
Digital Filtering Convolution Correlation Hilbert Transforms Fast Fourier Transforms Adaptive Filtering Windowing Waveform Generation	3-D Rotation Robot Vision Image Transmission/ Compression Pattern Recognition Image Enhancement Homomorphic Processing Workstations Animation/Digital Map	Spectrum Analysis Function Generation Pattern Matching Seismic Processing Transient Analysis Digital Filtering Phase-Locked Loops
Voice/Speech	**Control**	**Military**
Voice Mail Speech Vocoding Speech Recognition Speaker Verification Speech Enhancement Speech Synthesis Text-to-Speech	Disk Control Servo Control Robot Control Laser Printer Control Engine Control Motor Control	Secure Communications Radar Processing Sonar Processing Image Processing Navigation Missile Guidance Radio Frequency Modems
Telecommunications		**Automotive**
Echo Cancellation ADPCM Transcoders Digital PBXs Line Repeaters Channel Multiplexing 1200 to 19200-bps Modems Adaptive Equalizers DTMF Encoding/Decoding Data Encryption	FAX Cellular Telephones Speaker Phones Digital Speech Interpolation (DSI) X.25 Packet Switching Video Conferencing Spread Spectrum Communications	Engine Control Vibration Analysis Antiskid Brakes Adaptive Ride Control Global Positioning Navigation Voice Commands Digital Radio Cellular Telephones
Consumer	**Industrial**	**Medical**
Radar Detectors Power Tools Digital Audio/TV Music Synthesizer Toys and Games Solid-State Answering Machines	Robotics Numeric Control Security Access Power Line Monitors	Hearing Aids Patient Monitoring Ultrasound Equipment Diagnostic Tools Prosthetics Fetal Monitors

Many of the TMS320C2x features, such as single-cycle multiply/accumulate instructions, 32-bit arithmetic unit, large auxiliary register file with a separate arithmetic unit, and large on-chip RAM and ROM make the device particularly applicable in digital signal processing systems. At the same time, general-purpose applications are greatly enhanced by the large address spaces, on-chip timer, serial port, multiple interrupt structure, provision for external wait states, and capability for multiprocessor interface and direct memory access.

The TMS320C2x has the flexibility to be configured to satisfy a wide range of system requirements. This allows the device to be applied in systems currently using costly bit-slice processors or custom ICs. These are examples of such system configurations:

- A standalone system using on-chip memory,
- Parallel multiprocessing systems with shared global data memory, or
- Host/peripheral coprocessing using interface control signals.