TC8600F

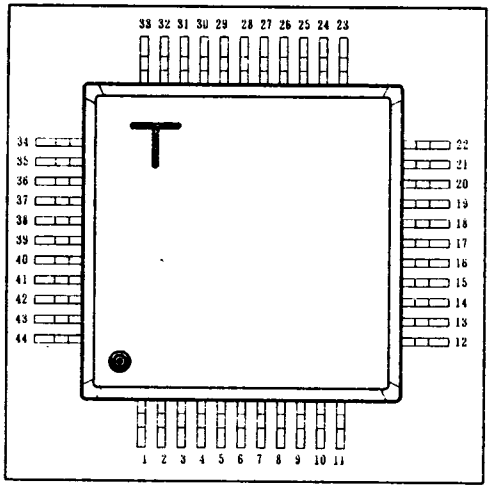
(Floppy Disk Mechanism Controller)

INTRODUCTION

The FDMC-II TC8600F is a one chip C-MOS LSI in which the control logic of FLOPPY DISK DRIVE (FDD), together with the 4-bit CPU and required random logic.

This LSI has the direct input terminal that receive the system interface input terminal of FDD and output terminal of the stepping motor, read/write circuit, etc, in the drive.

This LSI can be replaced by the digital control board. In the TC8600F, the firmware is builtin ROM of CPU, so it can use for 5.25 inch floppy disk drive immediately.



No.	I/O	Pin name	No.	I/O	Pin name
1	I	HDMODE	23	I	LPTYPE
2	I	-MOTRON	24	I	+AUTORZ
3	I	-HLOAD	25	O	+RWPWR
4	I	+TEST	26	O	+SMPS
5	I	XIN	27	O	+MOTREN
6	O	XOUT	28	O	+SWFLTR
7	I	-CLR	29	O	PHASE1
8	I	-HOLD	30	O	PHASE2
9	O	+DSOUT	31	O	+PWRON
10	O	+HD0	32	O	+LEDSCN
11	O	+ERA	33	O	+DSKCHG
12	O	+WE	34	O	+WP
13	I	-EXT0	35	O	+INDEX
14	I	-EXT1	36	O	+TRK00
15	I	-WG	37	O	+READY
16	I	-DKCHRS	38	G	(GND)
17	V	(VDD)	39	V	(VDD)
18	I	-SISEL	40	I	+WPSNS
19	I	-DS	41	I	-TZSNS
20	I	-DIR	42	I	-DISNS
21	I	STEP	43	I	+IXSNS
22	I	-SGND	44	I	-TWSTEP

FEATURES

- o Low power consumption by Si-Gate C-MOS technology.
- o TLCS-47 CPU full-compatible
- o Direct input terminal of system interface
  (TTL compatible)
- o Enable to various variation method in 5.25 inch FDD
- o Built in sensor (Photo-Diode) input circuit
- o 44 PIN mini FP

1. GENERAL DESCRIPTION

The TC8600F is a floppy disk mechanism controller (=FDMC) having various option selecting capability for composing a 5.25 inch floppy disk drive described as follows.

Disk Type Select

500KB / 1.0MB compatible drive

This mode is for producing two drive models using same mechanism which transfer head carriage with 96TPI at a phase shift of stepping motor. LSI has a programmability to select 1 or 2 phase shift on the each step pulse from the system interface. the "2STEP" mode correspond to 48TPI model.

1.0MB / 1.6MB Compatible Drive Model

This mode is for producing an user programable drive model that has a capability to changing spindle motor rotating speed. 300rpm and 360rpm are assumed as preprogramed rotation.

1.0M byte mode :	Media rotation	300 rpm
	Data transfer rate	250K bps
1.6M byte mode :	Media rotation	360 rpm
	Data transfer rate	500K bps

2.0MB Unformatted Capacity FDD Mode

This mode is for producing a high capacity disk drive. 2MB drive is accomplished by using 300 rpm media rotation and 500K bps data transfer rate. This FDD has the largest capacity in the 5.25 inch disk drive currently. In this type, the erase timing is programmed correspond to read/write erase gap of 400 to 550 um.

Option Select

Radial Mode Select

This mode supports the radial connection about the INDEX and READY signals that wire from all drives to each host controller. In this mode, [READY] and [INDEX] are always logic outputting independently of Drive Select [-DS] in the system interface.

Motor Off Delay Select

In the rotation control of spindle motor, it is possible to select the 2.5 sec off delay function.(a part of model)

Automatic Chucking Function

It is possible to select the function that makes spindle motor rotating momentary for sure chucking of the disk media inserted. The spindle motor rotates when the Disk-In is detected, and keeps rotating until internal ready is detected.(for all FDD)

2. DESCRIPTION OF PINS

[1] -HD/HM (Head Load DS/Head Load Motor on) Input
This pin defines the head load condition by selecting the active condition of [+HDEN] terminal. When this terminal is a "High level", [+HDEN] is controlled by [+MTRON] condition. Drive model is able to change by using jumper option on the FDD board.

[2]-MTRON(Motor on) Input
This pin is for the control the spindle motor. It is "Low active" signal and connects with the system interface terminal.

[3] -HLOAD (Head Load) Input
This pin is for the control the Head Load. It is "Low active" signal and connects with system interface terminal.

[4]+TEST(LSI Test) Input
This pin is a test pin for the LSI and usually in "Low level".

[5]XIN(X'tal Input) Input
This pin is connect with ceramic resonator for clock generator.

[6]XOUT(X'tal Output) Input
This pin is connect with ceramic resonator for clock generator.

[7]-RESET (Reset) Input
This pin is for system reset of the LSI. Input the "Low level" signal for initializing the LSI when the power is on.

[8] -HOLD (Hold) Input
This pin is for HOLD request of internal CPU. It is not used in TC8600F and usually set in a "High level".

[9] +DSOUT (Drive Select out) Output
This pin outputs "High active" logic of [-DS] in the system interface terminal. This pin is activated to "High level" when [-RESET] is a "High level" and [-DS] is a "Low level".

[10]+HEAD0 (Head 0 Select) Output
This pin is for the control of the read/write head drive circuit. Head 0 Select signal

[11]+ERASE (Erase Gate Output) Output
This pin is for the control of the erase head. This terminal provide the delayed erase signal for the Tunnel erase head with the positive logic.

[12]+WRITE (Write Gate) Output
This pin is for control of the read/write head. This terminal provide the write enable signal for the head for the positive logic.

[13]FWSEL-2 (Firm Ware Select-2) Input
This pin is a programming pin for the function selection.

[14] FWSEL-3 (Firmware Select-3) Input
This pin is a programming pin for the function selection.

[15]-WGATE (Write Gate) Input
This pin is connect to the WRITE GATE terminal of system interface

[16]-DKCHR (Disk Change Reset) Input
This pin is connect to the DISK CHANGE RESET terminal of the system interface.

[17] VDD (Power Supply) Input
Power source terminal for LSI. +5 V DC power will spilled.

[18]-SISEL(Side Select) Input
This pin is connect to the SIDE SELECT terminal of the system interface.

[19] -DS (Drive Select) Input
This pin is connect to the DRIVE SELECT n terminal of the system interface.

[20] -DIR (Direction) Input
This pin is connect to the DIRECTION of the system interface.

[21]-STEP (Step) Input
This pin is connect to the STEP terminal of the system interface.

[22] -INUSE (Inuse) Input
This pin is connect to the INUSE terminal of the system interface.

[23]FWSEL-0(Firmware Selection-0) Input
This pin is a programming pin for the function selection.

[24]FWSEL-1 (Firmware Selection-1) Input
This pin is a programming pin for the function selection.

[25]+HDEN (Head Load Enable) Output
This pin is activated to "High level" when the system needs currents flowing to the solenoid.

[26] +SMPS (Step Motor Power Supply) Output
This pin is activated to "High level" when the system needs cutting off the +12 V power supply for stepping motor.

[27] +MTREN (Motor Enable) Output
This pin is activated to "High level" when the system needs spindle motor rotating. The spindle motor will be controlled not only by the [MTRON] input but also by diskette chucking instantaneous operation.

[28] +LINUSE (Lamp Inuse) Output
This pin is an output signal of the inuse lamp control. It is possible to choose being controlled directly by the [-INUSE] or the signal latched by the [-DS]. This mode is called as latched inuse.

[29] +PHASE-1 (Phase-1) Output
This pin is a control output of the step motor phase. The first phase is outputted.

[30] +PHASE-2 (Phase-2) Output
This pin is a control output of the step motor phase. The second phase is outputted.

[31] +HLPS (Head Load Power Save) Output
This pin is an output terminal of the head load solenoid power control. This pin is activated to a "High level" when the system needs to keep low voltage applied to the head load solenoid.

[32] +SWFIL (Switch Filter) Output
This pin is an output terminal to control the compensation of the characteristics of the read/write circuit relation to the track position. If the track number is over 44, this pin is a "High level".

[33] +DS/RDY (Drive Select/Ready) Output
This pin is a supplementary output terminal for the circumstance circuit control. The function of this pin varies with three way. selection. At first, the positive logic [-DS] of the system interface, and second, logical AND signal of the [-DS] and [READY], and third [DISK CHANGED] output signal . In the last selection, this pin connects to the [DISK CHANGED] pin of the system interface via open collector buffer.

[34] +WP (Write Protect) Output
This pin is for the system interface output. This pin connects to the [-WRITE PROTECT] of the system interface via the open collector buffer

[35] +INDEX (Index) Output
This pin is for the system interface output. This pin connects to the [-INDEX] of the system interface via the open collector buffer.

[36] +TRACK0 (Track Zero) Output
This pin is for the system interface output. This pin connects to the [-Track 0] of the system interface via the open collector buffer.

[37] +READY (Ready) Output
This pin is for the system interface output. This pin connects to the [-READY] of the system interface via the open collector buffer.

[38] [VSS] (GND) Input
The LSI system ground terminal.

[39] [VDD] (Power Supply) Input
The power source terminal for LSI. +5 V DC power will applied.

[40] -WPSNS (Write Protect Sensor) Input
This pin is a photo sensor input. To apply a "High level" signal when the diskette is write protected.

[41] -TZSNS (Track Zero Sensor) Input
This pin is a photo sensor input. To apply a "Low level" signal when the head carriage is on the track 0 area.

[42] -DISNS (Disk In Sensor) Input
This pin is a photo sensor input. To apply a "Low level" signal when a diskette is inserted in the drive.

[43] +IXSNS (Index Sensor) Input
This pin is a photo sensor input. To apply a positive pulse signal derived from diskette index hole.

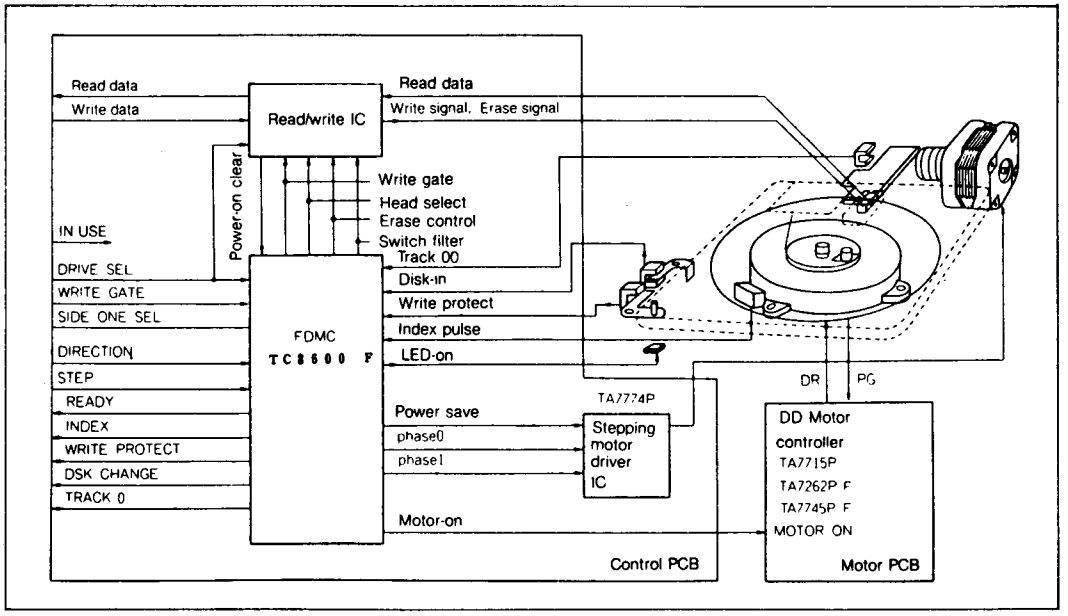
[44] -2STP/+ARTZ (2-Step/Automatic Return to Zero) Input
This pin is for a supplementary function selection. Beside with the function selection by the FWSEL 0 to 3, this terminal select the 2step seek mode or automatic return to zero function.

3. FLOPPY DISK SYSTEM

3.1 System Configuration

Fig 3.1 shows the situation of the FDMC in a FDD. TC8600F receives the control signals from the host system, and executes the digital control of the FDD.

Although read/write analogue signals are processed by R/W IC, the write enable and the erase enable are controlled suitably by TC8600F. The FDD has many mechanical parts, that is, step motor for positioning the head carriage, spindle motor for rotating disk media, solenoid for head loading, etc. The TC8600F puts out the control signals for these parts.



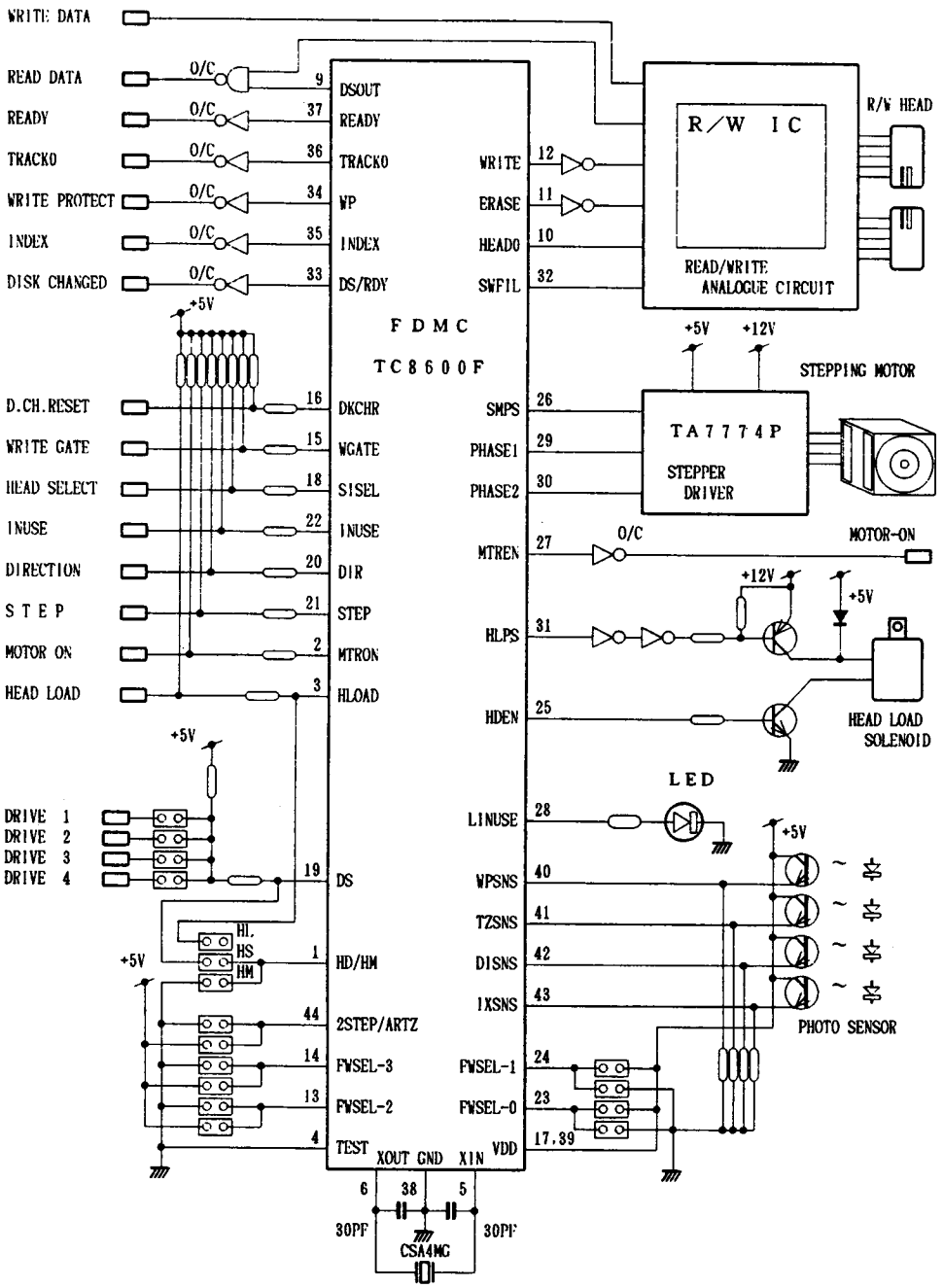
3.2 Operation Summary

There are two type of operation in a FDD which is controlled by TC8600F. These are initialization and normal operation. The initialization process consists of electrical setup and mechanical setup. In the electrical setup, TC8600F reads program input and sets operation mode required. In the mechanical setup, TC8600F moves head toward track 0 (outer) evaluating the track 0 sensor input so as to make match the counter in

the LSI with the physical position. (this operation is called recalibrate operation.)
In the normal operation, the following operation is proceeded.

- o Phase shift operation of the step motor according with the step pulse.
- o Generate the ready status by evaluating the INDEX PULSE.
- o Proceed auto chucking operation by disk in trigger.
- o Off delay control of head load signal.
- o Management the write enable(WE) and erase gate(ERA) signals correspond to the write gate from the system interface.

3.3 Example FDD System



4 FUNCTIONAL DESCRIPTION

4.1 Function Selection

The TC8600F has five pins for function selection (such as [FWSEL-3], [FWSEL-2], [FWSEL-1], [FWSEL-0], [+2STEP/+ARTZ]). Three pins ([FWSEL-3], [FWSEL-2] and [+2STEP/+ARTZ]) are evaluated only once after the LSI power is on. other two pins are repeatedly evaluated during normal operation. The function is selected one of the sixteen combined with 4-pins i.e.FWSEL-0 to -3.

According to this selection, the function of [+2STEP/-ARTZ] varies. In some mode, this pin selects 2step shift or not, and in another mode, this pin selects auto matic return to zero function is ON or not, as an option. These functions are shown in table 4.1a,4.1b,4.1c .

Table 4.1a Function Selection Map (a)

FWSEL 3210	DRIVE TYPES
11XX	1Mbyte, 1.6Mbyte, 500Kbyte each model
10XX	2Mbyte model, media rotation 300rpm, data transfer rate 500kbps R/W-E gap-length in this model correspond to 400, 450, 500, 560um
01XX	1Mbyte/1.6Mbyte Interface is daisy connective type (INDEX and READY)
00XX	1Mbyte/1.6Mbyte Interface is radial connective type (INDEX and READY)

Table 4.1b Function Selection Map (b)

FWSEL 3210	TYPE NO.	Index Ready Time (ms)	Spindle Rotation	Erase Delay (us) On Delay	Erase Delay (us) Off Delay	Options 2STEP	Options ARTZ	Power ON Step IN
1111	15	126 to 238	300/360	194±14	546±14	NA	SEL	EXECUTE
1110	14	158 to 238	300	314±14	934±14	SEL	NA	NO
1101	13	126 to 238	300/360	194±14	546±14	NA	SEL	EXECUTE
1100	12	158 to 238	300	314±14	934±14	SEL	NA	NO
1011	11	126 to 238	300/360	262±14	598±14	NA	SEL	EXECUTE
1010	10	126 to 238	300/360	202±14	542±14	NA	SEL	EXECUTE
1001	9	126 to 238	300/360	162±14	502±14	NA	SEL	EXECUTE
1000	8	126 to 238	300/360	122±14	462±14	NA	SEL	EXECUTE
0111	7	126 to 238	300/360	162±14	494±14	NA	SEL	EXECUTE
0110	6	126 to 238	300/360	114±14	514±14	NA	SEL	EXECUTE
0101	5	126 to 238	300/360	114±14	602±14	NA	SEL	EXECUTE
0100	4	126 to 238	300/360	162±14	494±14	NA	SEL	EXECUTE
0011	3	126 to 238	300/360	162±14	494±14	NA	SEL	EXECUTE
0010	2	126 to 238	300/360	114±14	514±14	NA	SEL	EXECUTE
0001	1	126 to 238	300/360	114±14	602±14	NA	SEL	EXECUTE
0000	0	126 to 238	300/360	162±14	494±14	NA	SEL	EXECUTE

Note NA : Not Available
SEL : Select a function if the [+2step/+ARTZ] pin is a "High level".

Function Selection by [+2STEP/+ARTZ]

At the function type No14 and No12 in the table 4.1, the [+2STEP/+ARTZ] pin decides whether the "2STEP" operation is selected or not. This function performs that both 96TPI and 48TPI FDD are able to produce with using the common mechanical parts except the magnetic head. If the "2STEP" operation is selected, TC8600F will generate double phase shift on each step pulse received. Additionally, the [SWFIL] output pin, that is for compensating read/write amplifier characteristic, is controlled at same position independently of this selection.

At the other function type mentioned-above, this pin decides whether the automatic return to zero function is selected or not. If this function is selected, the seek range limitation is done. The seek range limitation is a function that the LSI ignores the step pulse when the head carriage attempt to move outside the range defined.
The range is from 0-track to 83-track. The position of the 0-track is recalibrated by track zero sensor.

Automatic Return to Zero Function

This function works when LSI power is on ([-CLR] terminal of TC8600F is released). This automatic return to zero function has two parts. That is, the power on step in and the return to zero operation. The power on step in operation always executes even if the automatic return to zero function is not selected.

Power on Step in Operation

This operation is done as follows. At first, the track 0 sensor status is evaluated. If the status is active (active means the head is on the track 0 region.), the FDMC moves the head carriage to the inner direction at one track, and waiting phase shift time. this operation repeats by each tracks until the track 0 sensor is inactive. This sequence repeats 15 times at a maximum and the waiting time is 3 mS.

After repeating 15 times without track 0 detection, the FDMC goes to the next state, return to zero operation after waiting 15 mS settling time.

Return to Zero Operation

In this operation, FDMC executes outer seek operation until the TRACK-0 status will be active. This stepping operation will be done 200 phase shift at a maximum. After 200 phase shift is done without TRACK-0 detection, FDMC goes to next procedure.
The power on step in sequence is for the safe operation in such a drive that has elastic carriage stopper at the track zero position, so as to keep precisioness avoiding mechanical collision. But using such mechanism causes wrong track recalibrating, in case that head is located outer track 0(-1 or -2 track) position. In that drives, actual track 0 position is defined as a track which is the first zero track found scanning from inner direction. With this manner, FDMC never misplace track 0, even if start at negative track position by the residue of former status of disk drive.

Table 4.1c Function Selection Map (c)

FWSEL 3210	TYPE NO.	Motor off Delay (s)	28Pin Out (LINUSE)	33Pin Out (+DS/RDY)	Daisy/Radial Index,Ready	FDD Type Capa. Unformat R/Egap
1111	15	None	Lat.Inuse	DS&Ready	Daisy	1.0Mbyte
1110	14	None	In Use	DS	Daisy	1.0/0.5M
1101	13	2.5	Lat.Inuse	DS&Ready	Daisy	1.0Mbyte
1100	12	None	In Use	DS	Radial	1.0/0.5M
1011	11	None	In Use	Disk Changed	Radial	2 Mbyte 560um
1010	10	None	In Use	Disk Changed	Radial	2 Mbyte 500um
1001	9	None	In Use	Disk Changed	Radial	2 Mbyte 450um
1000	8	None	In Use	Disk Changed	Radial	2 Mbyte 400um
0111	7	None	In Use	Disk Changed	Daisy	1.6Mbyte
0110	6	None	In Use	Disk Changed	Daisy	1.0Mbyte
0101	5	None	In Use	Disk Changed	Daisy	1.0Mbyte
0100	4	2.5	In Use	Disk Changed	Daisy	1.0Mbyte
0011	3	None	In Use	Disk Changed	Radial	1.6Mbyte
0010	2	None	In Use	Disk Changed	Radial	1.0Mbyte
0001	1	None	In Use	Disk Changed	Radial	1.0Mbyte
0000	0	2.5	In Use	Disk Changed	Radial	1.0Mbyte

Motor Off Delay Control (TYPE 13,4,0)

Although the [+MTREN] terminal is controlled by the system interface [+MTRON], this function adds extra on signal at each time that the motor off. The off delay time is 2.5sec. This function make better the noise and response time when the motor turn to ON and OFF repeatedly in a short time.

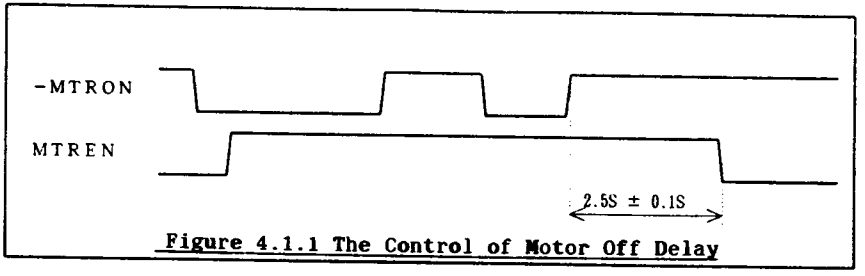


Figure 4.1.1 The Control of Motor Off Delay

Linuse Output

This 28th pin [LINUSE] may be selected the signal whether positive logic output of 22th pin [-INUSE] or latched [-INUSE] signal by [-DS] signal.

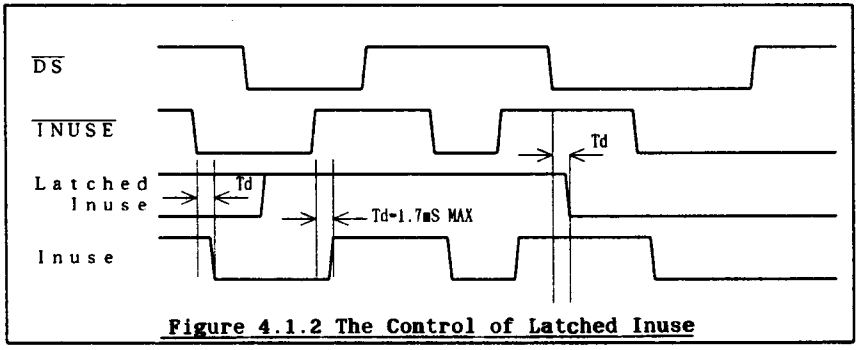


Figure 4.1.2 The Control of Latched Inuse

+DS/RDY Terminal Selection

The 33th [+DS/RDY] has the three function selecting pattern.

DS&Ready (TYPE 15,13)

The logical and signal of external [-DS] and internal Drive Ready. In this case, it is the same signal as 37th pin [+READY].

DS (TYPE 14,12)

This signal is a positive logic of [-DS] external. In this case, it is the same signal as the 9th pin [+DSOUT].

Disk Changed (TYPE 0 to 11)

The logical and signal of external [-DS] and an output of the internal flipflop disk changed which monitors changing of disk media.

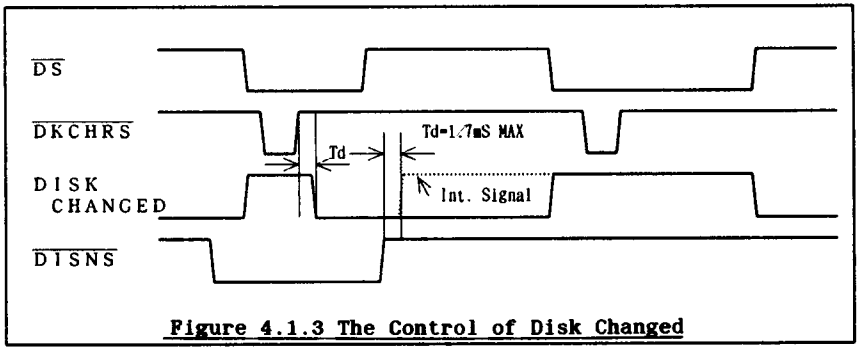


Figure 4.1.3 The Control of Disk Changed

DAISY/RADIAL Selection

In the daisy mode, the system interface output is available when [-DS] terminal is active. In the radial mode, [INDEX] signal and [READY] signal have no relation to [-DS], and they are always valid. In this case, the system interface output ([INDEX] signal and [READY] signal) is wired to the host controller directory. (radial connection).

4.2 Specification

4.2.1 Stepping Motor Control

FDMC controls stepping motor as a two-phase exciting type. The phase control signals are output to [PHASE1] and [PHASE2] in a positive logic. Actual stepping motor will be drived by a current drive IC.
The rising edge of the step pulse signal [-STEP] from the system interface is sampled together with the direction signal [-DIR]. The builtin CPU receives it as an interrupt request and updates motor phase output required.

The stepping motor power save output [SMPS] controls the motor drive IC to decrease the idling current of the stepping motor in a quiescent stage. A "High level" on this terminal means decrease the current.
The motor drive IC has an input to exchange driving voltage source. Usually, +12 V DC is for active driving and +5 V DC is for quiescent stage.

FDMC activates the [SMPS] terminal to a "High level" when the stepping operation is over and certain times elapsed (settling time).

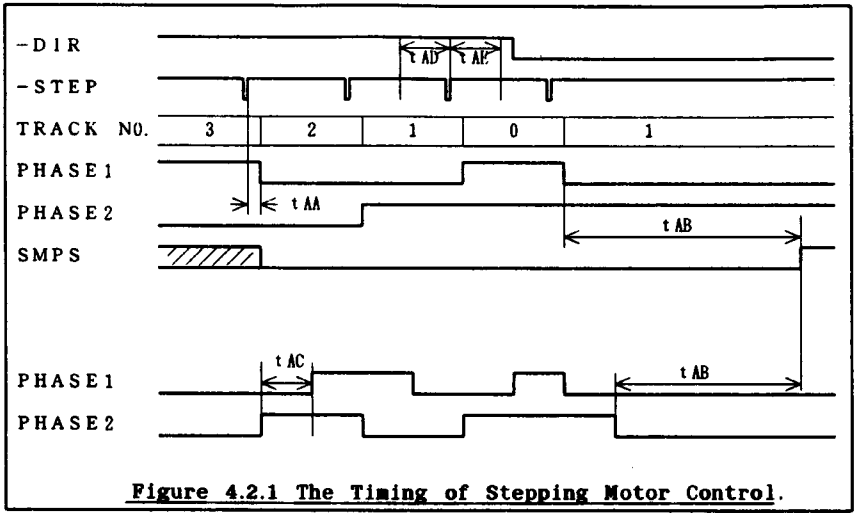


Figure 4.2.1 The Timing of Stepping Motor Control.

Table 4.2.1 Stepping Motor Driving Timing.

NAME	PARAMETERS	MIN	TYP	MAX	UNIT	REF.
tAA	Step to Phase Shift Time		150	270	us	
tAB	S.M.Motor Power Save Time	56	60	62	mS	
tAC	Second Phase Starting Delay	2.5	2.8	3.0	mS	
tAD	Set Up Time for direction	200			ns	
tAE	Hold Time for direction	200			ns	

4.2.2 Ready Timing Control

This operation generate the Ready signal by evolution pulse input from the [+IXSNS] pin.

o Ready on condition
Disk-In, Motor on and INDEX pulse comes continuously two cycles within the valid interval.

o Ready off condition
1. Disk is out or motor is off.
2. The pulse does not come within the valid interval.
3. The index pulse comes continuously five times off the interval.

Internal Ready status output to [+READY] terminal, but output condition is changed whether the FDMC mode is radial mode or the daisy mode.

o DAISY MODE

[+READY]=([-DS]="Low") and (internal ready="True")

o RADIAL MODE
[+READY]=(internal ready="True")

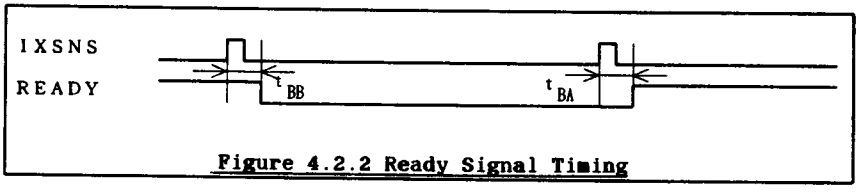


Figure 4.2.2 Ready Signal Timing

Table 4.2.2 Ready Signal Timing

NAME	PARAMETERS	MIN	TYP	MAX	UNIT	REF.
tBA	INDEX Sensor to READY	0.3	0.8	1.7	mS	
tBB	INDEX Sensor to NOT READY	0.3	0.8	1.7	mS	

4.2.3 Track Zero Output Control

The status of Track-0 is a condition that the sensor interface input terminal [-TZSNS] is a "Low level" and the stepping motor phase output is "00" ("00" means both PHASE1 and PHASE2 are "High level"). In this condition, track 0 output [+TRACK0] will be activated when the [-DS] is a "Low level"

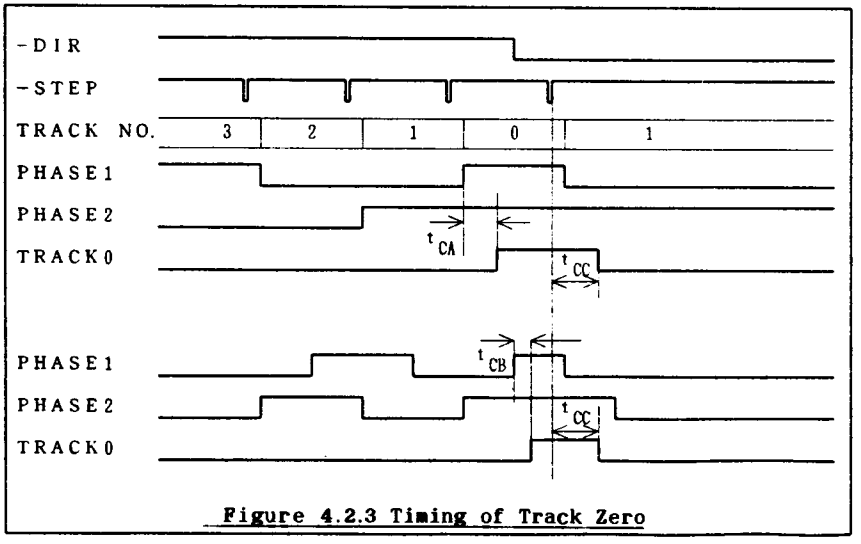


Figure 4.2.3 Timing of Track Zero

Table 4.2.3 Timing of Track Zero

NAME	PARAMETERS	MIN	TYP	MAX	UNIT	REF.
tCA	1'st Phase to Track 00			200	uS	
tCB	2'nd Phase to Track 00			200	mS	
tCC	Step to Not Track 00		150	500	uS	
tCD	Track0 sensor to Track00		0.7	1.7	mS	
tCE	Track0 sensor to Not Track00		0.7	1.7	mS	

4.2.4 Erase Timing Control

The erase delay timing is programed for a TUNNEL erase type of read/write head. Several parameters are prepared for the various kind of disk format. This parameter should be decided with consideration of the data transfer rate and disk rotation and the length of between R/W and ERASE. Table 4.1a shows the values on each function selected.

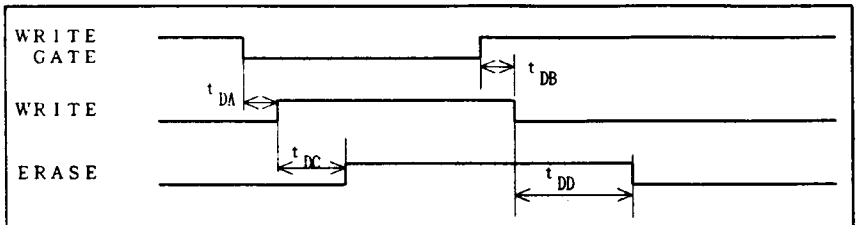


Figure 4.2.4 Erase Delay Control

Table 4.2.4a Erase Timing

NAME	P A R A M E T E R S	MIN	TYP	MAX	UNIT	REF.
tDA	Write Gate on to Write on	—	—	200	nS	
tDB	Write Gate off to Write off	—	—	200	nS	
tDC	Write Gate on to Erase on	Refer to Table 4.1a				
tDD	Write Gate off to Erase off	Refer to Table 4.1a				

4.2.5 Spindle Motor Control

The [+MTREN] is a "High level" when the system needs spindle motor rotation. The spindle motor is mainly controlled by the status of [-MTRON] input. Additional control is done at the automatic chucking operation.

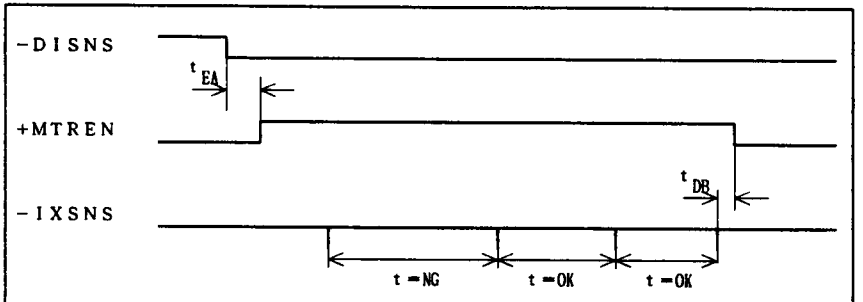


Figure 4.2.5a Auto Chucking Operation Timing

Table 4.2.5a Auto Chucking Operation Timing

NAME	PARAMETERS	MIN	TYP	MAX	UNIT	REF.
tEA	DISK-In to MOTOR on		0.7	1.7	mS	
tEB	READY to MOTOR off		0.7	1.7	mS	

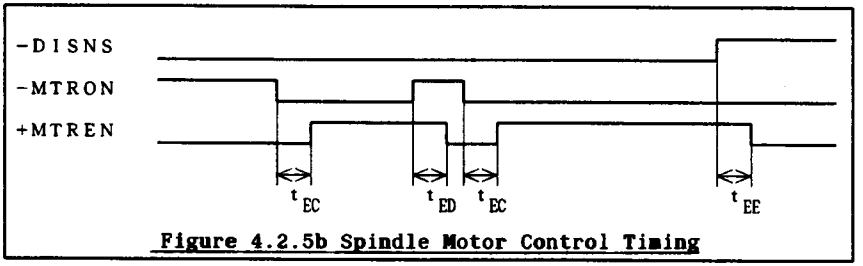


Figure 4.2.5b Spindle Motor Control Timing

Table 4.2.5b Spindle Motor Control Timing

NAME	PARAMETERS	MIN	TYP	MAX	UNIT	REF.
tEC	MOTOR on to MTREN off		0.7	1.7	mS	
tED	MOTOR off TO MTREN off	2.4	2.5	2.6	S	
tEE	DISK-In off to MTREN off		0.7	1.7	mS	

4.2.6 Head Load Control

[+HDEN] and [+HLPS] control head load solenoid. [+HDEN] is a "High level" when the head is loaded. A "High level" on the [+HDPS] means reducing idling current to the solenoid in a quiescent stage. This terminal is negate when [+HDEN] is turn to a "Low level", and is activated to a "High level" after several second elapsed.

The condition status of the head load is controlled by the combination of [-HLOAD] and [-HM/HD]. And also the status of Motor on and DISK-In is added to this condition. This is described as follows.

HDEN = ([-MRTON]="Low level") * ([-DISNS]="Low level") *
([-HLOAD]="Low level" * [-DS]="Low level" + [-HM/HD]="Low level")

Following table shows the HEAD LOAD condition.

HEAD LOAD INPUT PIN	[-HLOAD] connect to	[-HD/HM] connect to	Condition when [HDEN] is active
Use	HEAD LOAD	High(VDD)	(HEAD LOAD)*DS*MTRON*DISKIN
Use	HEAD LOAD	HEAD LOAD	(HEAD LOAD)*MTRON*DISKIN
Not Use	Low(GND)	High(VDD)	DS*MRTON*DISKIN
Not Use	High(VDD)	DS	DS*MRTON*DISKIN
Not Use	High(VDD)	Low(GND)	MRTON*DISKIN
Not Use	Low(GND)	Low(GND)	MRTON*DISKIN

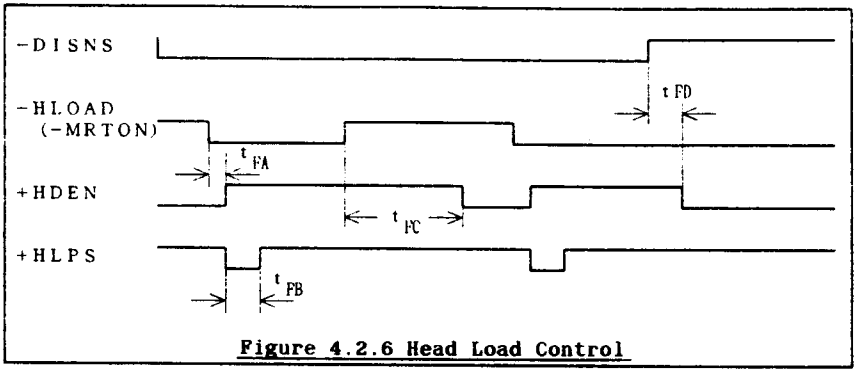


Figure 4.2.6 Head Load Control

Table 4.2.3 Head Load Solenoid Control Timing

NAME	PARAMETERS	MIN	TYP	MAX	UNIT	REF.
tFA	HEAD LOAD to +HDEN on		0.7	1.7	mS	
tFB	HEAD LOAD POWER Unsave Time	59.	60.	63.	mS	
tFC	HEAD LOAD off Delay Time	440	---	530	mS	
tFD	Disk Out to HEAD UNLOAD		0.7	1.7	mS	

4.2.7 Switch Filter Control

[+SWFIL] is prepared for adjusting the characteristics of a R/W analogue circuit characteristics.
The characteristics of the R/W circuit should be changed according to the track position processed. There are two method to compensate this.
One is to change frequency domain compensation in the read amplifier, it is called switch filter, and the other is reducing write current in the write amplifier.

Anyway this terminal will become active when the current head position is from 44 tracks to 80 tracks. In the view of minimizing the difference of characteristic between compensated track and non-compensated track, the ideal turning point of switch filter is 50 to 60 tracks. But in the view of compatibility among FDDs, it had better that the compensation is slight as possible. The FDMC chooses the latter one.
Additionally, in 48 TPI FDD used 2 PHASE/TRACK mode, [+SWFIL] becomes active at the same position as 96 TPI FDD.

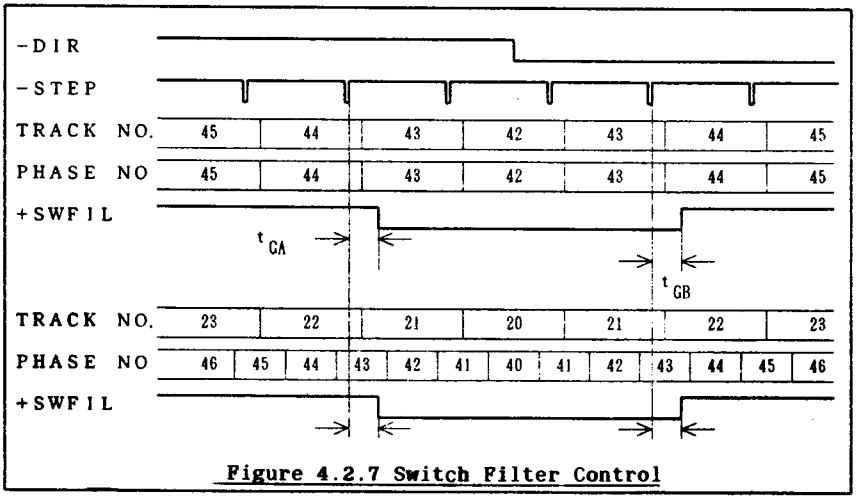


Figure 4.2.7 Switch Filter Control

Table 4.2.7 Switch Filter Control Timing

NAME	PARAMETERS	MIN	TYP	MAX	UNIT	REF.
tGA	Step to Switch Filter off		0.7	1.7	mS	
tGB	Step to Switch Filter on		0.7	1.7	mS	

5. ELECTRICAL CHARACTERISTICS

5.1 Absolute Maximum Rating

VSS = 0V (Gnd)

SYMBOL	I T E M	R A T I N G	UNIT
VDD	Supply Voltage	- 0.5 - 6.5	V
VIN	Input Voltage	- 0.5 - VDD+0.5	V
VOUT	Output Voltage	- 0.5 - VDD+0.5	V
Tstg	Storage Temperature	-55 - +125	°C
Topr	Operating Temperature	-30 - +70	°C
Iout1	Output Current each terminal	Output group 1 ± 3	mA
Iout2	Output Current each terminal	Output group 2 ± 6	mA
PD	Power Dissipation	300	mW

Note : If LSI is used above the maximum ratings, permanent destruction of LSI can result. In addition, it is desirable to use LSI for normal operation under the recommended conditions. If these conditions are exceeded, reliability of LSI may be adversely affected.

Output group 1
[+HLEN], [+SMPS], [+MTREN], [+LINUSE], [PHASE1], [PHASE2], [+HLPS], [+SWFIL].

Output group 2
[XOUT], [+DSOUT], [+HEADO], [+ERASE], [+WRITE], [+DS/RDY], [+WP], [+INDEX], [+TRK00], [+READY].

5.2 Recommended Operating Conditions

VDD = 5.0V, VSS = 0V

SYMBOL	I T E M	CONDITION	MIN	MAX	UNIT
Topr	Operating Temperature		-30	70	°C
VDD	Supply Voltage		4.5	5.5	V
fCLK	Clock Frequency		3.9	4.1	MHz

5.3 DC Characteristics

VDD = 5.0V, VSS = 0V, Topr=-30 to 70°C

SYMBOL	I T E M	C O N D I T I O N	MIN	TYP	MAX	UNIT
VHS1	Hysteresis Width (1)	Input terminal group 1	0.2	0.6		V
VHS2	Hysteresis Width (2)	Input terminal group 2	0.6	0.8		V
IIH1	Input High Current (1)	Input with pull up device	-20		20	uA
IIL1	Input Low Current (1)	Input with pull up device	-100		-20	uA
IIN	Input Current (2)	CMOS input gate	-20		20	uA
VIH1	Input High Voltage (1)	Input terminal group 1	2.1		VDD	V
VIL1	Input Low Voltage (1)	Input terminal group 1	0.0		0.6	V
VIH2	Input High Voltage (2)	Input terminal group 2	2.8		VDD	V
VIL2	Input Low Voltage (2)	Input terminal group 2	0.0		1.0	V
VIH3	Input High Voltage (3)	Input terminal group 3	3.5		VDD	V
VIL3	Input Low Voltage (3)	Input terminal group 3	0.0		1.5	V
IOH1	Output High Current(1)	VOH=4.6V Output group 1	--		-2.0	mA
IOL1	Output Low Current (1)	VOL=0.4V Output group 1	2.0		--	mA
IOH2	Output High Current(2)	VOH=4.6V Output group 2	--		-3.0	mA
IOL2	Output Low Current (2)	VOL=0.4V Output group 2	3.0		--	mA
IDD	Power Consumption	VDD=5.0V fC=4.0MHz	--	2.0	4.0	mA

Input terminal group 1
[-HD/HM],[-MTRON], [-HLOAD],[-WGATE], [S1SEL],[-DS],[-DIR], [-STEP], [-INUSE], [-STP], [-2TSP/+ARTZ]
Input terminal group 2
[-RESET], [-WPSNS], [-TZSNS], [-DISNS], [+DISNS], [IXSNS]
Input terminal group 3
[+TEST], [XIN], [-HOLD], [FWSEL-0], [FWSEL-1], [FWSEL-2], [FWSEL-3]
Output group 1
[+HLEN], [+SMPS], [+MTREN], [+LINUSE], [PHASE1], [PHASE2], [+HLPS], [+SWFIL].
Output group 2
[XOUT], [+DSOUT], [+HEAD0], [+ERASE], [+WRITE], [+DS/RDY], [+WP], [+INDEX], [+TRK00], [+READY].

5.4 AC Characteristics

Unless otherwise noticed, Ta=0°C to 70°C, VDD = 5.0 ± 0.5V

5.4.1 Pulse Width

SYMBOL	I T E M	MIN	TYP	MAX	UNIT
tWSP	Step pulse width	500			nS

5.4.2 Transmission Delay Characteristics

SYMBOL	I T E M				MIN	TYP	MAX	UNIT
tWEH	Write Gate Fall -> Write Enable Rise				-		200	nS
tWEL	Write Gate Rise -> Write Enable Fall				-		200	nS
tIFH	-DS Fall	->	+DSOUT	Rize				
		->	+DSKCHG	Rize				
		->	+WP	Rize	-	-	200	nS
		->	+INDEX	Rize				
		->	+READY	Rize				
tIFL	-DS Rize	->	+DSOUT	Fall				
		->	+DSKCHG	Fall				
		->	+WP	Fall	-	-	200	nS
		->	+INDEX	Fall				
		->	+READY	Fall				
tHDH	-SISEL Rize	->	+HEADO	Rize	-	-	200	nS
tHDL	-SISEL Fall	->	+HEADO	Fall	-	-	200	nS
tSNH	+IXSNS Rize	->	+INDEX	Rize				
	-WPSNS Fall	->	+WP	Rize	-	-	200	nS
tSNL	+IXSNS Fall	->	+INDEX	Fall				
	-WPSNS Rize	->	+WP	Fall	-	-	200	nS
tDS	(setup time) DIR from -STEP Fall				-	-	200	nS
tDH	(hold time) DIR from -STEP Fall				-	-	200	nS

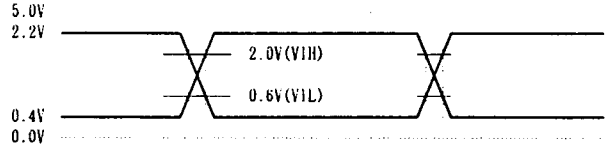
5.4.3 Testing Waveform

(VDD = 5.0V)

LSTTL Equivalence Input

Input terminal group 1

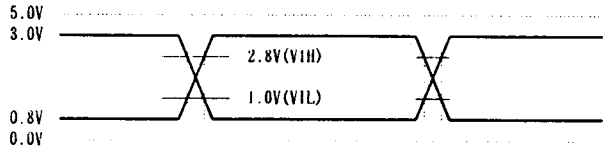
[-HD/HM], [-MTRON], [-HLOAD], [-WGATE], [SISEL], [-DS], [-DIR], [-STEP], [-INUSE], [-STP], [-INUSE], [-2STP/-ARTZ]



Sensor Input Terminals

Input terminal group 2

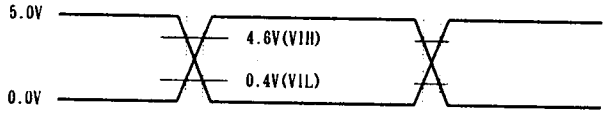
[-RESET], [-WPSNS], [-TZSNS], [-DISNS], [+IXSNS]



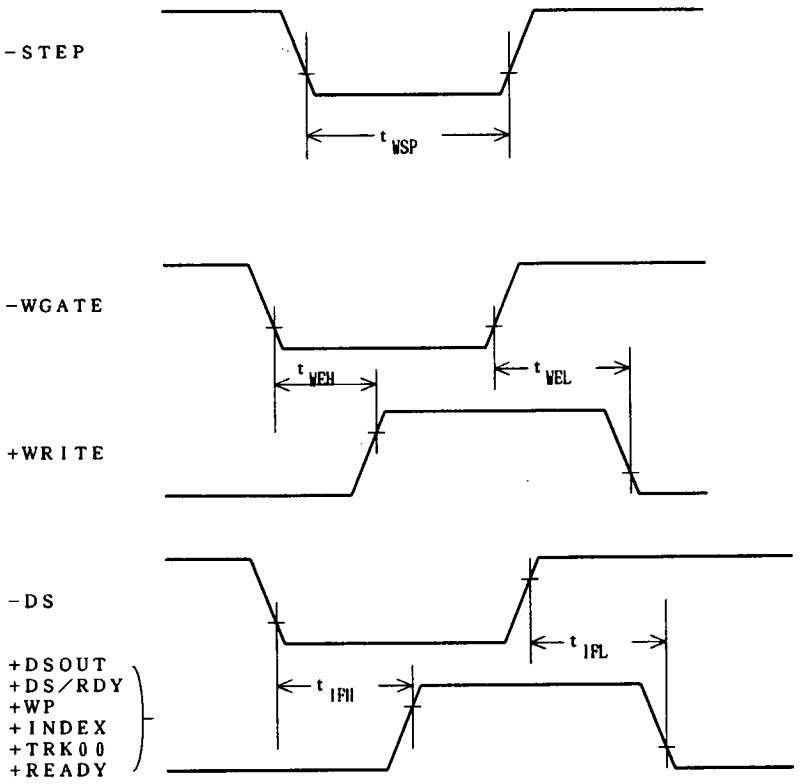
Other Input Terminals

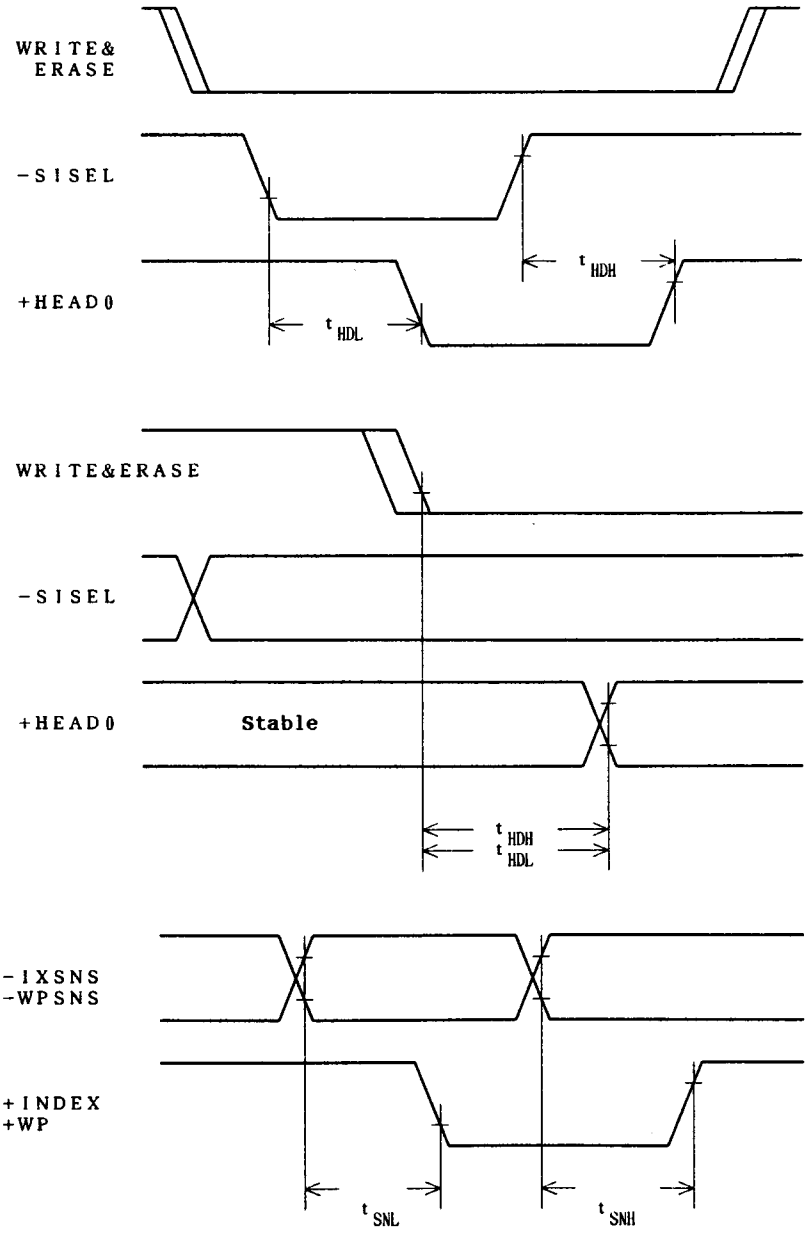
Input terminal group 3

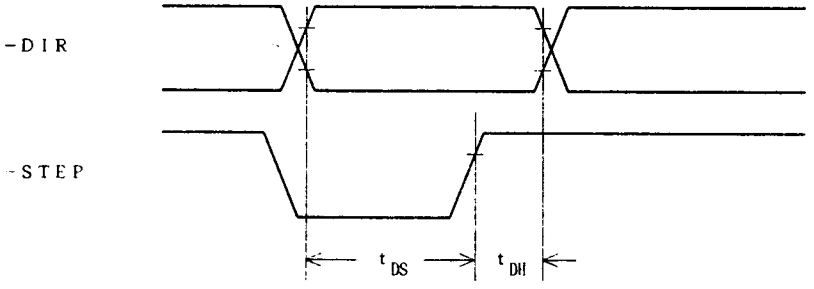
[+TEST], [XIN], [-HOLD], [FWSEL-0], [FWSEL-1], [FWSEL-2], [FWSEL-3]



5.4.4 Timing Waveform

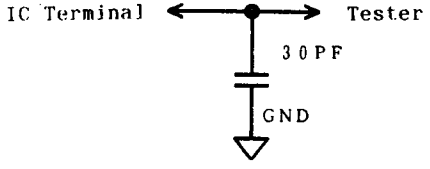



WRITE&
ERASE
-SISEL
+HEAD0
t HDH
t HDL
WRITE&ERASE
-SISEL
+HEAD0
Stable
t HDH
t HDL
-IXSNS
-WPSNS
+INDEX
+WP
t SNL
t SNH



5.4.5 Testing Terminal Load

Apllied to CMOS output terminal.



6. 44 PIN mini FP (Flat Package)

UNIT : mm