

## Low Current Consumption FM IF Amplifier for Pagers

### Description

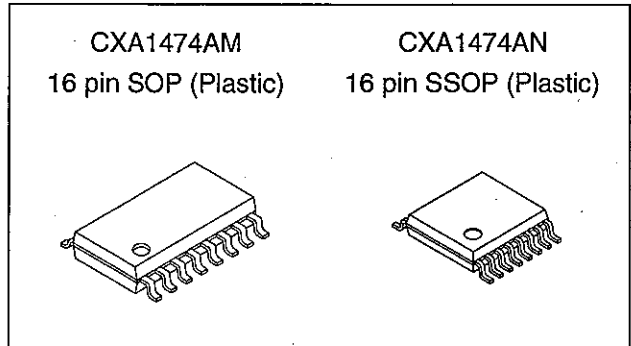
The CXA1474AM/AN is a low current consumption FM IF amplifier which employs the newest bipolar process. It is suitable for such sets as Japan single conversion pagers which require low current consumption.

### Features

- Low current consumption 720 $\mu$ A (typ. at Vcc = 1.5V)
- Low voltage operation Vcc = 1.0 to 4.0V
- Few external parts for needless of IF decoupling capacitor
- Built-in reference power supply for operational amplifier and comparator
- Small package 16-pin SSOP
- IF input Vcc standard

### Functions

- Second IF and limiter amplifiers
- FM detector
- Quaternary LPF operational amplifier
- FSK comparator
- Regulator output for RF amplifier and first mixer
- Power-save function
- Reduced voltage detection circuit



### Applications

Single super pagers for Japan and overseas

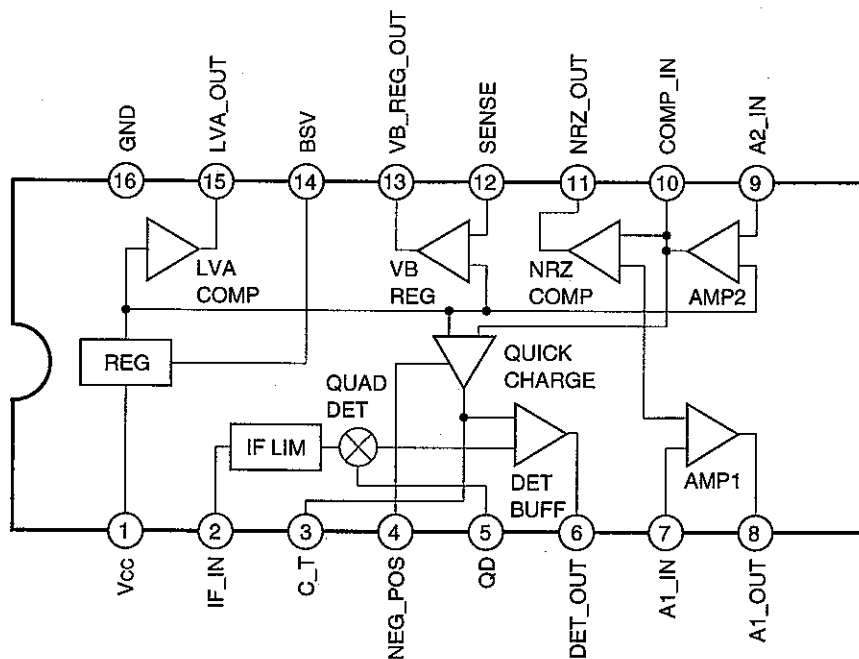
### Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	Vcc	7.0	V
• Operating temperature	Topr	-20 to +75	°C
• Storage temperature	Tstg	-65 to +150	°C

### Operating Condition

Supply voltage	Vcc	1.0 to 4.0	V
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### Block Diagram



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Pin Description

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
1	Vcc			Power supply.
2	IF_IN	1.5V		IF limiter amplifier input.
3	C_T	0.2V		Connects a capacitor that determines the low cut-off frequency for the entire system.
4	NEG_POS	0V		Controls the ON/OFF operation of the quick-charge circuit. (Applied voltage range: -0.5 to +7.0V)
5	QD	1.5V		Connects the phase shifter of FM detector circuit.

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
6	DET_OUT	0.2V		FM detector output.
7 9	A1_IN A2_IN	0.2V 0.2V		Input for operational amplifiers 1 and 2 (AMP1, AMP2).
8	A1_OUT	0.2V		Output for operational amplifier 1 (AMP1).
10	COMP_IN	0.2V		NRZ comparator input. Output for operational amplifier 2 (AMP2) is connected.

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
11 15	NRZ_OUT LVA_OUT	— —		NRZ and LVA comparator outputs and they are open collectors. (Applied voltage range -0.5 to +7.0V)
12	SENSE	0.2V		Input for internal constant-voltage source amplifier. This pin is controlled to maintain 200mV.
13	VB_REG_OUT	—		Output pin for internal constant-voltage source amplifier. Connect the base of PNP transistor. (Current capacity: 100μA)
14	BSV	—		Controls the battery saving. Setting this pin low suspends the operation of IC. (Applied voltage range: -0.5 to +7.0V)
16	GND	—		Ground

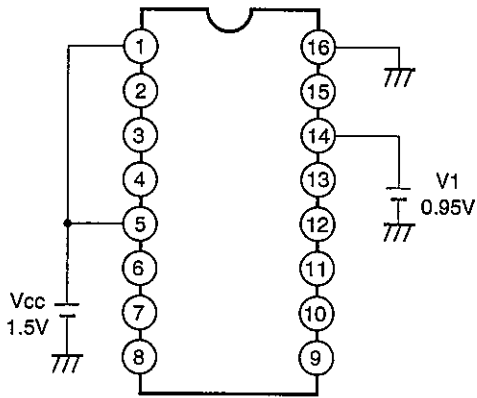
**Electrical Characteristics** ( $V_{CC} = 1.5V$ ,  $T_a = 25^\circ C$ ,  $F_s = 455kHz$ ,  $F_{MOD} = 256Hz$ ,  $F_{DEV} = 2.3kHz$ ,  $AM_{MOD} = 30\%$ )

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Current consumption	I <sub>CC</sub>	Measurement circuit 1	500	720	930	μA
Current consumption	I <sub>CCS</sub>	Measurement circuit 1, $V_1 = 0.3V$			20	μA
AM rejection ratio	AMRR	Measurement circuit 3, $V_{IN} = 60dB\mu$	25			dB
Op amp. input bias current	I <sub>BIAS</sub>	Measurement circuit 2		40	100	nA
Op amp. open loop gain	A <sub>v</sub>	Measurement circuit 4	45			dB
Op amp. output voltage amplitude	V <sub>O</sub>	Measurement circuit 5	0.65			V <sub>p-p</sub>
NRZ output saturation voltage	V <sub>SATNRZ</sub>	Measurement circuit 8			0.4	V
NRZ output leak current	I <sub>LNRZ</sub>	Measurement circuit 7			5.0	μA
NRZ hysteresis width	V <sub>TWNRZ</sub>	Measurement circuit 6	5	10	15	mV
VB output current	I <sub>OUT</sub>	—	100			μA
VB output saturation voltage	V <sub>SATVB</sub>	Measurement circuit 9			0.4	V
VB SENSE voltage	V <sub>SENVB</sub>	—	200	215	230	mV
LVA operating voltage	V <sub>LVA</sub>	Measurement circuit 10, NRZ_COMP operation	1.05	1.10	1.15	V
LVA output leak current	I <sub>LLVA</sub>	Measurement circuit 10			5.0	μA
LVA output saturation voltage	V <sub>SATLVA</sub>	Measurement circuit 8			0.4	V
Detector output voltage	V <sub>ODET</sub>	Measurement circuit 3	21	28	38	mV
Logic input voltage high level	V <sub>THBSV</sub>		0.9			V
Logic input voltage low level	V <sub>TLBSV</sub>				0.35	V
Limiting sensitivity	V <sub>IN (LIM)</sub>	Measurement circuit 3		17	24	dBμ

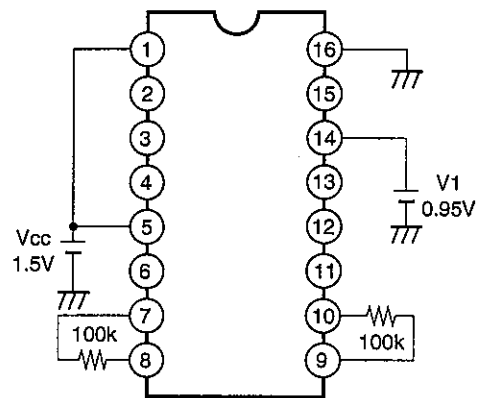
**Design Data**

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
IF limiter input resistance	R <sub>INLIM</sub>		1.6	2.0	2.4	kΩ
Op amp. minimum input voltage					0.05	V
Comparator minimum input voltage					0.05	V
LVA hysteresis	V <sub>THLVA</sub>	Measurement circuit 10, NRZ_COMP operation		10		mV

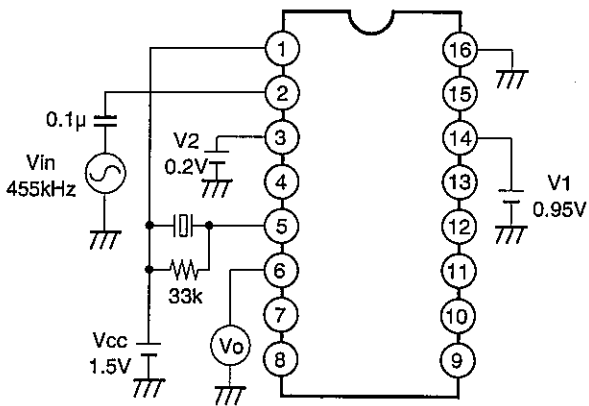
Measurement Circuit



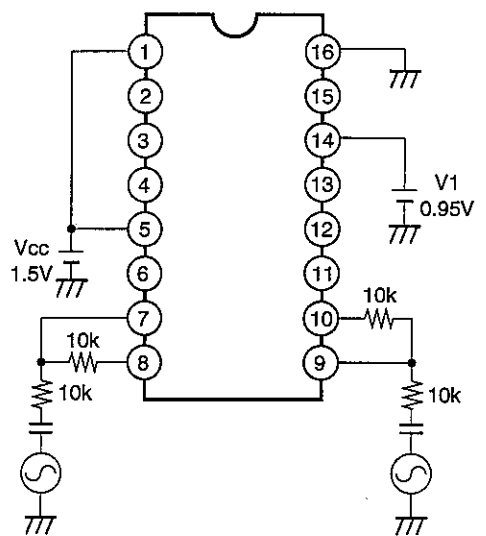
Measurement circuit 1



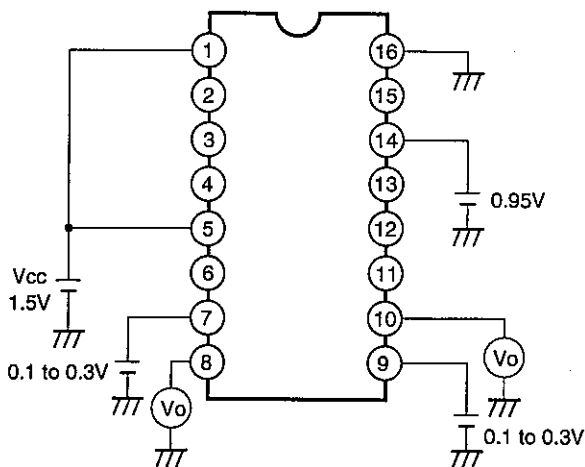
Measurement circuit 2



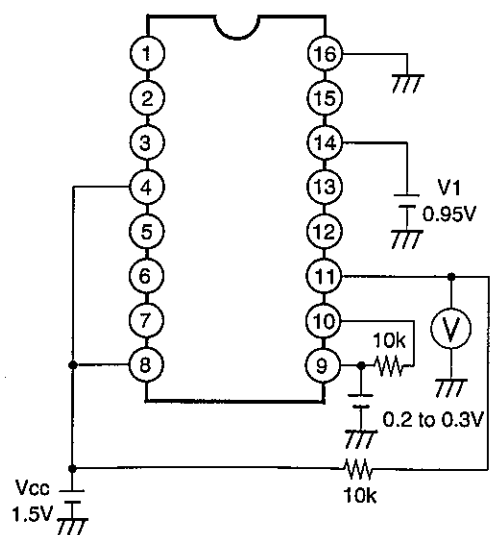
Measurement circuit 3



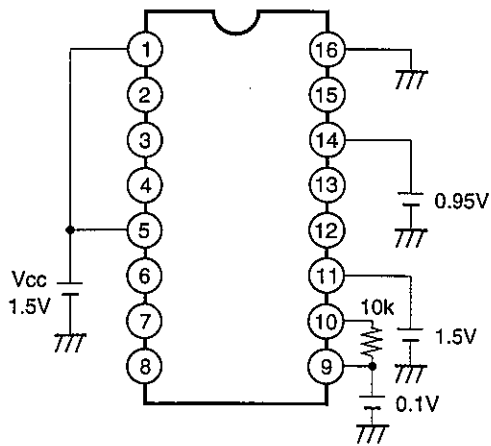
Measurement circuit 4



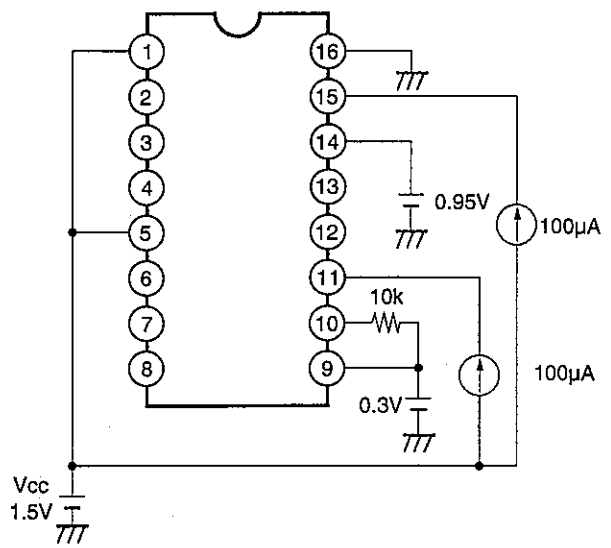
Measurement circuit 5



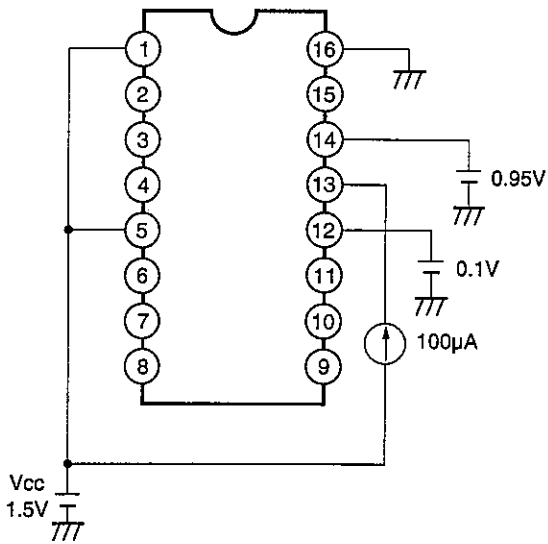
Measurement circuit 6



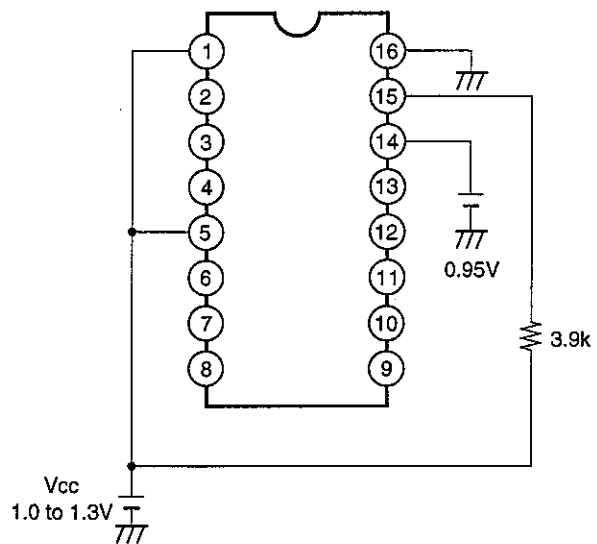
Measurement circuit 7



Measurement circuit 8



Measurement circuit 9



Measurement circuit 10

**1) Power Supply**

The CXA1474AM/AN, with built-in regulator, is designed to permit stable operation at wide range of supply voltage from 1.0 to 4.0V. Decouple the wiring to Vcc (Pin 1) as close to the pin as possible.

**2) IF Filter**

The filter to be connected between IF limiters should have the following specifications.

- Output impedanc: 2.0kΩ ± 10%
- Band width: Changes according to applications

**3) IF Limiter Amplifier**

The gain of this IF limiter amplifier is approximately 100dB. Take notice of the following points in making connection to the IF limiter amplifier input pin (Pin 2).

- a) Be sure the wire to the IF limiter amplifier input (Pin 2) is as short as possible.
- b) As the limiter amplifier output appears at QD (Pin 5), be sure the wire to the RLC and ceramic discriminator connected to QD is as short as possible and reduce the interference with the IF limiter amplifier input.

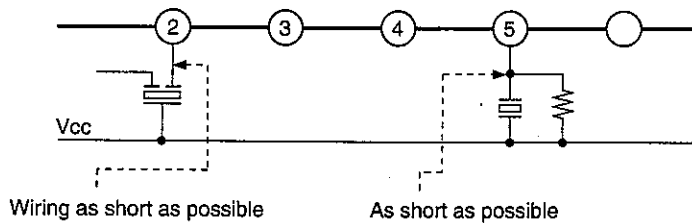


Fig. 1

**4) Quick Charge**

In order to hasten the rising time from when power is turned on or when reception standby, the CXA1474AM/AN features a quick charge circuit.

Therefore, the quick charge circuit eliminates the need to insert a capacitor between the detector output and the LPF as is the case with conventional ICs, but connects a capacitor to Pin 3 to determine the average signal level during steady-state reception. The capacitance of the capacitor connected to Pin 3 should be chosen such that the voltage does not vary much due to discharge during battery saving.

Connect a signal for controlling the quick charge circuit to Pin 4. Setting this pin high enables the quick charge mode, setting this pin low enables the steady-state reception mode. Quick charge is used when the power supply is turned on. The battery saving must be set high at the time. Quick charge is also used according to need during battery saving.

Connect Pin 4 to GND when quick charge is not being used.

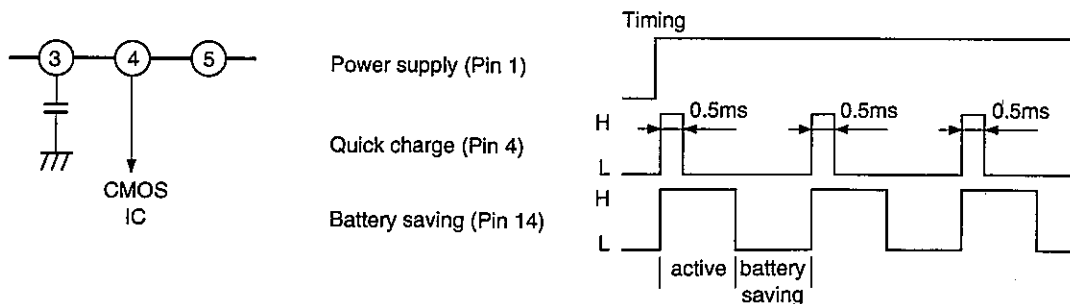


Fig. 2

5) Detector

The detector is of quadrature type. To perform phase shift, connect RLC resonator circuit or ceramic discriminator to Pin 5.

The phase shifting capacitor for the quadrature detector is built in.

The demodulated FM (FSK) signal from the detector will have its high-frequency component eliminated through the LPF of the DET-BUFF and then fed to DET-OUT (Pin 6).

DET-OUT output impedance is 200Ω or less.

The CDBM455C25 (MURATA MFG. CO., LTD.) ceramic discriminator for the CXA1474AM/AN is recommended.



Fig. 3

6) AMP, NRZ-OUT

Two operational amplifiers are built in this IC.

One of them is connected internally to an NRZ comparator.

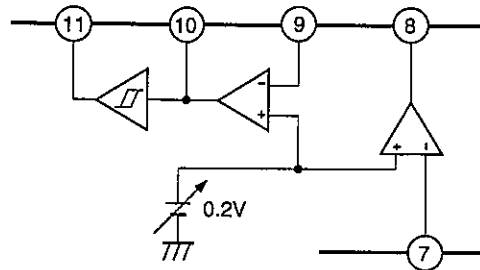


Fig. 4.

Using these two operational amplifiers to construct an LPF, remove noise from the demodulated signal and input to the NRZ comparator, which is the next stage.

The NRZ comparator molds waveform of this input signal and outputs it as a square wave. the NRZ comparator output stage is for open collector.

Thus, if the CPU is of CMOS-type and the supply voltage is different, a direct interface as illustrated in the figure below can be implemented.

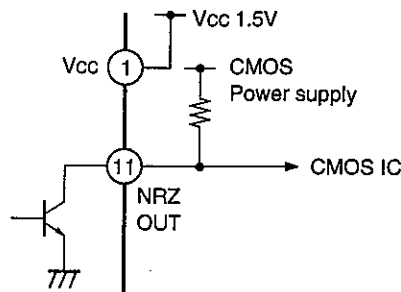


Fig. 5

7) SENE, VB\_REG-OUT

Controls the base bias of the external transistors.

8) LVA-OUT

This pin goes high (open) when the supply voltage becomes low. Since the output is an open collector, it can be used to directly drive CMOS device as can NRZ-OUT. The setting voltage of the LVA is 1.10V (typ.), and it possesses a hysteresis with respect to the supply voltage. The hysteresis width is 10mV (typ.).

9) BSV

Operation of the CXA1474AM/AN can be halted by setting this pin low. This pin can be connected directly to CMOS device. The current consumption for BSV is 20μA or less (at 1.5V).

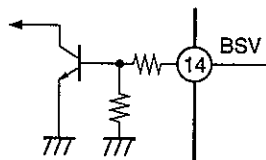


Fig. 6

Principle of Quick Charge Operation

BUF in Fig. 7 is the detector buffer amplifier, and AMP1 and AMP2 are operational amplifiers to construct an LPF. COMP is the NRZ comparator. Coupling on conventional system is performed by placing a capacitor between the detector buffer and the LPF operational amplifier, matching of DC is not performed. Thus, this matching capacitor must be charged when restoring the system from reception standby mode to reception mode, within which time signals from the comparator appear at the NRZ output.

To shorten this rise time, as shown in Fig. 7 the CXA1474AM/AN adds feedback loop from the comparator input to the input circuit of output. This equalizes the average value of the comparator input voltage to the reference voltage, with the quick charge circuit of CHG being set inside the feedback loop. Switching the current of quick charge circuit enables reduction of the rise time.

In this block, CHG is a comparator which compares the input voltage and outputs the current based on this comparison. The current on CHG is switched between high and low at Pin 4. To shorten the time constant when switching from reception standby mode to reception mode, switch the current to high and increase the charge current at C in Fig. 7. During steady-state reception mode, switch the current to low, lengthening the charge time constant, and allowing for stable data retrieval.

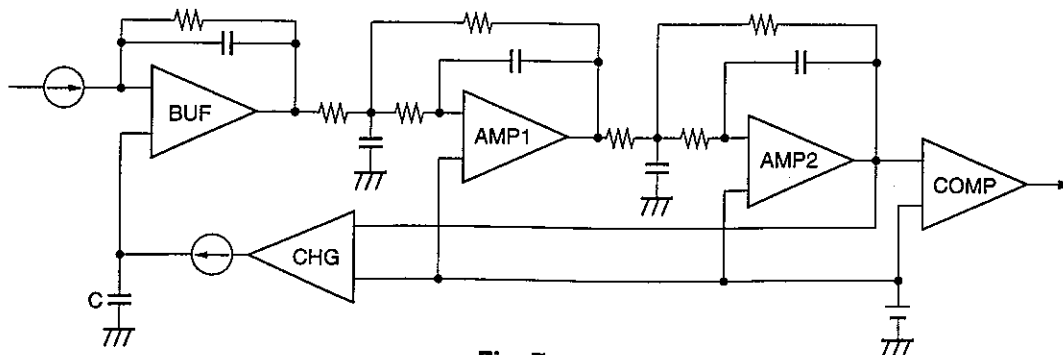


Fig. 7

[CXA1474AM/AN data filter constant settings]

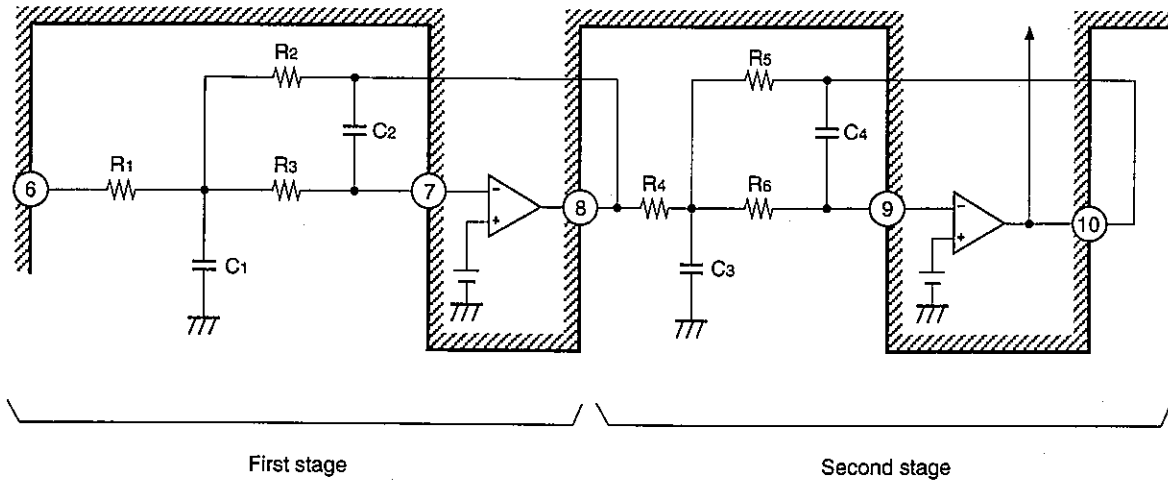


Fig. 8

<Method for determining the circuit constants>

The data filter cut-off frequency  $f_c$  (Hz) is determined according to the data speed. By first determining the value of the capacitor  $C_1 (= C_3)$ , the parameter  $K$  is determined.

$$K = \frac{100}{f_c C'} \quad \text{where } C' \text{ is the value of } C_1 \text{ expressed in } \mu\text{F}.$$

If the value of  $K$  calculated in this way is multiplied by the appropriate value from the following table, the required characteristics are obtained.

Circuit Constant Values

Part symbol	Gain of each stage (dB)	
	0	6
R <sub>1</sub> , R <sub>4</sub>	3.374	2.530
R <sub>2</sub> , R <sub>5</sub>	3.374	5.060
R <sub>3</sub> , R <sub>6</sub>	3.301	3.301
C <sub>2</sub> , C <sub>4</sub>	0.15C <sub>1</sub>	0.1C <sub>1</sub>

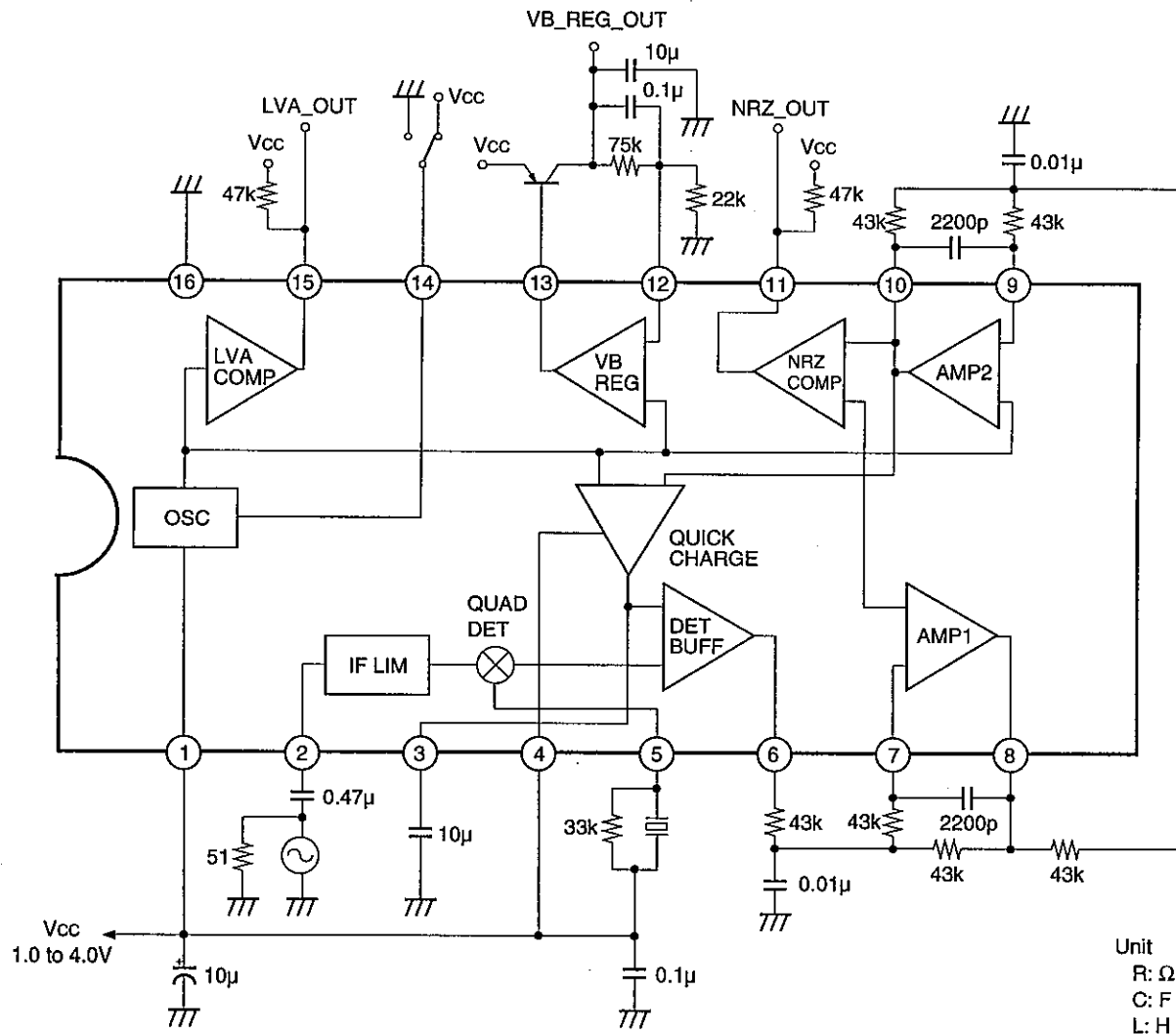
Resistance when parameter  $K = 1$  (Unit:  $k\Omega$ )

Ex.) Assuming  $f_c = 768\text{Hz}$  ( $256\text{Hz} \times 3$ ) and  $C_1 (= C_3) = 0.01\mu\text{F}$

$$K = \frac{100}{768 \times 0.01} \approx 13.0$$

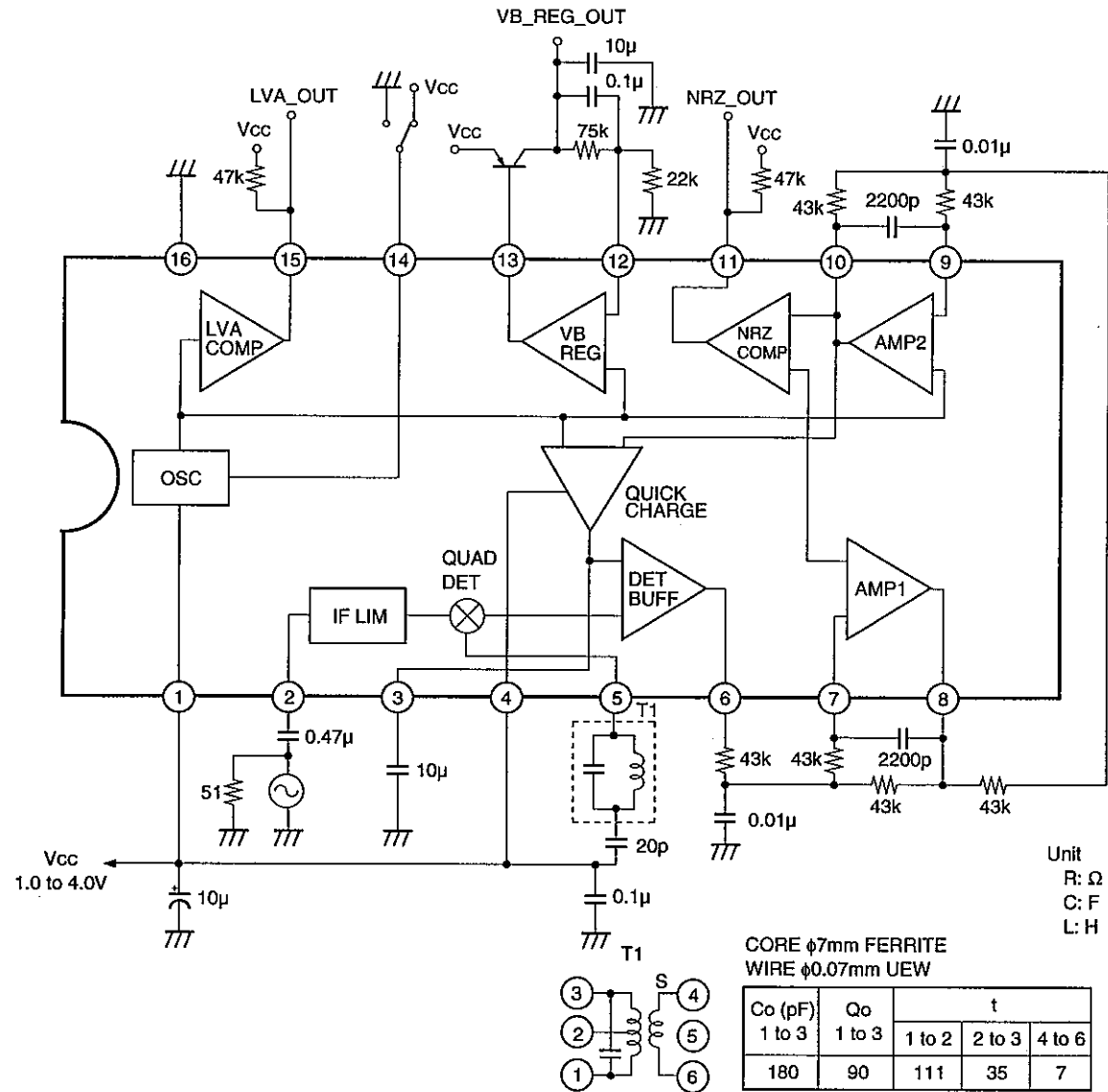
The usable resistances and capacitances derived from this  $K$  value and above table are indicated in the following Application Circuit.

Application circuit 1



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

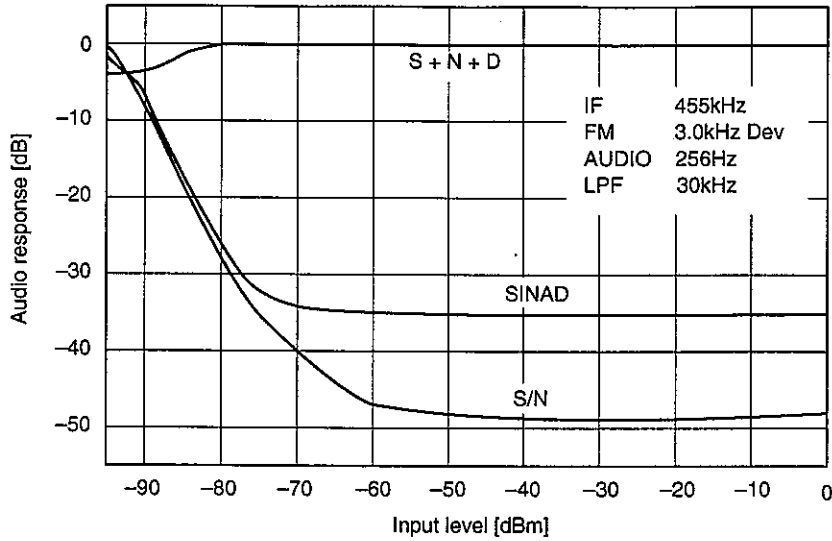
Application circuit 2



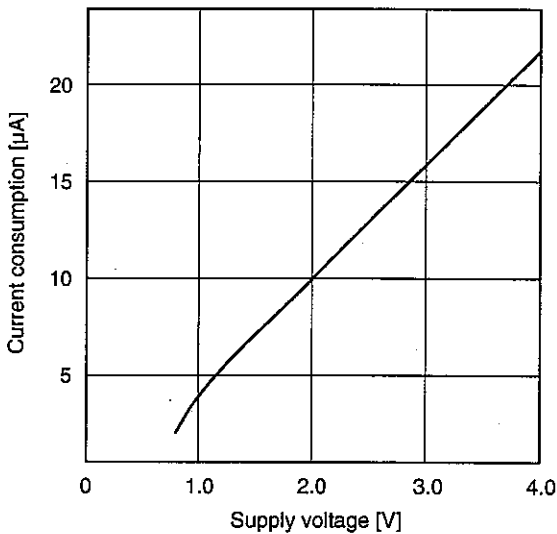
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Example of Representative Characteristics

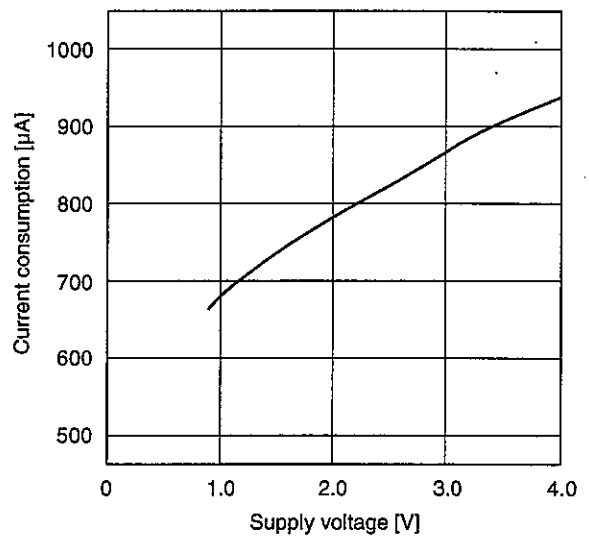
Input/output characteristics (at Pin 10)



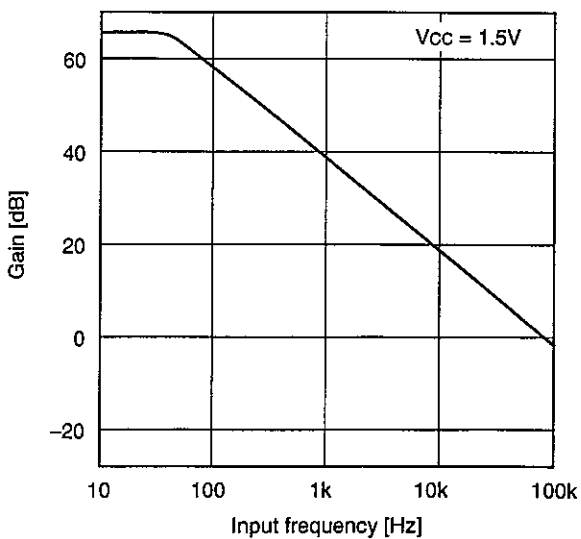
Supply voltage vs. Current consumption (battery saving mode)



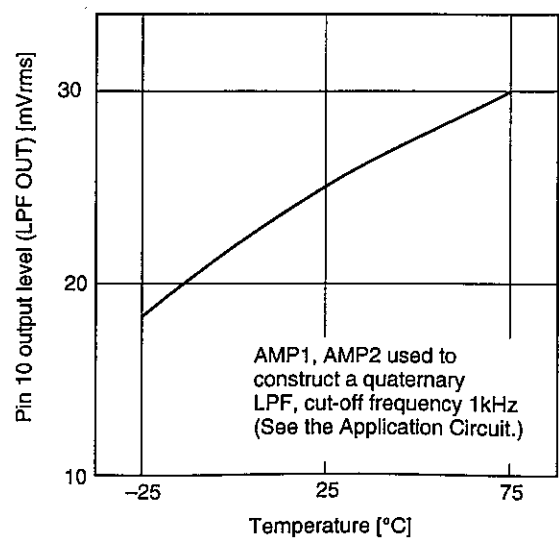
Supply voltage vs. Current consumption



Operational amplifier input frequency vs. Gain



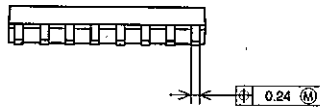
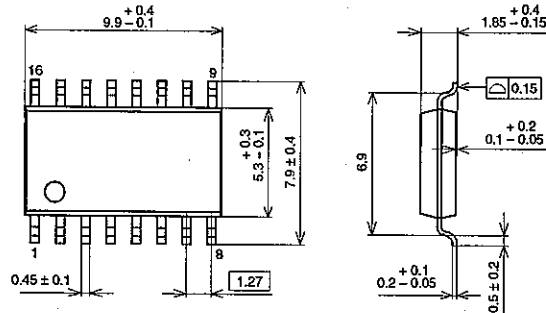
Pin 10 output level vs. Temperature



Package Outline Unit: mm

CXA1474AM

16PIN SOP (PLASTIC)



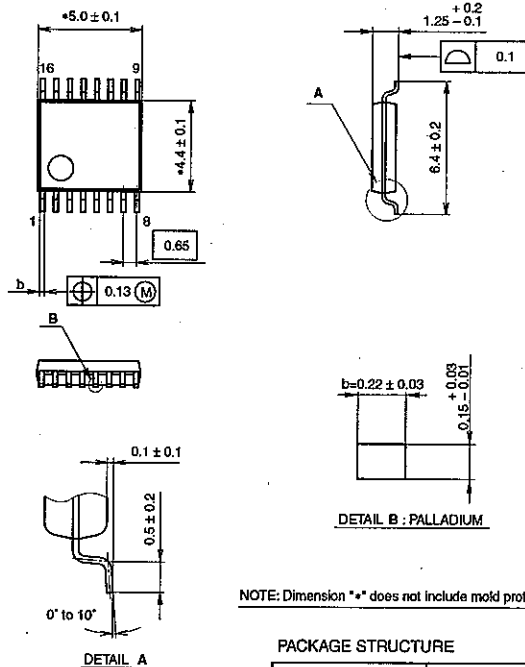
SONY CODE	SOP-16P-L01
EIAJ CODE	SOP016-P-0300
JEDEC CODE	

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.2g

CXA1474AN

16PIN SSOP (PLASTIC)



NOTE: Dimension "\*" does not include mold protrusion.

SONY CODE	SSOP-16P-L01
EIAJ CODE	P-SSOP16-4.4x5.0-0.65
JEDEC CODE	

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	PALLADIUM PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.1g