S3097

DEVICE SPECIFICATION

SONET/SDH/ATM OC-192 16:1 Low Power Transmitter

FEATURES

- Low power operation
- Silicon Germanium BiCMOS technology
- Complies with Telcordia and ITU-T specifications
- Integrated Phase Lock Loop
- Supports OC-192 to OC-192 with Forward Error Correction (FEC) rates
- Supports G.709 and 10 Gigabit Ethernet rates
- VCO Tunable from 9.953 GHz to 10.709 GHz
- 622.08 MHz REFCLK input (or equivalent FEC rate)
- 16-bit parallel, 622.08 Mbps LVDS data path (or equivalent FEC rate)
- 155.52/622.08 MHz clock outputs (or equivalent FEC rate)
- 311.04 MHz or 622.08 MHz parallel input clock (or equivalent FEC rate)
- Programmable skew on 311.04 MHz parallel input clock
- Lock error/phase error indicator
- Low jitter CML Differential or Single-Ended serial interface
- Self initilaizing internal FIFO to decouple transmit clocks
- Power 1.9 W (typ)
- Compact 15 mm x 15 mm 148-pin CBGA package

APPLICATIONS

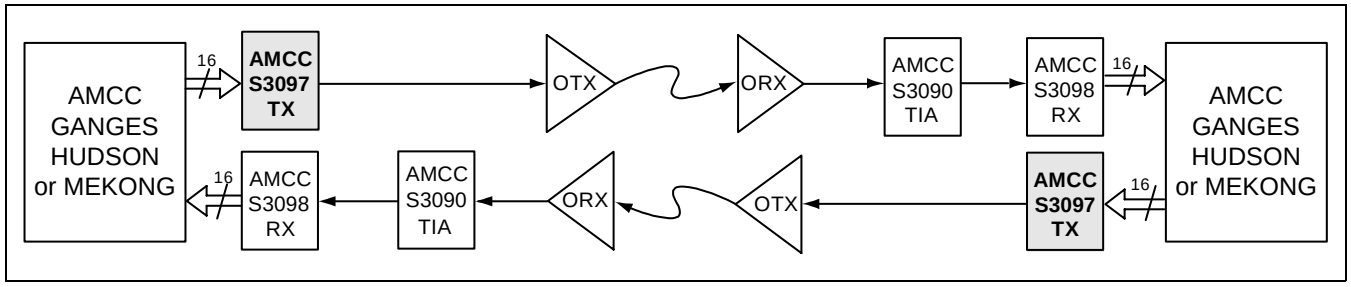
- SONET/SDH-based transmission systems
- SONET/SDH modules
- SONET/SDH test equipment
- ATM over SONET/SDH
- Section repeaters
- Add Drop Multiplexers (ADM)
- Broad-band cross-connects
- Fiber optic terminators
- Fiber optic test equipment

GENERAL DESCRIPTION

The S3097 OC-192 16:1 low power transmitter is a fully integrated serialization device. The chip performs all necessary parallel-to-serial functions in conformance with SONET/SDH transmission standards. The device is suitable for SONET-based ATM applications. Figure 1, *System Block Diagram*, shows a typical network application.

On-chip clock synthesis PLL components are contained in the S3097 Multiplexer (MUX) chip, allowing the use of a slower external transmit clock reference. The chip can be used with a 622.08 MHz (or equivalent FEC rate) reference clock, in support of existing system clocking schemes.

Figure 1. System Block Diagram



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S3097 OVERVIEW

The S3097 transmitter implements SONET/SDH serialization and transmission functions. This chip can be used to implement the front end of SONET equipment, which consists primarily of the serial transmit interface and the serial receive interface. The chip includes parallel-to-serial conversion and system timing. The system timing circuitry consists of a high-speed phase detector, clock dividers, and clock distribution throughout the front end. The sequence of transmitter operations is as follows:

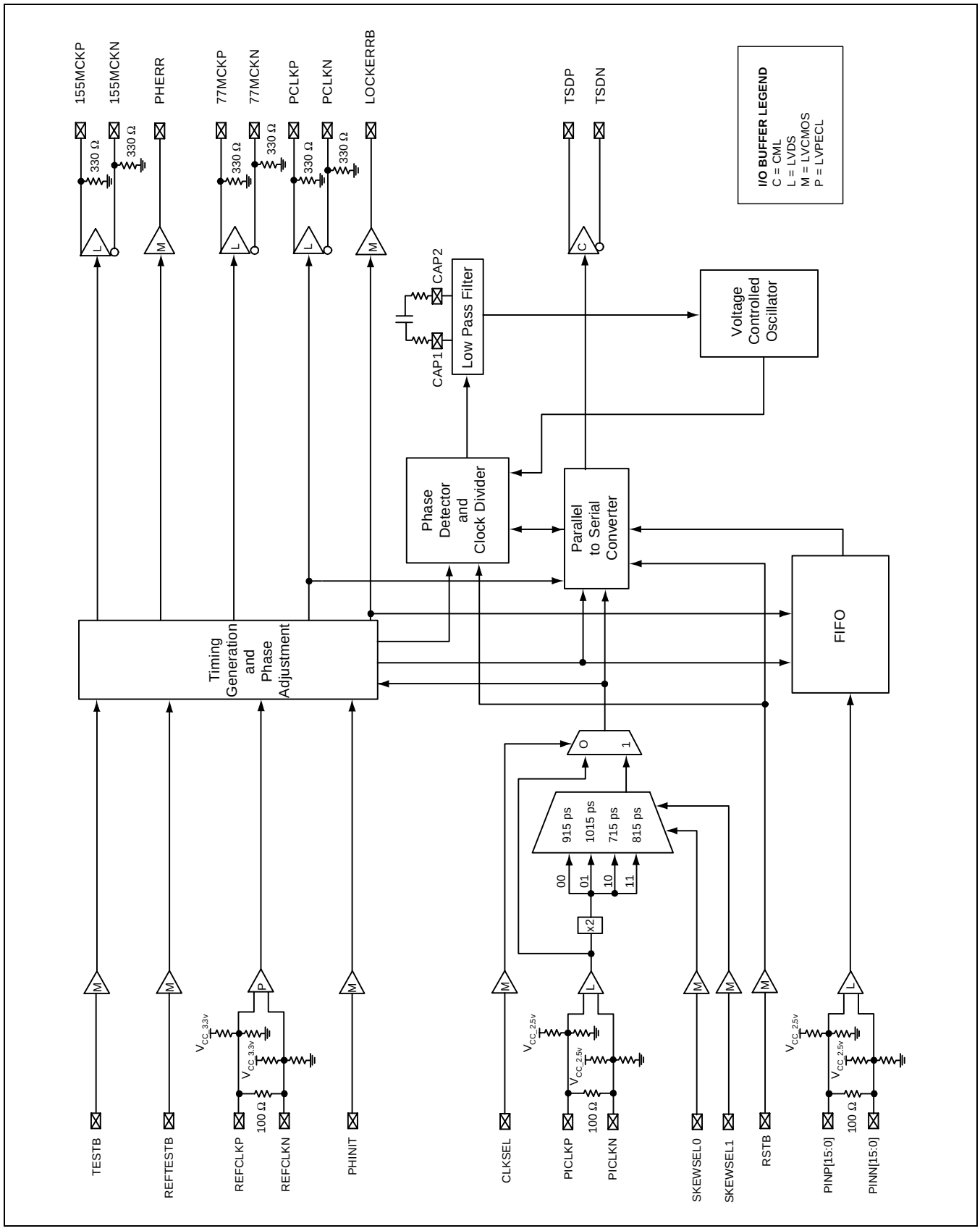
1. 16-bit parallel input
2. Parallel-to-serial conversion
3. Serial output

Internal clocking and control functions are transparent to the user. Details of data timing can be seen in Figure 6, *AC Input Timing (PICLKP/N = 622.08 MHz to 669.33 MHz)* and Figure 7, *AC Input Timing (PICLKP/N = 311.04 MHz to 334.67 MHz)*.

Suggested Interface Devices

AMCC	GANGES (S19202)	OC-192 SONET/SDH Mapper
AMCC	GANGES II (S19202CBI20)	OC-192 SONET/SDH Mapper
AMCC	HUDSON (S19203)	Digital Wrapper
AMCC	MEKONG (S19204)	OC-192 Pointer Processor
AMCC	S2509	SONET Digital Wrapper Backplane SERDES
AMCC	S3090	OC-192 Transimpedance Amp
AMCC	S3098	OC-192 CDR + DeMUX
AMCC	S3099	10 Gbps EAM Driver

Figure 2. Functional Block Diagram



S3097 PIN DESCRIPTION

Parallel Input Data (PINP/N[15:0])

PINP/N[15:0] is the parallel LVDS data input bus which is multiplexed 16:1 and transmitted serially at OC-192 rates. This data is aligned with the Parallel Input Clock (PICLKP/N). Bit 15 is the most significant bit. These pins are internally biased and terminated. This bus is typically connected to a framer, mapper or digital wrapper (e.g. GANGES, GANGES II, MEKONG or HUDSON).

Parallel Input Clock (PICLKP/N)

PICKLP/N is the LVDS 311.04 MHz or 622.08 MHz (or equivalent FEC Rate) input clock to which the Parallel Input Data (PINP/N[15:0]) is aligned. This clock is used to transfer the data from the inputs to a holding register in the internal parallel-to-serial converter. This input is internally biased and terminated.

Factory Test (TESTB, REFTESTB, 77MCKP/N)

The LVCMOS Test Clock Enable (TESTB), LVCMOS Reference Test (REFTESTB) and LVDS 77.76 MHz Output Clock (77MCKP/N) pins are for factory test purposes only. For normal operation, connect TESTB and REFTESB to $V_{CC\_2.5\ V}$ through a 10 kΩ resistor. The 77MCKP/N output may be left unconnected.

Reference Clock (REFCLKP/N)

The differential LVPECL 622.08 MHz (or equivalent FEC Rate) Reference Clock (REFCLKP/N) input is used to establish the operating frequency of the clock recovery Phase Lock Loop (PLL). This input is internally biased and terminated. See Table 1, *Reference Frequency.*

Reset (RSTB)

The LVCMOS master Reset (RSTB) pin, when asserted Low, asynchronously resets the device. For normal operation, connect to $V_{CC\_2.5\ V}$ through a 10 kΩ resistor. This should be active for 100 ns to accurately reset the device.

Loop Filter (CAP1, CAP2)

The external loop filter capacitor and resistors are connected to these pins. These devices should be surrounded by a ground shield. The components value are as stated in Table 19, *External Loop Filter Components.*

Table 1. Reference Frequency

Increased Serial Data Output (TSD) Frequency	Required (REFCLK) Frequency
9.953 Gbps	622.08 MHz
10.234 Gbps	639.62 MHz
10.317 Gbps	644.84 MHz
10.402 Gbps	650.12 MHz
10.488 Gbps	655.48 MHz
10.575 Gbps	660.96 MHz
10.664 Gbps	666.51 MHz
10.709 Gbps	669.33 MHz

Phase Initialization (PHINIT)

The active High LVCMOS Phase Initialization (PHINIT) pin is an asynchronous input that initializes the internal phase adjust circuit. When active, this pin recenters the internal First-In First-Out (FIFO) register. PHINIT must remain active for 10 ns to recenter the FIFO. PHINIT must be asserted if the PHERR signal is active, indicating potential internal setup/hold timing violations. During this initialization, four to ten bytes of data may be lost. See Figure 8, *Phase Adjust Timing*.

Clock Select (CLKSEL)

The LVCMOS Clock Select (CLKSEL) input is used to select between the 622.08 and 311.04 MHz frequencies (or equivalent FEC rate) on the PICLKP/N input. See Table 2, *Clock Select.*

Table 2. Clock Select

CLKSEL	PICLK FREQUENCY
0	622.08 MHz (or equivalent FEC rate)
1	311.04 MHz (or equivalent FEC rate)

155.52 MHz Clock Output (155MCKP/N)

The LVDS 155.52 MHz Clock Output (or equivalent FEC rate) (155MCKP/N) pin is an internally generated clock output used to drive the reference clock input of an external Clock and Data Recovery unit (CDR) (e.g. as found in the S3098). This output is internally terminated with 330 Ω to ground (GND).

Lock Error/Phase Error (LOCKERRB)

The LVCMOS Lock Error/Phase Error (LOCKERRB) output will be inactive once the internal PLL has locked to the clock provided on the REFCLK input. Once lock detect has been achieved, the pin is used as an indicator of a phase error condition between the input PICLK phase and the internally generated byte clock phase. See PHERR and PHINIT pin descriptions for further explanation of this function.

Phase Error (PHERR)

The LVCMOS Phase Error (PHERR) output will be asserted High at the start of a PCLK cycle for which there may be setup/hold timing violations between the PICLK and internal byte clock timing domains. Minimum pulse width for this output is four to ten byte clocks (byte clock = 622.08 MHz (or equivalent FEC rate)). This output is normally connected to the PHINIT input.

Skew Select (SKEWSEL[1:0]) (311.04 MHz Mode Only)

The LVCMOS Skew Select (SKEWSEL[1:0]) inputs control the PICLK skew relative to the PINP/N[15:0] data. The nominal skew is 915 ps. The nominal skew setting (SKEWSEL[1:0] = 00) allows the internally generated sampling clock to be placed in the center of the data valid window. The skew may be varied from 715 ps to 1015 ps. See Table 3, *Skew Select*. See Table 18, *AC Transmitter Timing Characteristics*, and Figure 7, *AC Input Timing*, for diagram and timing specifications.

Table 3. Skew Select

SKEWSEL[1]	SKEWSEL[0]	311.04 MHz PICLK Target Skew
0	0	915 ps
0	1	1015 ps
1	0	715 ps
1	1	815 ps

Transmit Serial Data (TSDP/N)

The differential CML Transmit Serial Data (TSDP/N) are the serialized version of the incoming parallel data stream.

Parallel Clock (PCLKP/N)

The LVDS Parallel Clock (PCLKP/N) output is a 622.08 MHz (or equivalent FEC rate) internally generated clock output used to coordinate parallel data transfers with upstream logic. This output is internally terminated with 330 Ω to ground (GND).

S3097 FUNCTIONAL DESCRIPTION

Multiplexer Operation

The S3097 performs the serializing stage in the processing of a transmit SONET OC-192 bit serial data stream. It converts the 16-bit parallel data stream into a bit serial data format ranging from 9.953 Gbps to 10.709 Gbps.

A high frequency bit clock is generated from a 622.08 MHz (or equivalent FEC rate) frequency reference by using a frequency synthesizer consisting of an on-chip Phase Lock Loop (PLL) circuit with a divider, a Voltage Controlled Oscillator (VCO), and a loop filter.

Clock Divider and Phase Detector

The clock divider and phase detector, shown in Figure 2, *Functional Block Diagram*, contains monolithic PLL components that generate signals required to drive the loop filter.

The Reference Clock (REFCLK) input must be generated from a differential LVPECL clock oscillator that has a frequency accuracy that meets the value stated in Table 8, *Performance Specifications,* in order for the VCO Clock frequency to meet the accuracy requirements of a SONET system. See Table 1, *Reference Frequency*, for REFCLK frequency requirements.

Timing Generator

The timing generator function, shown in Figure 2, *Functional Block Diagram*, provides two separate functions. It provides a 16-bit parallel rate clock, and a mechanism for aligning the phase between the incoming clock and the clock which loads the parallel-to-serial shift register.

The Parallel Clock (PCLK) output is a 16-bit parallel rate clock. For OC-192, the PCLK frequency is 622.08 MHz. PCLK is intended for use as a 16-bit parallel clock for upstream multiplexing and overhead processing circuits. Using PCLK for upstream circuits will ensure a stable frequency and phase relationship between the data coming into and leaving the S3097 device.

In the parallel-to-serial conversion process, the incoming data is passed from the Parallel Input Clock (PICLK) timing domain to the internally generated byte clock timing domain using an internal First In, First Out register (FIFO).

The timing generator also produces a feedback reference clock to the clock synthesizer. A counter divides the synthesized clock down to the same frequency as the reference clock (REFCLK). The PLL in the clock synthesizer maintains the stability of the synthesized clock by comparing the phase of the feedback clock with that of the reference clock (REFCLK). The modulus of the counter is a function of the reference clock frequency and the operating frequency.

FIFO

A FIFO is added to decouple the internal and external parallel clocks. The internally generated divide-by-16 clock is used to clock out data from the FIFO. PHINIT and LOCKERRB are used to center or reset the FIFO. The PHINIT and LOCKERRB signals will center the FIFO after the third PICLK pulse. (See Figure 8, *Phase Adjust Timing*.) This ensures that PICLK is stable. This scheme allows the user to have an infinite PCLK-to-PICLK delay through the ASIC. Once the FIFO is centered, the PCLK-to-PICLK delay can have a maximum drift as specified in Table 17, *AC Transmitter Timing Characteristics (PICLKP/N = 622.08 MHz to 669.33 MHz).*

The FIFO shown in Figure 2, *Functional Block Diagram,* is comprised of two sets of registers. The 622.08 MHz or 311.04 MHz (or equivalent FEC rate) dual edge PICLK clocks in the data from PINP/N[15:0] bus to the first register of the FIFO. A second register is a parallel loadable shift register which takes its parallel input from the first register.

An internally generated byte clock, which is phase aligned to the transmit serial clock, activates the parallel data transfer between registers. This 16-bit data is presented to the parallel-to-serial converter.

If the 311.04 MHz (or equivalent FEC rate) dual edge PICLK mode is selected. PICLK skew relative to PINP/N[15:0] will be introduced to optimize data and clock setup and hold times. SKEWSEL[1:0] may be used to control the skew which is nominally 915 ps.

FIFO Initialization

The FIFO can be initialized in one of the following three ways:

1. During power up, once the PLL has locked to the reference clock provided on the REFCLK pins, the LOCKERRB will go active and initialize the FIFO.
2. When RSTB goes active, the entire chip is reset. This causes the PLL to go out of lock and thus the LOCKERRB goes inactive. When the PLL reacquires the lock, the LOCKERRB goes active and initializes the FIFO. Note that PCLK does not toggle when RSTB is active.
3. The user can also initialize the FIFO by raising PHINIT.

During normal running operation, the incoming data is passed from the PICLK timing domain to the internally generated divide-by-16 clock timing domain. Although the frequency of PICLK and the internally generated clock is the same, their phase relationship is arbitrary.

To prevent errors caused by short setup or hold times between the two timing domains, the timing generator circuitry monitors the phase relationship between PICLK and the internally generated clock. When a potential setup or hold time violation is detected, Phase Error (PHERR) goes High. If the condition persists, PHERR will remain High. When PHERR condition occurs, PHINIT should be activated to recenter the FIFO (at least 10 ns). This can be done by connecting PHERR to PHINIT. When realignment occurs, four to ten bytes of data will be lost. The user can also take in the PHERR signal, process it and send an output to PHINIT in such a way that idle bytes are lost during the realignment process. PHERR will go inactive when the realignment is complete. (See Figure 8, *Phase Adjust Timing.*)

Parallel-to-Serial Converter

The Parallel-to-Serial converter shown in Figure 2, *Functional Block Diagram*, is comprised of staged registers and 2:1 multiplexers. The 16-bit wide data output from the FIFO is presented to the first register/ 2:1 multiplexer and converted from 16 bits to 8 bits wide. This procedure is repeated to convert to 4, 2, and finally 1 bit wide serial data.

Power Sequencing

In order to avoid latch up, the following power-up sequence is required. Apply GND first, next -5.2 V, then the positive supplies, +2.5 V and +3.3 V. These two positive supplies can be brought up simultaneously or in any order.

Table 4. Input Pin Assignments and Descriptions

Pin Name	Level	I/O	Pin #	Description
PIN0P PIN0N PIN1P PIN1N PIN2P PIN2N PIN3P PIN3N PIN4P PIN4N PIN5P PIN5N PIN6P PIN6N PIN7P PIN7N PIN8P PIN8N PIN9P PIN9N PIN10P PIN10N PIN11P PIN11N PIN12P PIN12N PIN13P PIN13N PIN14P PIN14N PIN15P PIN15N	LVDS	I	N2 N3 P3 P4 N4 N5 P5 P6 N6 N7 P7 P8 N8 N9 P9 P10 M11 M12 N12 N13 N14 M14 L13 K13 K14 J14 H14 G14 G13 F13 F14 E14	**Parallel Data Input.** A 16-bit parallel, 622.08 Mbps data, (or equivalent FEC rate) aligned to the Parallel Input Clock (PICLK). PINP/N[15] is the most significant bit (corresponding to bit 1 of each word, the first bit transmitted). PINP/N[0] is the least significant bit (corresponding to bit 16 of each word, the last bit transmitted). PINP/N[15:0] is sampled on the rising edge of PICLK. Internally biased and terminated with 100 Ω line-to-line.
PICLKP PICLKN	LVDS	I	D14 C14	**Parallel Input Clock.** A 622.08 MHz or 311.04 MHz (or equivalent FEC rate) nominally 50% duty cycle input clock to which PINP/N[15:0] is aligned. PICLK is used to transfer the data on the PIN inputs into a holding register in the parallel-to-serial converter. Internally biased and terminated with 100 Ω line-to-line.
TESTB	LVCMOS	I	C6	**Test Mode Enable.** Active Low. Set Low to provide access to the PLL during factory production tests. Connect to $V_{CC\_2.5\ V}$ through a 10 kΩ resistor for normal system operation.
REFCLKP REFCLKN	Diff. LVPECL	I	B1 C1	**Reference Clock Input.** Used as the reference for the internal bit clock frequency synthesizer. Internally biased and terminated 100 Ω line-to-line.
RSTB	LVCMOS	I	A7	**Master Reset.** Active Low. Reset input for the device. For correct reset, this input must be asserted Low for 100 ns. During reset, PCLK does not toggle. Connect to $V_{CC\_2.5\ V}$ through a 10 kΩ resistor if not used.
CAP1 CAP2	Analog	I	B4 C4	**Loop Filter.** Connections for external loop filter capacitor and resistors. (See Figure 14, *External Loop Filter* and Table 19, *External Loop Filter Components*.)

Table 4. Input Pin Assignments and Descriptions (Continued)

Pin Name	Level	I/O	Pin #	Description
PHINIT	LVCMOS	I	C13	**Phase Initialization.** Active High. Asynchronous input that initializes the phase adjust circuit. (See Figure 8, *Phase Adjust Timing*.)
REFTESTB	LVCMOS	I	M2	**Reference Test** Active Low. Set Low to provide access to the PLL during factory production tests. Connect to $V_{CC\_2.5\,V}$ through a 10 kΩ resistor for normal system operation.
CLKSEL	LVCMOS	I	A6	**Clock Select.** Used to select between the 622.08 or 311.04 MHz (or equivalent FEC rate) clock on the PICLKP/N input. See Table 2, *Clock Select*.
SKEWSEL0 SKEWSEL1	LVCMOS	I	D13 J13	**Skew Select.** Used in 311.04 MHz (or equivalent FEC rate) PICLK mode to optimize PICLK and PINP/N[15:0] setup and hold times. See Table 3, *Skew Select.*

Table 5. Output Pin Assignments and Descriptions

Pin Name	Level	I/O	Pin #	Description
TSDP TSDN	Differential CML	O	G1 J1	**Transmit Serial Data.** Serial data stream signals, normally connected to an optical transmitter module.
PCLKP PCLKN	LVDS	O	B11 A11	**Parallel Clock.** A 622.08 MHz (or equivalent FEC rate) clock output. It is normally used to coordinate transfers between upstream logic and the S3097 device. Internally terminated with 330 Ω to GND
155MCKP 155MCKN	LVDS	O	B10 B9	**155.52 MHz Clock Output.** A 155.52 MHz (or equivalent FEC rate) clock output from the clock synthesizer. This output should be connected to the reference clock input of the external clock and data recovery function (such as the S3098). Internally terminated with 330 Ω to GND
77MCKP 77MCKN	LVDS	O	A10 A9	**77.76 MHz Clock Output.** For test purposes only.
LOCKERRB	LVCMOS	O	C12	**Lock Error/Phase Error.** Active Low. Goes inactive after the PLL has locked to the clock provided on the REFCLK pins. LOCKERRB goes active for at least 100 ns when PHERR goes active. LOCKERRB stays active as long as PHERR is active. LOCKERRB is an asynchronous output.
PHERR	LVCMOS	O	A12	**Phase Error.** Active High. Pulses High at start of each PCLK cycle for which there is a potential set-up/hold timing violation between the internal byte clock and PICLK timing domains.

Table 6. Common Pin Assignments and Descriptions

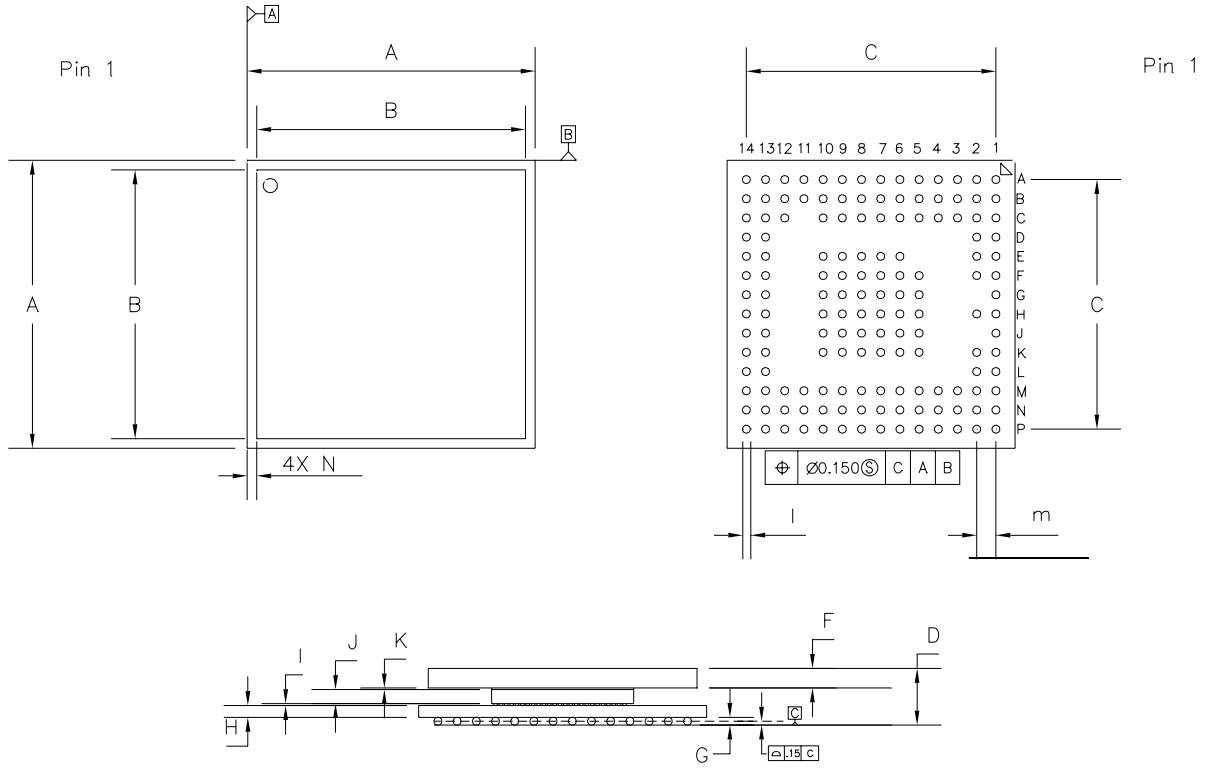
Pin Name	Level	I/O	Pin #	Description
CORE VCC	+2.5 V	PWR	C8, M6	Digital $V_{CC\_2.5V}$ +2.5 V ± 5%
LVDSVCC	+2.5 V	PWR	C9, H13, M3, M9, M13	LVDS $V_{CC\_2.5V}$ +2.5 V ± 5%
LVCMOSVCC	+2.5 V	PWR	C7	LVCMOS $V_{CC\_2.5V}$ +2.5 V ± 5%
ANALOG AVCC	+3.3 V	PWR	A3, A5	Analog $V_{CC\_3.3V}$ +3.3 V ± 5%
DIGITAL VCC	+3.3 V	PWR	B8, M5	Digital $V_{CC\_3.3V}$ +3.3 V ± 5%
CMLVEE	-5.2 V	PWR	D1, E2, L2	CML V_{EE} -5.2 V ± 5%
SUBVEE	-5.2 V	PWR	B13, M8, N11	Substrate V_{EE} -5.2 V ± 5%
GND	0 V	GND	A1, A2, A4, A8, A13, A14, B2, B3, B5, B6, B7, B12, B14, C2, C3, C5, C10, D2, E1, E13, F1, F2, H1, H2, K1, K2, L1, L14, M1, M4, M7, M10, N1, N10, P1, P2, P11, P12, P13, P14	Analog/Digital Ground
THERMAL GND	0 V	GND	E6, E7, E8, E9, E10, F5, F6, F7, F8, F9, F10, G5, G6, G7, G8, G9, G10, H5, H6, H7, H8, H9, H10, J5, J6, J7, J8, J9, J10, K5, K6, K7, K8, K9, K10	Thermal Ground

Note: All digital, analog, and thermal grounds are connected together on the package.

Figure 3. S3097 Pinout (Top View)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	ANALOG GND	ANALOG GND	ANALOG AVCC +3.3V (FILTER)	ANALOG GND	ANALOG AVCC +3.3V (VCO)	CLKSEL	RSTB	DIGITAL GND	77MCKN	77MCKP	PCLKN	PHERR	DIGITAL GND	DIGITAL GND
B	REFCLKP	ANALOG GND	ANALOG GND	CAP1	ANALOG GND	ANALOG GND	DIGITAL GND	DIGITAL VCC +3.3V (PD)	155MCKN	155MCKP	PCLKP	DIGITAL GND	SUB VEE -5.2V	DIGITAL GND
C	REFCLKN	ANALOG GND	ANALOG GND	CAP2	ANALOG GND	TESTB	LVCMOS VCC +2.5V	CORE VCC +2.5V	LVDS VCC +2.5V	DIGITAL GND		LOCK ERRB	PHINIT	PICLKN
D	CML VEE -5.2V	ANALOG GND											SKEW SEL0	PICLKP
E	ANALOG GND	CML VEE -5.2V				THERMAL GND	THERMAL GND	THERMAL GND	THERMAL GND	THERMAL GND			DIGITAL GND	PIN15N
F	ANALOG GND	ANALOG GND			THERMAL GND	THERMAL GND	THERMAL GND	THERMAL GND	THERMAL GND	THERMAL GND			PIN14N	PIN15P
G	TSDP				THERMAL GND	THERMAL GND	THERMAL GND	THERMAL GND	THERMAL GND	THERMAL GND			PIN14P	PIN13N
H	ANALOG GND	ANALOG GND			THERMAL GND	THERMAL GND	THERMAL GND	THERMAL GND	THERMAL GND	THERMAL GND			LVDS VCC +2.5V	PIN13P
J	TSDN				THERMAL GND	THERMAL GND	THERMAL GND	THERMAL GND	THERMAL GND	THERMAL GND			SKEW SEL1	PIN12N
K	ANALOG GND	ANALOG GND			THERMAL GND	THERMAL GND	THERMAL GND	THERMAL GND	THERMAL GND	THERMAL GND			PIN11N	PIN12P
L	ANALOG GND	CML VEE -5.2V				**PACKAGE TOP VIEW**							PIN11P	DIGITAL GND
M	ANALOG GND	REFTESTB	LVDS VCC +2.5V	DIGITAL GND	DIGITAL VCC +3.3V (MUX)	CORE VCC +2.5V	DIGITAL GND	SUB VEE -5.2V	LVDS VCC +2.5V	DIGITAL GND	PIN8P	PIN8N	LVDS VCC +2.5V	PIN10N
N	DIGITAL GND	PIN0P	PIN0N	PIN2P	PIN2N	PIN4P	PIN4N	PIN6P	PIN6N	DIGITAL GND	SUB VEE -5.2V	PIN9P	PIN9N	PIN10P
P	DIGITAL GND	DIGITAL GND	PIN1P	PIN1N	PIN3P	PIN3N	PIN5P	PIN5N	PIN7P	PIN7N	DIGITAL GND	DIGITAL GND	DIGITAL GND	DIGITAL GND

Figure 4. Compact 15 mm x 15 mm 148-pin CBGA Package



DIMENSIONS (millimeters)

UNIT	A	B	C	D	F	G	H	I	J	K	l	m	N
MIN	14.80	14.40	12.90	2.58	0.965	0.425 REF.	0.51	0.100 REF.	.730	0.025	0.33	1.00 REF.	0.05
NOM	15.00	14.50	13.00	2.97	1.016		0.61		.736	0.053	0.40		0.25
MAX	15.20	14.60	13.10	3.10	1.067		0.71		.743	0.080	0.47		0.45

Table 7. Package Thermals[1]

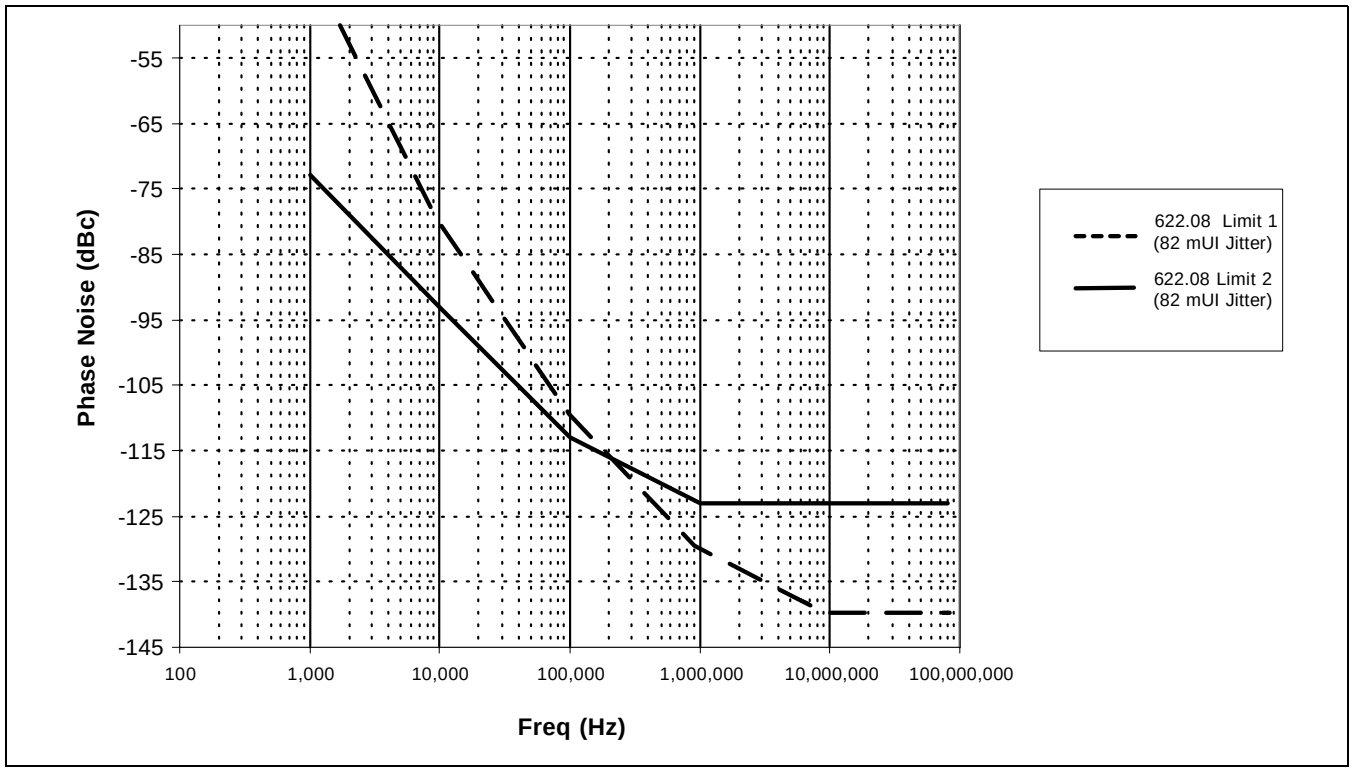
Max Package Power (85°C Ambient)	**Θja**	**Θjc**
1.95 W	20.5°C/Watt	3.0°C/Watt

1. The S3097 requires thermal management at the higher end of the ambient range (> 75°C ambient). This is assuming a junction temperature of 125°C.

Table 8. Performance Specifications

Parameter	Min.	Typ	Max	Units	Condition
VCO Center Frequency	9.953		10.709	GHz	
Phase noise requirements for 622.08 MHz (or equivalent FEC rate) REFCLK.		-112		dBc/Hz	@ 10 kHz offset from carrier (See Figure 5, *622.08 MHz REFCLK Phase Noise versus Typical Jitter Generation.*
J_{gen} Jitter Generation (TSDP/N)			0.082	UI $_{(p-p)}$	Peak-to-peak, in lock, for 50 kHz to 80 MHz B.W. with 622.08 MHz REFCLK phase noise shown in Figure 5, *622.08 MHz REFCLK Phase Noise versus Typical Jitter Generation*. (BER = 10E-12)
TSDP/N Output Return Loss (S_{22})			-10	dB	DC - 10 GHz
Reference Clock Frequency Tolerance	-100		+100	ppm	± 20 ppm is required to meet SONET output frequency specification.
Reference Clock Input Duty Cycle	45		55	%	
Reference Clock Rise & Fall Times	0.1		0.3	ns	20% to 80% of amplitude.
Acquisition Lock Time (phase lock)		16	25	µs	After the release of RSTB with device already powered up and with a valid REFCLK. Guaranteed, but not tested.

Figure 5. 622.08 MHz REFCLK Phase Noise versus Typical Jitter Generation



Note: Using an oscillator with either phase noise spectrum shown will yield similar jitter generation as the integrated phase noise under each mask is similar.

Table 9. Absolute Maximum Ratings

The following are the absolute maximum stress ratings for the S3097 device. Stresses beyond those listed may cause permanent damage to the device. Absolute maximum ratings are stress ratings only, and operation of the device at the maximums stated or any other conditions beyond those indicated in the "Recommended Operating Conditions" of the document are not inferred. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameter	Min.	Typ	Max	Units
Storage Temperature	-55		150	°C
$V_{CC\_2.5V}$ +2.5 V Supply	-0.5		2.7	V
$V_{CC\_3.3V}$ +3.3 V Supply	-0.5		3.6	V
V_{EE} -5.2 V Supply	-7.0		-0.5	V
LVCMOS Input Voltage	-0.5		$V_{CC\_2.5\ V}$ +0.5	V
LVPECL Input Voltage	-0.5		$V_{CC\_3.3\ V}$ +0.5	V
LVDS Input Voltage	-0.5		$V_{CC\_2.5\ V}$ +0.5	V
CML Output Current Per Pin			13	mA
LVDS Output Current Per Pin			5	mA
LVCMOS Output Current per pin (source/sink)			30/1000	uA
LVCMOS Input Current per pin (source/sink)			200/65	uA
LVDS Input Current Per Pin			7	mA
LVPECL Input Current Per Pin			13	mA

Electrostatic Discharge (ESD) Ratings

The S3097 is rated to the following ESD voltages based on the human body model per JESD22-A114-B specification:

1. All pins are rated at 100 V.

Table 10. Recommended Operating Conditions

Parameter	Min.	Typ	Max	Units	Conditions
Ambient Temperature Under Bias	0		+85	°C	
Junction Temperature Under Bias	25		125	°C	
Voltage on $V_{CC\_2.5\ V}$ with Respect to GND	2.375	2.5	2.625	V	
Voltage on $V_{CC\_3.3\ V}$ with Respect to GND	3.135	3.3	3.465	V	
Voltage on V_{EE} with Respect to GND	-4.94	-5.2	-5.46	V	
$I_{CC\_2.5V}$ Supply Current			370	mA	Outputs terminated.
I_{EE_CML} Supply Current			125	mA	Outputs terminated.
$I_{CC\_3.3V\_AVCC/VCC}$ Supply Current			208	mA	Outputs terminated. 30% is AVCC 70% is VCC
Power Dissipation			2.37	W	Outputs terminated.
Power Supply Noise Rejection		35		mVpp	6 kHz to 2 MHz bandwidth

Table 11. LVCMOS Input DC Characteristics

Parameter	Description	Min.	Typ	Max	Units	Conditions
V_{IH}	Input High Voltage	1.7		$V_{CC\_2.5\ V}$	V	Over process, voltage and temperature range.
V_{IL}	Input Low Voltage	0		0.7	V	Over process, voltage and temperature range.
I_{IH}	Input High Current			65	µA	V_{IH} min
I_{IL}	Input Low Current			200	µA	V_{IL} min

Table 12. LVCMOS Output DC Characteristics

Parameter	Description	Min.	Typ	Max	Units	Conditions
V_{OH}	Output High Voltage	2.0		$V_{CC\_2.5\ V}$	V	Over process, voltage and temperature range. I_{OH} = 30 uA
V_{OL}	Output Low Voltage	0		0.4	V	Over process, voltage and temperature range. I_{OL} = 1 mA

Table 13. Differential CML Output DC Characteristics

Parameter	Description	Min.	Typ	Max	Units	Conditions
V_{OH}	Output High Voltage	GND -0.55		GND -0.25	V	Over process, voltage and temperature range. Output loading is 100 Ω line-to-line.
V_{OL}	Output Low Voltage	GND -1.25		GND -0.80	V	Over process, voltage and temperature range. Output loading is 100 Ω line-to-line.
V_{ODIFF}	Serial Output Differential Voltage Swing	1000		1500	mV	Over process, voltage and temperature range. Output loading is 100 Ω line-to-line. See Figure 9, *Differential Voltage Measurement.*
$V_{OSINGLE}$	Serial Output Single-ended Voltage Swing	500		750	mV	Over process, voltage and temperature range. Output loading is 100 Ω line-to-line. See Figure 9, *Differential Voltage Measurement.*
R_{ODIFF}	Differential Output Impedance	80	100	120	Ω	Over process, voltage and temperature range.

Table 14. Internally Biased LVDS Input DC Characteristics

Parameter	Description	Min.	Typ	Max	Units	Conditons
V_{IH}	Input High Voltage	1.16		1.9	V	Over process, voltage and temperature range.
V_{IL}	Input Low Voltage	0.6		1.5	V	Over process, voltage and temperature range.
V_{IDIFF}	Input Voltage Differential	200		2400	mV	Over process, voltage and temperature range. See Figure 9, *Differential Voltage Measurement.*
$V_{ISINGLE}$	Input Single-ended Voltage	100		1200	mV	Over process, voltage and temperature range. See Figure 9, *Differential Voltage Measurement.*
V_{ICM}	Input Common Mode Voltage	0.9		1.7	V	Over process, voltage and temperature range.
R_{IDIFF}	Differential Input Impedance	80	100	120	Ω	Over process, voltage and temperature range.

Table 15. LVDS Output DC Characteristics

Parameter	Description	Min.	Typ	Max	Units	Conditons
V_{OH}	Output High Voltage	1.25		1.8	V	Output loading is 100 Ω line-to-line. Over process, voltage and temperature range.
V_{OL}	Output Low Voltage	0.85		1.45	V	Output loading is 100 Ω line-to-line. Over process, voltage and temperature range.
V_{ODIFF}	Output Differential Voltage	500	740	1100	mV	Output loading is 100 Ω line-to-line. Over process, voltage and temperature range. See Figure 9, *Differential Voltage Measurement.*
$V_{OSINGLE}$	Output Single-ended Voltage	250	370	550	mV	Output loading is 100 Ω line-to-line. Over process, voltage and temperature range. See Figure 9, *Differential Voltage Measurement.*
R_{ODIFF}	Differential Output Impedance			140	Ω	Over process, voltage and temperature range. Guaranteed by design.

Table 16. LVPECL Input DC Characteristics (REFCLKP/N)

Parameter	Description	Min.	Typ	Max	Units	Conditions
V_{IH}	Input High Voltage	$V_{CC\_3.3\ V}$ -1.2		$V_{CC\_3.3\ V}$ -0.5	V	Over process, voltage and temperature range.
V_{IL}	Input Low Voltage	$V_{CC\_3.3\ V}$ -2.00		$V_{CC\_3.3\ V}$ -1.4	V	Over process, voltage and temperature range.
V_{IDIFF}	Differential Input Voltage Swing	300		1200	mV	Over process, voltage and temperature range. See Figure 9, *Differential Voltage Measurement.*
$V_{ISINGLE}$	Single-ended Input Voltage Swing	150		600	mV	Over process, voltage and temperature range. See Figure 9, *Differential Voltage Measurement.*
V_{ICM}	Input Common Mode Voltage	$V_{CC\_3.3\ V}$ -1.6		$V_{CC\_3.3\ V}$ -0.95	V	Over process, voltage and temperature range.
R_{IDIFF}	Differential Input Impedance	80	100	120	Ω	Over process, voltage and temperature range.

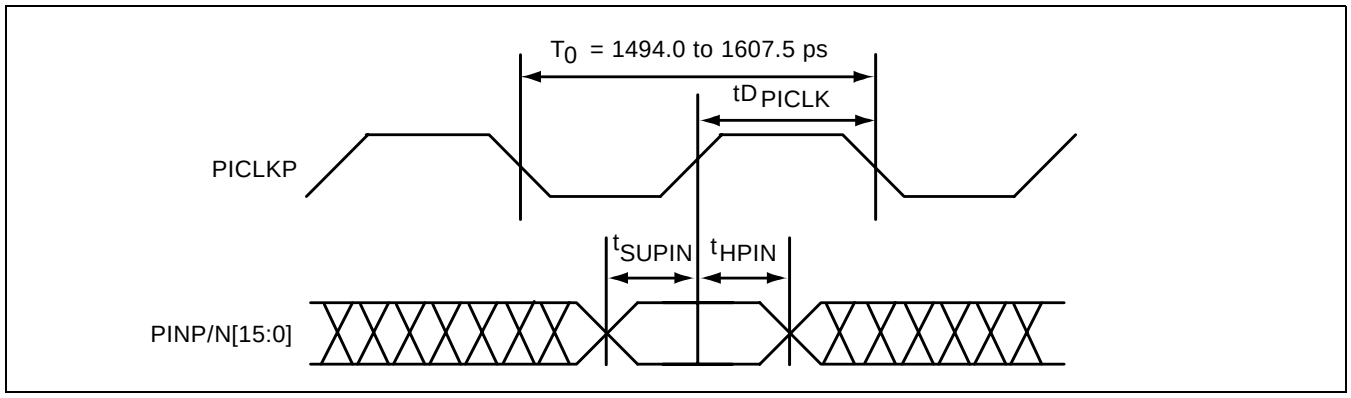
Table 17. AC Transmitter Timing Characteristics (PICLKP/N = 622.08 MHz to 669.33 MHz)

Parameter	Description	Min.	Typ	Max	Units	Conditions
Duty Cycle	PICLK Duty Cycle = tD_{PICLK} / T_0 See Figure 6, *AC Input Timing (PICLKP/N = 622.08 MHz to 669.33 MHz.*)	40		60	%	Over process, voltage and temperature range.
	PCLKP/N Duty Cycle	45		55	%	Over process, voltage and temperature range.
	155MCKP/N Duty Cycle	45		55	%	Over process, voltage and temperature range.
t_{SUPIN}	PINP/N[15:0] Set-up Time with respect to the rising edge of 622.08 MHz PICLKP	185			ps	Over process, voltage and temperature range.
t_{HPIN}	PINP/N[15:0] Hold Time with respect to the rising edge of 622.08 MHz PICLKP	185			ps	Over process, voltage and temperature range.
t_r/t_f	CML Output Rise and Fall Time (20% - 80%)			30	ps	Over process, voltage and temperature range.
	LVPECL Input Rise and Fall Time (20% - 80%)	100		300	ps	Over process, voltage and temperature range.
	LVDS Output Rise and Fall Time (20% - 80%)	80		250	ps	Over process, voltage and temperature range.
	LVDS Input Rise and Fall Time (20% - 80%)	80		300	ps	Over process, voltage and temperature range.
	LVCMOS Output Rise and Fall Time (20% - 80%) 5 pF load 15 pF load			 50 100	ns	Over process, voltage and temperature range. Guaranteed by design.
t_{PW}	PHINIT Minimum Pulse Width (See Figure 8, *Phase Adjust Timing*.)	10			ns	Over process, voltage and temperature range.

Table 17. AC Transmitter Timing Characteristics (PICLKP/N = 622.08 MHz to 669.33 MHz) (Continued)

Parameter	Description	Min.	Typ	Max	Units	Conditions
t_{PW}	PHERR Minimum Pulse Width	4 to 10 byte clocks				Byte clock = 622.08 MHz (or equivalent FEC rate). Guaranteed by design.
t_{PW}	RSTB Minimum Pulse Width	100			ns	Guaranteed by design.
t_{DRIFT}	PCLK to PICLK drift after FIFO is centered			2	ns	Over process, voltage and temperature range.

Figure 6. AC Input Timing (PICLKP/N = 622.08 MHz to 669.33 MHz)[1,2]



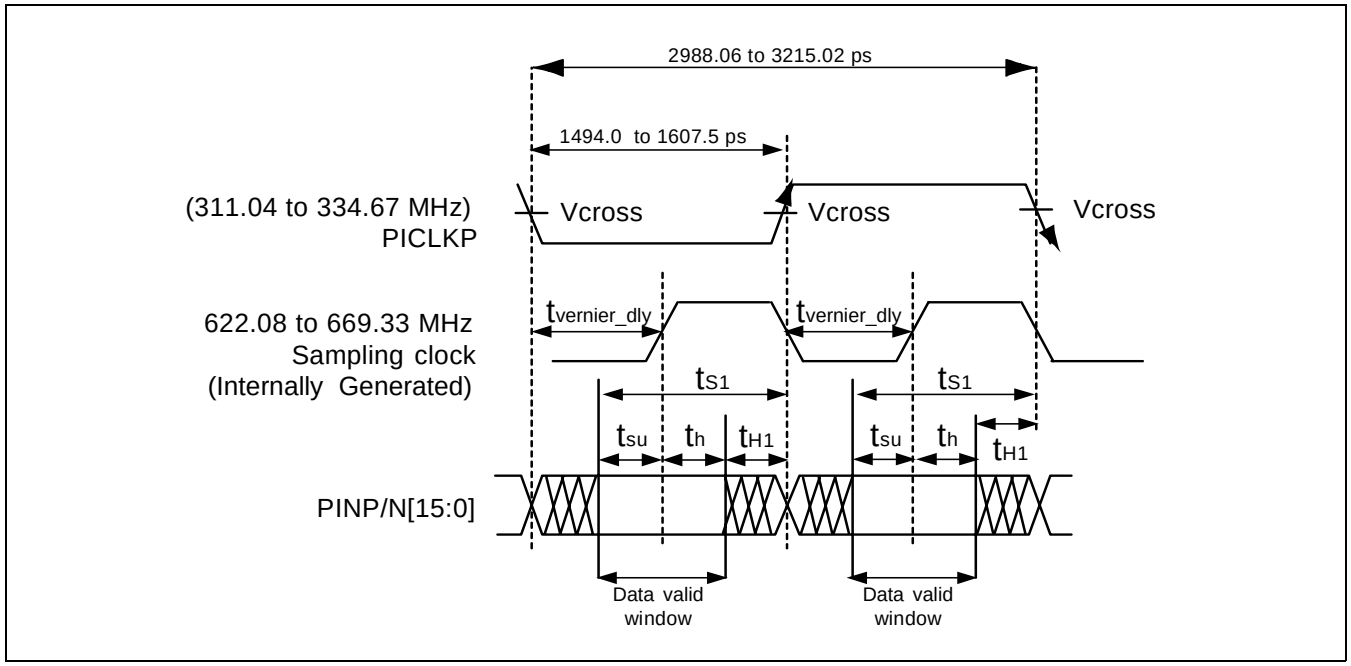
1. When a setup time is specified on LVDS signals between an input and a clock, the setup time in picoseconds, is from the 50% point of the input to the 50% point of the clock.
2. When a hold time is specified on LVDS signals between an input and a clock, the hold time in picoseconds, is from the 50% point of the clock to the 50% point of the input.

Table 18. AC Transmitter Timing Characteristics (PICLKP/N = 311.04 MHz to 334.67 MHz)[1]

Parameter	Description	Min.	Typ	Max	Units
Duty Cycle	PICLK Duty Cycle = tD_{PICLK} / T_0 (See Figure 7, *AC Input Timing (PICLKP/N = 311.04 MHz to 334.67 MHz.*))	48		52	%
t_{su}	PINP/N[15:0] Set-up Time with respect to the rising edge of internally generated sampling clock. Guaranteed by design.	200			ps
t_h	PINP/N[15:0] Hold Time with respect to the rising edge of internally generated sampling clock. Guaranteed by design.	200			ps
$t_{vernier\_dly}$	User selectable delay time from the rising or falling edge of the PICLK to the rising (sampling) edge of the 622.08 to 669.33 MHz sampling clock. (See Table 3, *Skew Select*.) Guaranteed by design.	715		1015	ps
t_{S1}	PINP/N Set-up Time with respect to next rising edge of PICLKP.	985			ps
t_{H1}	PINP/N Hold Time with respect to next rising edge of PICLKP.			615	ps

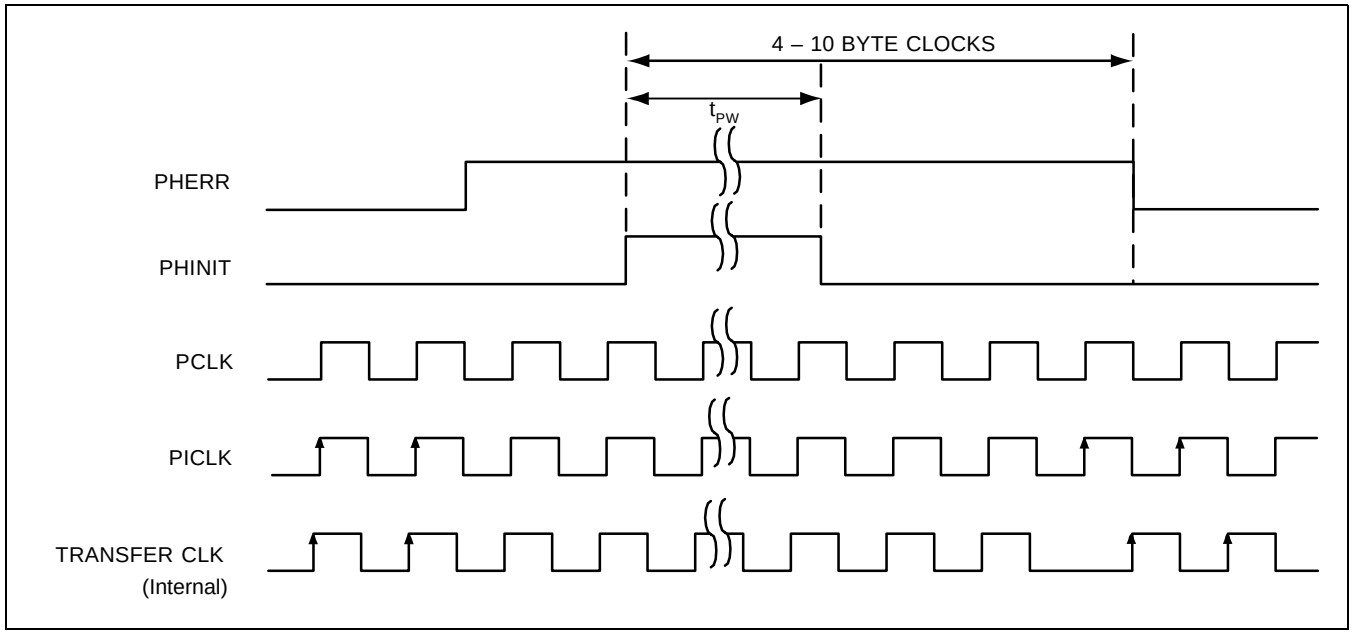
1. SKEWSEL[1:0] = 00 setting.

Figure 7. AC Input Timing (PICLKP/N = 311.04 MHz to 334.67 MHz)



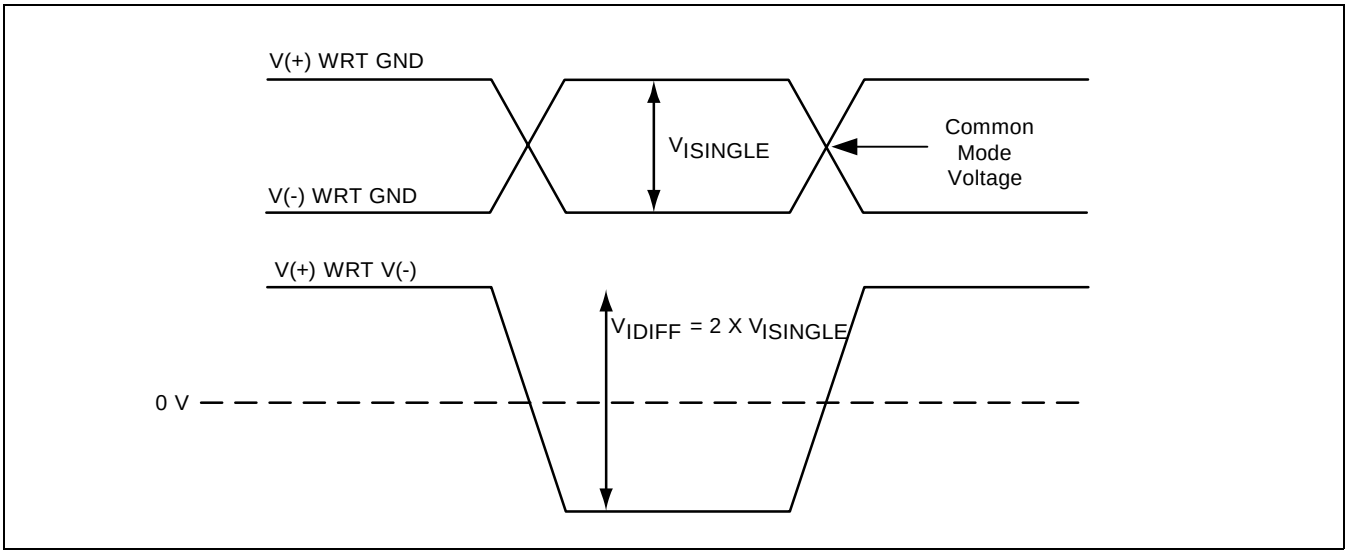
Note: The rising edge of the 622.08 to 669.33 MHz internally generated sampling clock will move in time based upon the user selectable vernier delay. This delay is set via SKEWSEL[1:0]. The SKEWSWEL[1:0] selection will determine where the rising edge of the sampling clock will fall within the data valid window. Setting SKEWSEL[1:0] to the 715 ps mode will move the internally generated sampling clock to the left of the centered data window. Setting SKEWSEL[1:0] to the 1015 ps mode will move the internally generated sampling clock edge to the right of the centered data window. The sampling clock rising edge is generated from the rising and falling edges of the PICLK.

Figure 8. Phase Adjust Timing



Note: The byte clock = 622.08 MHz (or equivalent FEC rate).

Figure 9. Differential Voltage Measurement



Note: WRT = with respect to.

Table 19. External Loop Filter Components (See Figure 14 External Loop Filter)

Symbol	Description	Value	Unit
R_1, R_2	Resistor, Surface Mount, 0402	120	Ω
C_1	Capacitor, Surface Mount, Non-polarized, 0603 or larger	1	µF

Figure 10. S3097 CML Output to -5.2 V ECL Input DC Coupled Termination

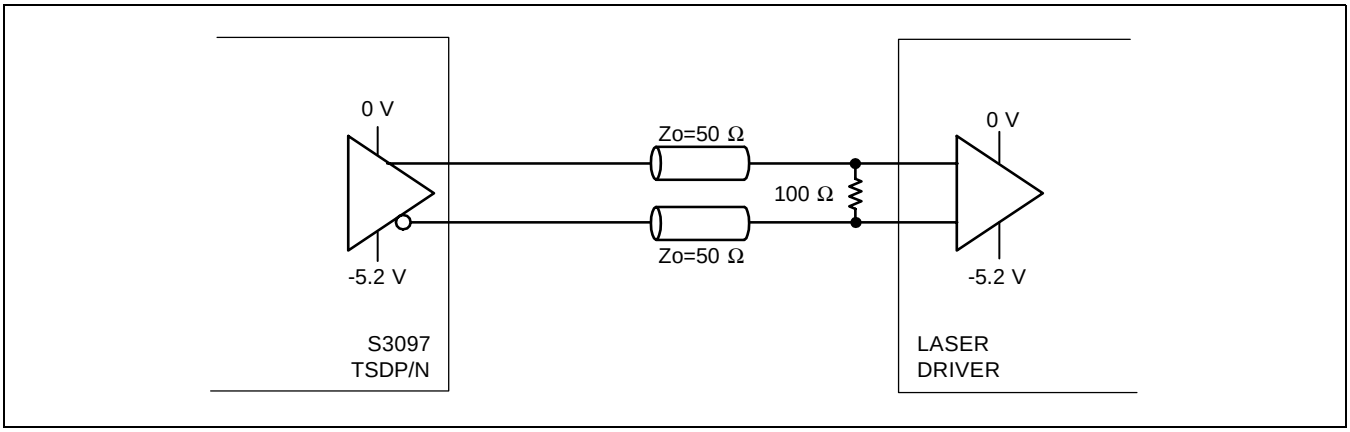


Figure 11. S3097 LVDS Output to LVDS Input

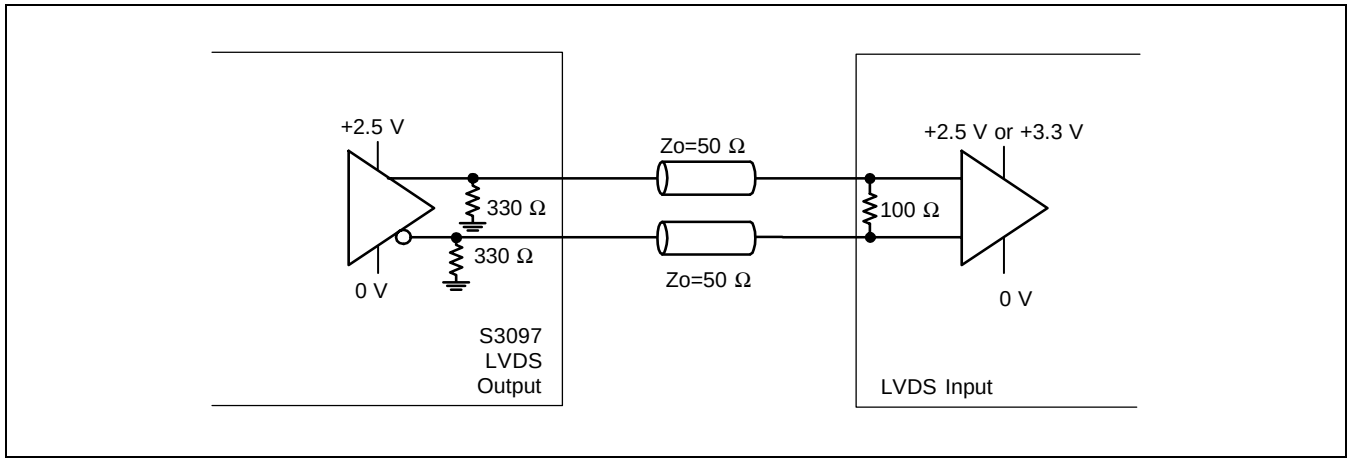


Figure 12. LVDS Output to S3097 LVDS Input

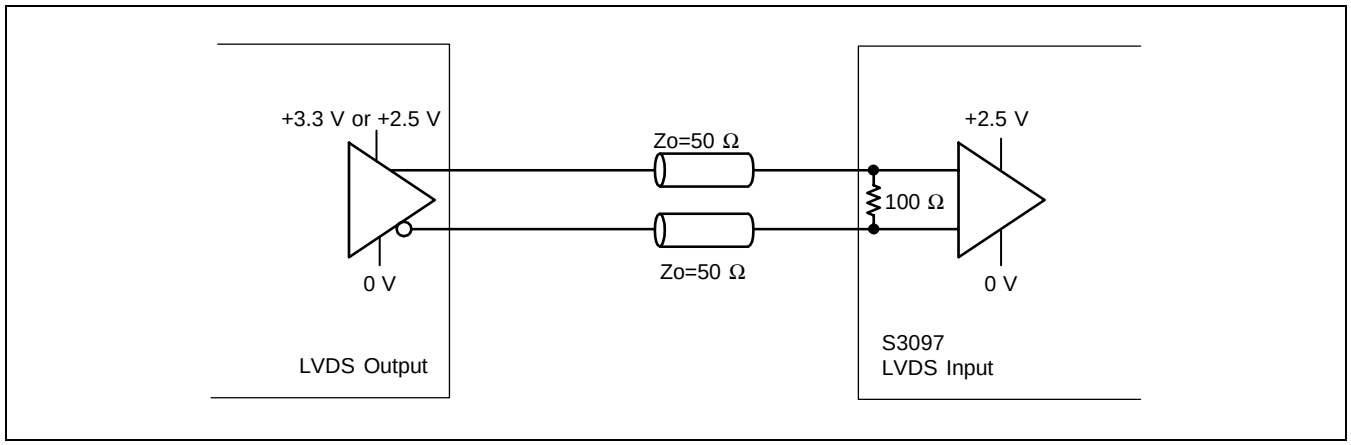


Figure 13. +3.3 V Differential LVPECL Driver to S3097 LVPECL Reference Clock Input, AC Coupled Termination

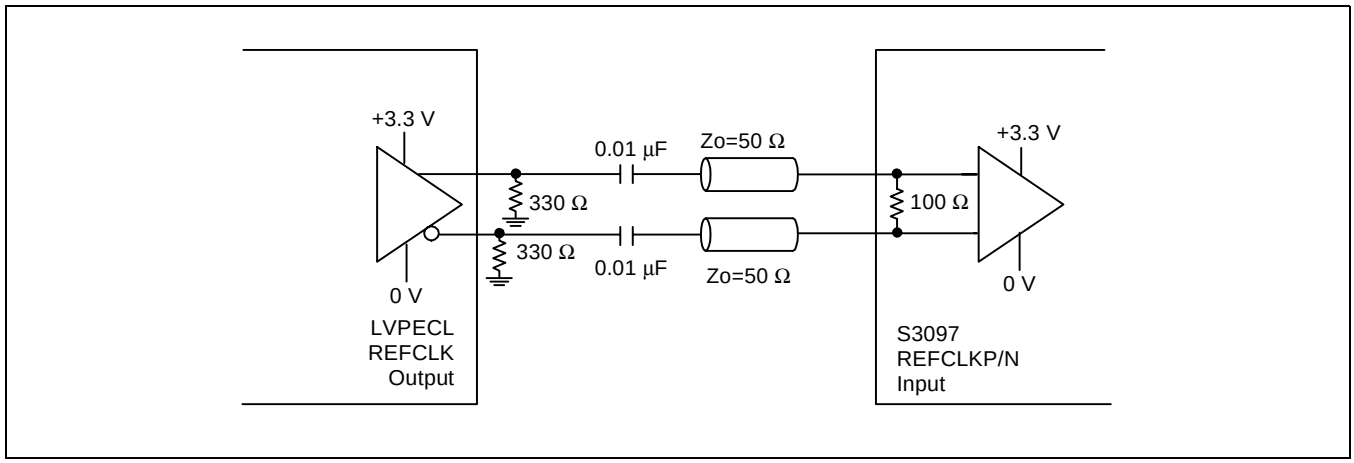
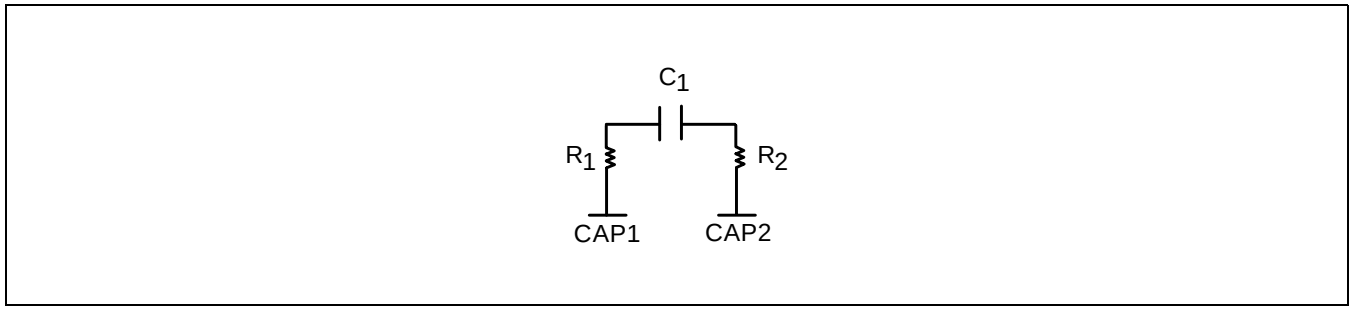


Figure 14. External Loop Filter (See Table 19, External Loop Filter Components)



Ordering Information

Prefix	Device	Package	Revision
S – Integated Circuit	3097	CB – 148 CBGA	12
X	XXXX	XX	XX
Prefix	Device	Package	Revision

Applied Micro Circuits Corporation
6290 Sequence Dr., San Diego, CA 92121
Phone: (858) 450-9333 — (800) 755-2622 — Fax: (858) 450-9885
http://www.amcc.com

D37/R830