HARRIS SEMICONDUCTOR

HM-92570

256K Buffered Synchronous CMOS RAM Module

January 1992

Features

- Low Standby Current.....600µA/3.5mA
- Fast Access Time.....250ns
- Data Retention.....2.0V
- Three-State Outputs
- Organizable As 32K x 8 or 16K x 16 Array
- Buffered Address And Control Lines
- On Chip Address Registers
- 48 Pin DIP Pinout - 2.66" x 1.30" x 0.29"
- Operating Temperature Range.....-55°C to +125°C

Ordering Information

PACKAGE	TEMP. RANGE	250ns
Module	-55°C to +125°C	HM5-92570-8

Description

The HM-92570 is a fully buffered 256K bit CMOS RAM Module consisting of sixteen HM-6516 2K x 8 CMOS RAMs, two 82C82 CMOS octal latching bus drivers, and two HCT-138 CMOS 3:8 decoders in leadless chip carriers mounted on a multilayer ceramic substrate. The HM-92570 RAM Module is organized as two 16K x 8 CMOS RAM arrays sharing a common address bus. Separate data input/output buses allow the user to format the HM-92570 as either a 16K x 16 or 32K x 8 array.

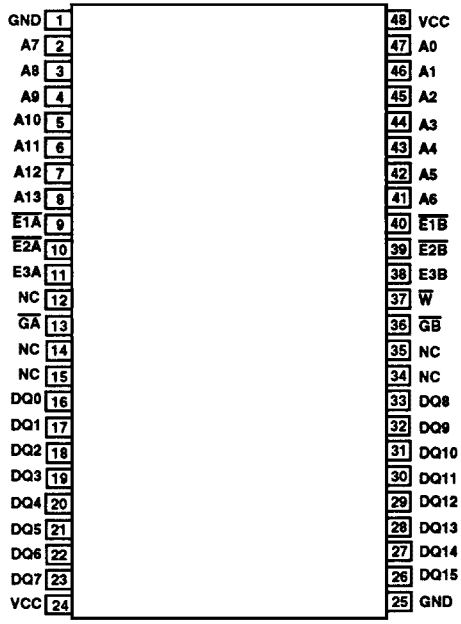
On-board buffers and decoders reduce external package count requirements. Write enable, output enable and chip enable control signals are buffered along with address inputs. Ceramic capacitors sealed in leadless carriers are included on the substrate to reduce power supply noise and to reduce the need for external decoupling.

The synchronous design of the HM-92570 provides low operating power along with address latches for ease of interface to multiplexed address/data bus microprocessors.

The HM-92570 is physically constructed as an extra wide 48 pin dual-in-line package with standard 0.1" centers between pins. This package technique combines the high packing density of CMOS and leadless chip carriers with the ease of use of DIP packaging.

Pinout

48 LEAD MODULE
TOP VIEW



PIN NAMES

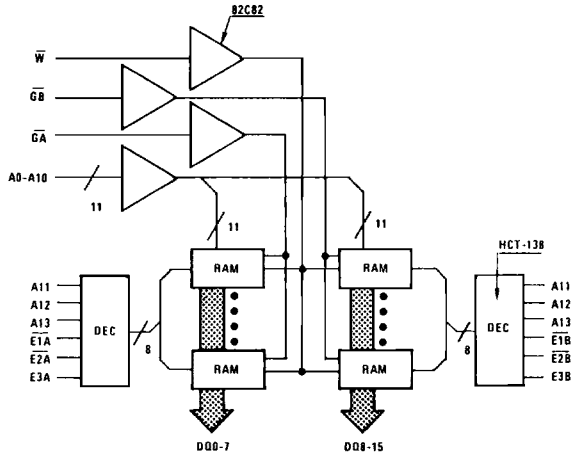
PIN	DESCRIPTION
A	Address Input
DQ	Data Input/Output
GX	Output Enable
EXX	Chip Enable
$\overline{W}$	Write Enable
NC	No Connection

6 CMOS MEMORY

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3010

Functional Diagram



Organizational Guide

FOR 32K X 8 CONFIGURATION

Connect: Pin 16 (DQ0) to Pin 33 (DQ8)
Pin 17 (DQ1) to Pin 32 (DQ9)
Pin 18 (DQ2) to Pin 31 (DQ10)
Pin 19 (DQ3) to Pin 30 (DQ11)
Pin 20 (DQ4) to Pin 29 (DQ12)
Pin 21 (DQ5) to Pin 28 (DQ13)
Pin 22 (DQ6) to Pin 27 (DQ14)
Pin 23 (DQ7) to Pin 26 (DQ15)

FOR 16K X 16 CONFIGURATION

Connect: Pin 9 ($\overline{E1A}$) to Pin 40 ($\overline{E1B}$)
Pin 10 ($\overline{E2A}$) to Pin 39 ($\overline{E2B}$)
Pin 11 ($\overline{E3A}$) to Pin 38 ($\overline{E3B}$)
Pin 13 ($\overline{GA}$) to Pin 36 ($\overline{GB}$)

Concerns for Proper Operation of Chip Enables:

The transition between blocks of RAM requires a change in the chip enable being used. When operating in the 16K x 16 mode, use the chip enables as if there were only three, E1 thru E3. In the 32K x 8 mode, all chip enables must be treated separately. Transitions between chip enables must be treated with the same timing constraints that apply to any one chip enable. All chip enables must be high at least one chip enable high time (TEHEL) before any chip enable can fall. As the HM-92570 is a synchronous memory, every address transition must be accompanied by a chip enable transition (see timing diagrams). More than one chip enable low simultaneously, for devices whose outputs are tied common either internally or externally, is an illegal input condition and must be avoided. To properly decode the chip enables, addresses A11, A12, and A13 must be valid for the duration of TAVAV.

Printed Circuit Board Mounting:

The leadless chip carrier packages used in the HM-92570 have conductive lids. These lids are electrically connected to GND. The designer should be aware of the possibility that the carriers on the bottom side could short conductors below if pressed completely down against the surface of the circuit board. The pins on the package are designed with a standoff feature to help prevent the leadless carriers from touching the circuit board surface.

Absolute Maximum Ratings

Supply Voltage ..... +7.0V
Input, Output or I/O Voltage ..... GND-0.3V to VCC+0.3V
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... +175°C
Lead Temperature (Soldering 10s) ..... +300°C
Gate Count ..... 417200 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range ..... +4.5V to +5.5V
Operating Temperature Range ..... -55°C to +125°C

DC Electrical Specifications VCC = 5V ± 10%; T_A = -55°C to +125°C (HM-92570-8)

SYMBOL	PARAMETER	MIN	MAX	UNITS	(NOTE 1) TEST CONDITIONS
ICCSB	Standby Supply Current	-	600	µA	IO = 0mA, VI = VCC or GND
ICCOP	Operating Supply Current (16K x 16) (Note 3)	-	30	mA	$\overline{E}$ = 1MHz, IO = 0mA, VI = VCC or GND, $\overline{G}$ = VCC
ICCOP	Operating Supply Current (32K x 8) (Note 3)	-	15	mA	$\overline{E}$ = 1MHz, IO = 0mA, VI = VCC or GND, $\overline{G}$ = VCC
ICCDR	Data Retention Supply Current	-	450	µA	VCC = 2.0V, IO = 0mA, VI = VCC or GND, $\overline{E}$ = VCC
VCCDR	Data Retention Supply Voltage	2.0	-	V	
II	Input Leakage Current	-1.0	+1.0	µA	VI = VCC or GND
IIOZ	Input/Output Leakage Current	-5.0	+5.0	µA	VO = VCC or GND
VIL	Input Low Voltage	0	0.8	V	
VIH	Input High Voltage	3.5	VCC	V	
VOL	Output Low Voltage	-	0.4	V	IO = 3.2mA
VOH1	Output High Voltage	2.4	-	V	IO = -0.4mA
VOH2	Output High Voltage (Note 2)	VCC-0.4	-	V	IO = -100µA

Capacitance T_A = +25°C

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
CIA	Address Input Capacitance (Note 2)	-	50	pF	VI = VCC or GND, f = 1MHz
CIE1	Decoder Enable Input Capacitance (16K x 16) (Note 2)	-	50	pF	VI = VCC or GND, f = 1MHz
CIE2	Decoder Enable Input Capacitance (32K x 8) (Note 2)	-	25	pF	VI = VCC or GND, f = 1MHz
CIG1	Output Enable Input Capacitance (16K x 16) (Note 2)	-	50	pF	VI = VCC or GND, f = 1MHz
CIG2	Output Enable Input Capacitance (32K x 8) (Note 2)	-	25	pF	VI = VCC or GND, f = 1MHz
CIO1	Input/Output Capacitance (16K x 16) (Note 2)	-	150	pF	VI/O = VCC or GND, f = 1MHz
CIO2	Input/Output Capacitance (32K x 8) (Note 2)	-	250	pF	VI/O = VCC or GND, f = 1MHz
CIW	Write Input Capacitance (Note 2)	-	25	pF	VI = VCC or GND, f = 1MHz
CCVCC	Decoupling Capacitance (Note 2)	0.5	-	µF	f = 1MHz

NOTES:

1. VCC = 4.5V and 5.5V.
2. Tested at initial design and after major design changes.
3. ICCOP is proportional to operating frequency.

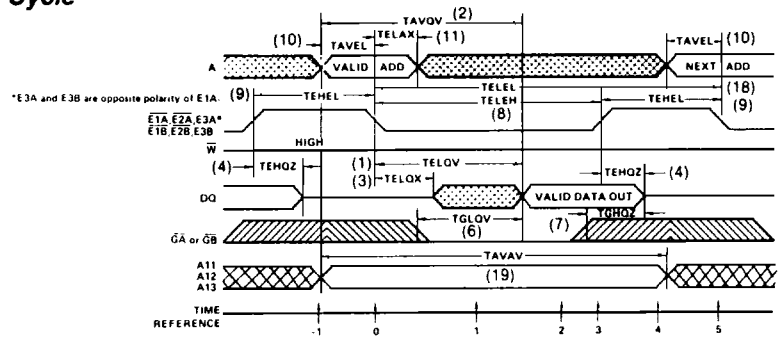
AC Electrical Specifications V_{CC} = 5V ± 10%; T_A = -55°C to +125°C (HM-92570-8)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
(1) TELQV	Chip Enable Access Time	-	250	ns	(Notes 1, 4)
(2) TAVQV	Address Access Time	-	270	ns	(Notes 1, 4)
(3) TELQX	Chip Enable Output Enable Time	5	-	ns	(Notes 2, 4)
(4) TEHQZ	Chip Enable Output Disable Time	-	150	ns	(Notes 2, 4)
(5) TGLQX	Output Enable Output Enable Time	10	-	ns	(Notes 2, 4)
(6) TGLQV	Output Enable Output Valid Time	-	120	ns	(Notes 1, 4)
(7) TGHQZ	Output Enable Output Disable Time	-	150	ns	(Notes 2, 4)
(8) TELEH	Chip Enable Pulse Negative Width	250	-	ns	(Notes 1, 4)
(9) TEHEL	Chip Enable Pulse Positive Width	100	-	ns	(Notes 1, 4)
(10) TAVEL	Address Setup Time	20	-	ns	(Notes 1, 3, 4)
(11) TELAX	Address Hold Time	120	-	ns	(Notes 1, 4)
(12) TWLWH	Write Enable Pulse Width	140	-	ns	(Notes 1, 4)
(13) TWLEH	Write Enable Pulse Setup Time	140	-	ns	(Notes 1, 4)
(14) TELWH	Write Enable Pulse Hold Time	250	-	ns	(Notes 1, 4)
(15) TDVWH	Data Setup Time	20	-	ns	(Notes 1, 4)
(16) TWHDX	Data Hold Time	70	-	ns	(Notes 1, 4)
(17) TWLDV	Write Data Delay Time	120	-	ns	(Notes 1, 4)
(18) TELEL	Read or Write Cycle Time	350	-	ns	(Notes 1, 4)
(19) TAVAV	Enable Decoder Address Valid Time	270	-	ns	(Applies Only to A11, A12, A13)

NOTES:

1. Input pulse levels: 0 to 3.0V; Input rise and fall times: 10ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
2. Tested at initial design and after major design changes.
3. Includes A11, A12, A13.
4. VCC = 4.5V and 5.5V.

Read Cycle



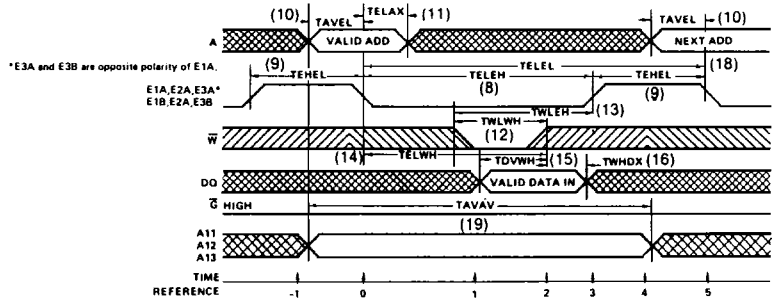
TRUTH TABLE

TIME REFERENCE	INPUTS $\overline{E}$	$\overline{W}$	$\overline{G}$	A	A11, A12, A13	DATA I/O DQ	FUNCTION
-1	H	X	X	X	X	Z	Memory Disabled
0	↘	H	X	V	V	Z	Cycle Begins, Addresses are Latched
1	L	H	L	X	V	X	Output Enabled
2	L	H	L	X	V	V	Output Valid
3	↗	H	X	X	V	V	Read Accomplished
4	H	X	X	X	X	Z	Prepare for Next Cycle (Same as -1)
5	↘	H	X	V	V	Z	Cycle Ends, Next Cycle Begins (Same as 0)

Read Cycle (Continued)

The address information is latched in the on chip registers on the falling edge of $\overline{E}$ (T = 0), minimum address setup and hold time requirements must be met. After the required hold time, the addresses may change state without affecting device operation. During time (T = 1), the outputs become enabled but data is not valid until time (T = 2), $\overline{W}$ must remain high throughout the read cycle. After the data has been read, $\overline{E}$ may return high (T = 3). This will force the output buffers into a high impedance mode at time (T = 4). $\overline{G}$ is used to disable the output buffers when in a logical "1" state (T = -1, 0, 3, 4, 5). After (T = 4) time, the memory is ready for the next cycle.

Write Cycle



TRUTH TABLE

TIME REFERENCE	INPUTS				A11, A12, A13	DATA I/O DQ	FUNCTION
	$\overline{E}$	$\overline{W}$	$\overline{G}$	A			
-1	H	X	H	X	X	X	Memory Disabled
0	↘	X	H	V	V	X	Cycle Begins, Addresses are Latched
1	L	L	H	X	V	X	Write Period Begins
2	L	↗	H	X	V	V	Data In Is Written
3	↗	H	H	X	V	X	Write Completed
4	H	X	H	X	X	X	Prepare For Next Cycle (Same As -1)
5	↘	X	H	V	V	X	Cycle Ends, Next Cycle Begins (Same As 0)

The write cycle is initiated on the falling edge of $\overline{E}$ (T = 0), which latches the address information in the on chip registers. If a write cycle is to be performed where the output is not to become active, $\overline{G}$ can be held high (inactive). TDVWH and TWHDX must be met for proper device operation regardless of $\overline{G}$. If $\overline{E}$ and $\overline{G}$ fall before $\overline{W}$ falls (read mode), a possible bus conflict may exist. If $\overline{E}$ rises before $\overline{W}$ rises, reference data setup and hold times to the $\overline{E}$ rising edge. The write operation is terminated by the first rising edge of $\overline{W}$ (T = 2) or $\overline{E}$ (T = 3). After the minimum $\overline{E}$ high time (TEHEL), the next cycle may begin. If a series of consecutive write cycles are to be performed, the $\overline{W}$ line may be held low until all desired locations have been written. In this case, data setup and hold times must be referenced to the rising edge of $\overline{E}$.