
HN62448 Series

524288-word \times 16-bit/1048576-word \times 8-bit CMOS
Mask Programmable ROM

HITACHI

ADE-203-397B (Z)

Rev. 2.0

Oct. 2, 1996

Description

The Hitachi HN62448 is a 8-Mbit CMOS mask-programmable ROM organized either as 524288-words by 16-bits or as 1048576-words by 8-bits. And a high speed access of 100/120 ns is the most suitable to the system using a high speed microcomputer by 16 bits.

Features

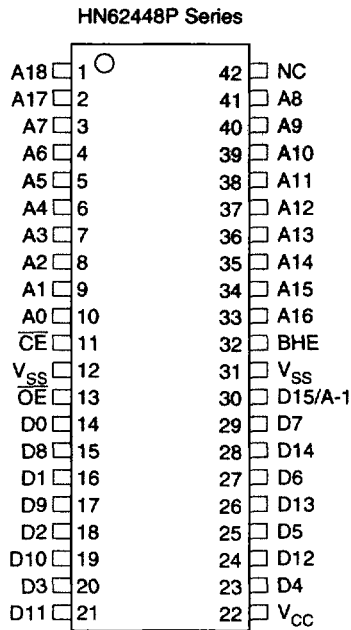
- Single 5 V power supply
- Access time:
 - Normal access time: 100/120 ns (max)
- Low power dissipation
 - Active: 300 mW (typ)
 - Standby: 5 μ W (typ)
- Byte-wide or word-wide data organization with BHE
- Three-state data output for wired or-tying
- Directly TTL compatible (All input and output)

Ordering Information

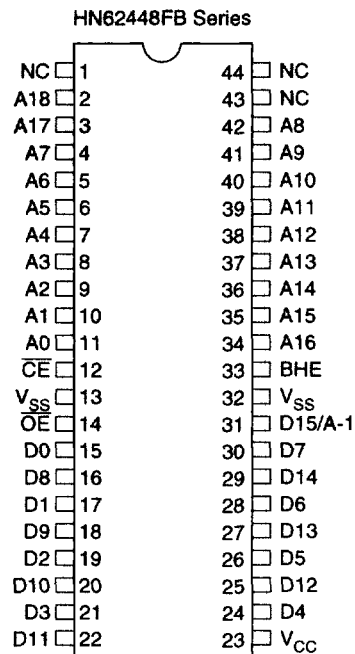
Type No.	Access time	Package
HN62448P-10	100 ns	600mil 42-pin plastic DIP (DP-42)
HN62448P-12	120 ns	
HN62448FB-10	100 ns	44-pin plastic SOP (FP-44D)
HN62448FB-12	120 ns	
HN62448TT-10	100 ns	44-pin plastic TSOP II (TTP-44D)
HN62448TT-12	120 ns	

HN62448 Series

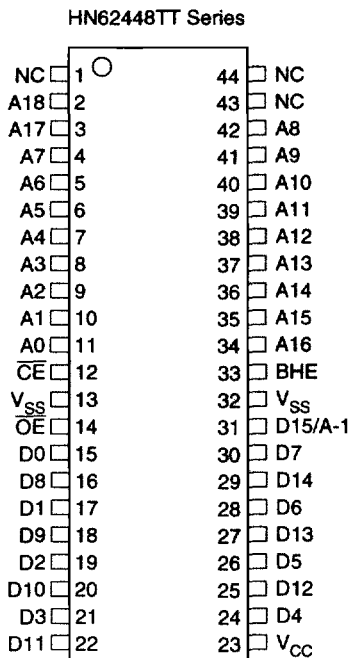
Pin Arrangement



(Top View)



(Top View)

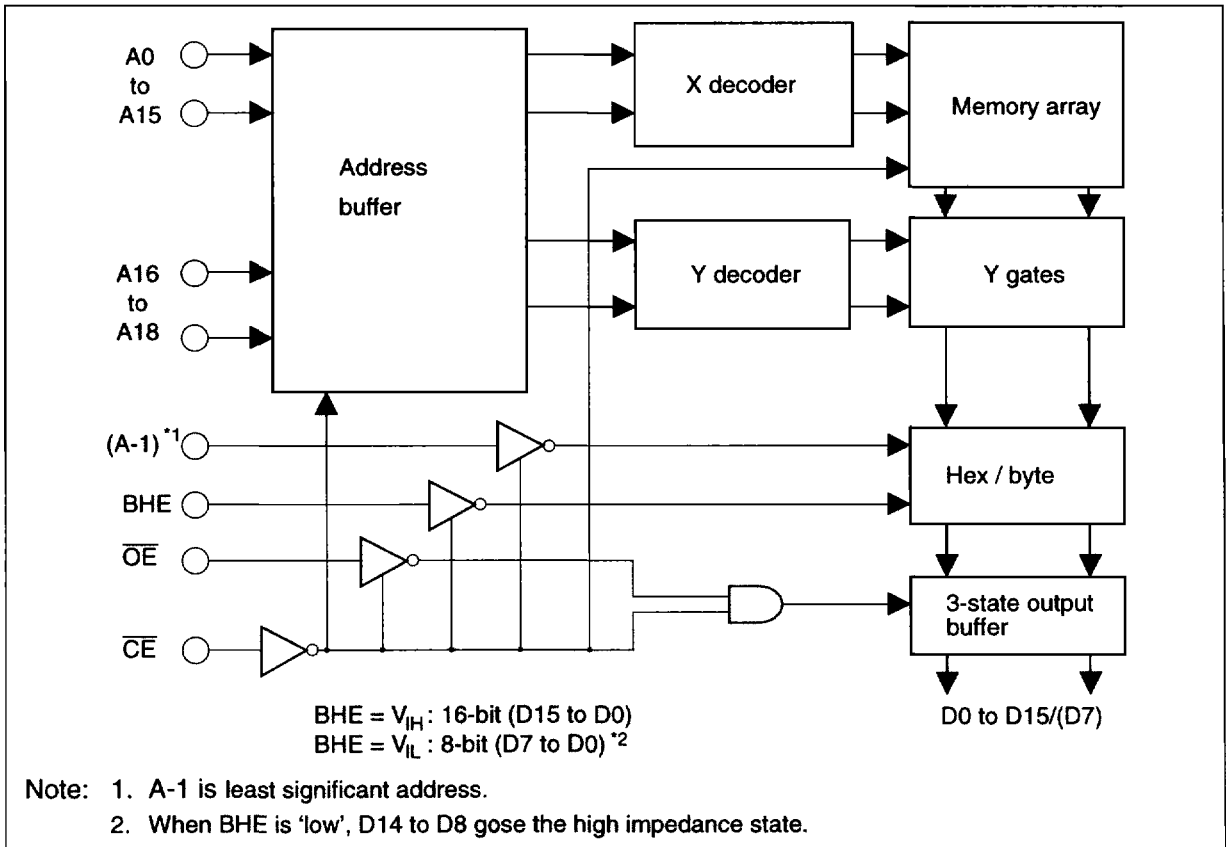


(Top View)

Pin Description

Pin name	Function
A0 to A18	Address input
D0 to D14	Data output
D15/A-1	Data output/address input
\overline{OE}	Output enable
\overline{CE}	Chip enable
BHE	Byte/word selection
V_{CC}	Power supply
V_{SS}	Ground
NC	No connection

Block Diagram



HN62448 Series

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit	Note
Supply voltage	V_{CC}	-0.3 to +7.0	V	1
All input and output voltage	V_{in}, V_{out}	-0.3 to $V_{CC} + 0.3$	V	1
Operating temperature range	T_{opr}	0 to 70	°C	
Storage temperature range	T_{stg}	-55 to +125	°C	
Temperature under bias	T_{bias}	-20 to +85	°C	

Note: 1. With respect to V_{SS} .

Recommended DC Operating Conditions ($T_a = 0$ to $+70^\circ\text{C}$)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input voltage	V_{IH}	2.2	—	$V_{CC} + 0.3$	V
	V_{IL}	-0.3	—	0.8	V

DC Characteristics ($V_{CC} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $T_a = 0$ to $+70^\circ\text{C}$)

Parameter	Symbol	Min	Max	Unit	Test conditions
Supply current	Active I_{CC}	—	100/80	mA	$V_{CC} = 5.5\text{ V}$, $I_{DOUT} = 0\text{ mA}$, $t_{RC} = 100/120\text{ ns}$
	Standby I_{SB1}	—	30	μA	$V_{CC} = 5.5\text{ V}$, $\overline{CE} \geq V_{CC} - 0.2\text{ V}$
	Standby I_{SB2}	—	3	mA	$V_{CC} = 5.5\text{ V}$, $\overline{CE} \geq 2.2\text{ V}$
Input leakage current	$ I_{IL} $	—	10	μA	$V_{in} = 0$ to V_{CC}
Output leakage current	$ I_{OL} $	—	10	μA	$\overline{CE} = 2.2\text{ V}$, $V_{OUT} = 0$ to V_{CC}
Output voltage	V_{OH}	2.4	—	V	$I_{OH} = -205\text{ }\mu\text{A}$
	V_{OL}	—	0.4	V	$I_{OL} = 1.6\text{ mA}$

Capacitance ($V_{CC} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $T_a = 25^\circ\text{C}$, $V_{in} = 0\text{ V}$, $f = 1\text{ MHz}$)

Parameter	Symbol	Min	Max	Unit
Input capacitance*1	C_{in}	—	15	pF
Output capacitance*1	C_{out}	—	15	pF

Note: 1. This parameter is periodically sampled and not 100% tested.

AC Characteristics ($V_{CC} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $T_a = 0\text{ to } +70^\circ\text{C}$)

Test Condition

- Output load: 1TTL gate + $C_L = 100\text{ pF}$ (including scope & jig)
- Input pulse levels: 0.45 to 2.8 V
- Input and output timing reference levels: 1.5V
- Input rise and fall time: 5 ns

Read Cycle

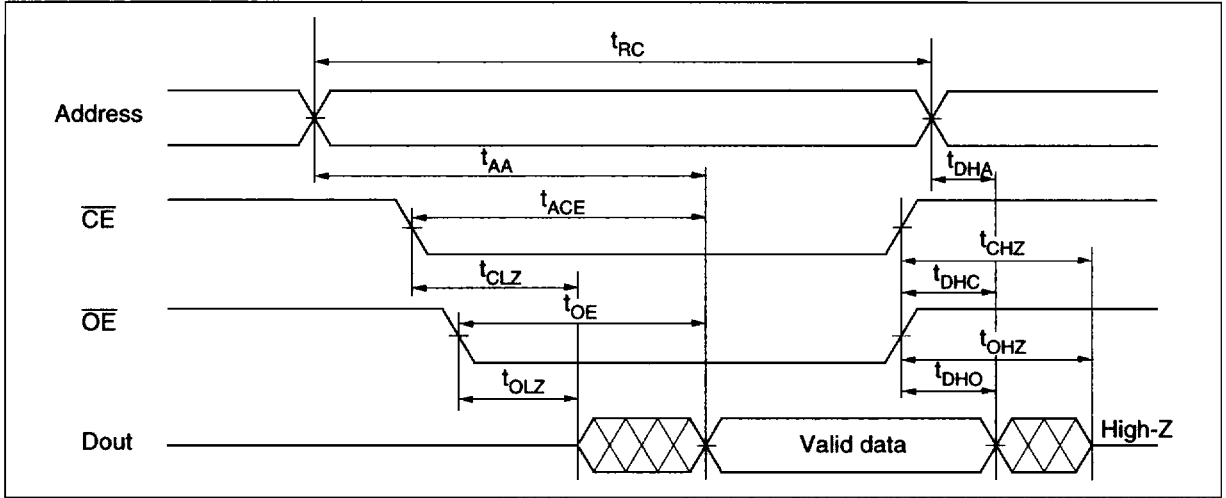
Parameter	Symbol	HN62448-10		HN62448-12		Unit	Note
		Min	Max	Min	Max		
Read cycle time	t_{RC}	100	—	120	—	ns	
Address access time	t_{AA}	—	100	—	120	ns	3
\overline{CE} access time	t_{ACE}	—	100	—	120	ns	3
\overline{OE} access time	t_{OE}	—	40	—	50	ns	3
BHE access time	t_{BHE}	—	100	—	120	ns	
Output hold time from address change	t_{DHA}	0	—	0	—	ns	2
Output hold time from \overline{CE}	t_{DHC}	0	—	0	—	ns	2
Output hold time from \overline{OE}	t_{DHO}	0	—	0	—	ns	2
Output hold time from BHE	t_{DHB}	0	—	0	—	ns	
\overline{CE} to output in high-Z	t_{CHZ}	—	40	—	40	ns	1
\overline{OE} to output in high-Z	t_{OHZ}	—	40	—	40	ns	1
BHE to output in high-Z	t_{BHZ}	—	40	—	40	ns	1
\overline{CE} to output in low-Z	t_{CLZ}	5	—	5	—	ns	4
\overline{OE} to output in low-Z	t_{OLZ}	5	—	5	—	ns	4
BHE to output in low-Z	t_{BLZ}	5	—	5	—	ns	

- Note:
1. t_{CHZ} , t_{OHZ} and t_{BHZ} are defined as the time at which the output achieves the open circuit conditions and are not referred to output voltage levels.
 2. t_{DHA} , t_{DHC} , t_{DHO} : Determined by faster.
 3. t_{AA} , t_{ACE} , t_{OE} : Determined by slower.
 4. t_{CLZ} , t_{OLZ} : Determined by slower.
 5. \overline{CE} and \overline{OE} are enable A18 to A0 are valid.
 6. D15/A-1 pin is in the output state when BHE is high, \overline{CE} and \overline{OE} are enable. Therefore, the input signals of opposite phase to the output must not be applied to them.
 7. This device is used ATD (Address Transient Detector). Therefore, transfer either \overline{CE} or address (A2 to A18) after power up to 4.5 V.

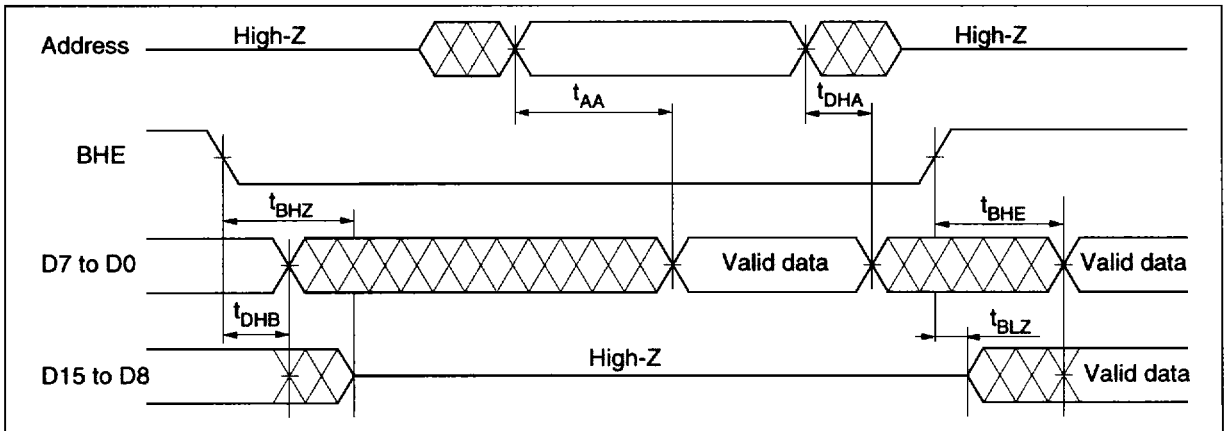
HN62448 Series

Timing Waveforms

Word Mode (BHE = 'V_{IH}') or Byte Mode (BHE = 'V_{IL}')*2,3,4



Word Mode, Byte Mode Switch*5,6



Power Up Sequence*7

