CMOS 14-STAGE COUNTER AND OSCILLATOR

FEATURES

- 14 Fully Static Stages
- 10 Buffered Outputs Available
- Common Reset Line
- 8MHz Counting Rate @ 10Vdc
- All Active Oscillator Components on Chip for R-C or Crystal Control

DESCRIPTION

The 4060 B consists of an oscillator section and 14 ripple-carry binary counter stages. The oscillator configuration allows design of either R-C or crystal oscillator circuits. A Reset input is provided which resets the counter to the all-0's state. A high level on the Reset line accomplishes the reset function. The state of the counter is advanced one step in binary order on the negative transition of the Clock input ϕ. All inputs and outputs are fully buffered. Outputs are available from stages 4 through 10 and 12 through 14.

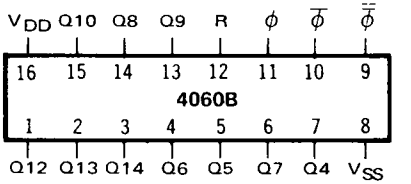
Applications include timers, frequency dividers, delay circuits and counter controls.

TRUTH TABLE

CLOCK	RESET	OUTPUT STATE
⌐‾	0	No Change
‾⌐	0	Advance to next state
X	1	All Outputs are low

X = Don't Care

CONNECTION DIAGRAM
(all packages)



Add suffix for package:

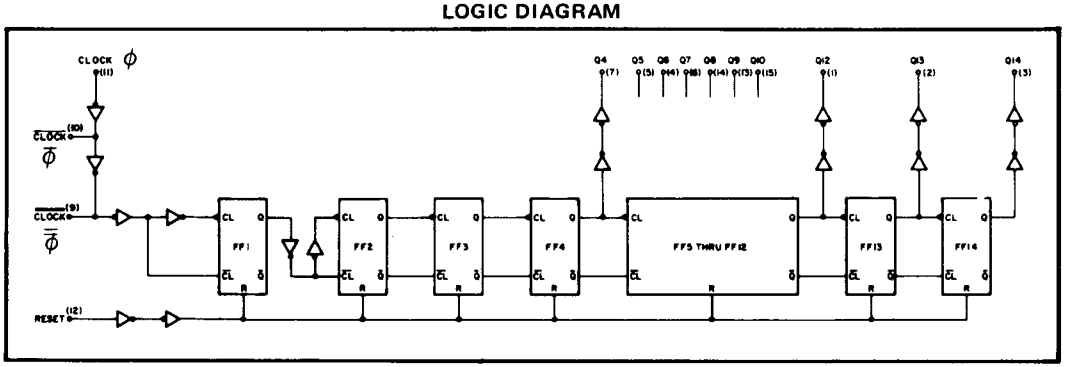
C 16-pin Cerdip
D 16-pin Ceramic
E 16-pin Epoxy
F 16-pin Flat
H Chip

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15 V_O
Operating Temperature	T_A	
C, D, F, H Device		-55 to +125 °C
E Device		-40 to +85 °C

LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS

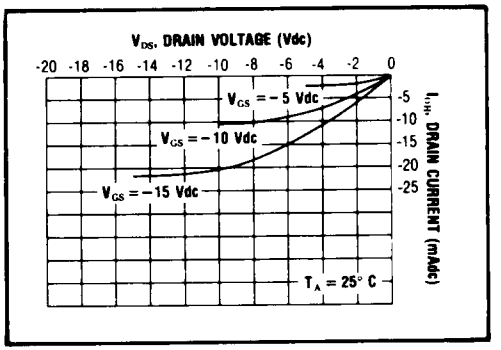
STATIC CHARACTERISTICS[1]

PARAMETER		V_{DD} (Vdc)	CONDITIONS	T_{LOW}[2]		+25°C			T_{HIGH}[2]		Units
				Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I_{DD}	5	$V_{IN}=V_{SS}$ or V_{DD}	–	5	–	0.05	5	–	150	μAdc
		10	All valid input	–	10	–	0.1	10	–	300	
		15	combinations	–	20	–	0.2	20	–	600	

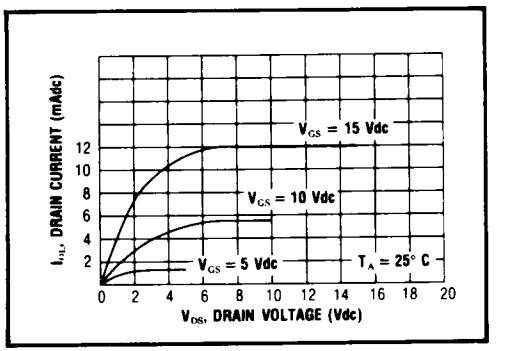
NOTES: [1] Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications".
[2] T_{LOW} = -55°C for C, D, F, H device.
= -40°C for E device.
T_{HIGH} = +125°C for C, D, F, H device.
= + 85°C for E device.

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER		V_{DD} (Vdc)	Min.	Typ.	Max.	Units
CLOCKED OPERATION						
PROPAGATION DELAY TIME Clock to Q4	t_{PLH}, t_{PHL}	5	–	400	800	ns
		10	–	200	400	
		15	–	150	300	
Q_i to $Q_i + 1$	t_{PLH}, t_{PHL}	5	–	100	200	ns
		10	–	40	80	
		15	–	30	60	
OUTPUT TRANSITION TIME	t_{TLH}, t_{THL}	5	–	100	200	ns
		10	–	40	80	
		15	–	30	60	
MINIMUM CLOCK PULSE WIDTH	PW_{CL}	5	–	70	140	ns
		10	–	30	60	
		15	–	20	40	
MAXIMUM CLOCK FREQUENCY	f_{CL}	5	3.0	4.5	–	MHz
		10	6.0	9.0	–	
		15	7.5	11.0	–	
MAXIMUM CLOCK RISE AND FALL TIME	t_{rCL}, t_{fCL}	5	50	100	–	μs
		10	50	100	–	
		15	50	100	–	
RESET OPERATION						
PROPAGATION DELAY TIME	t_{PHL}	5	–	200	400	ns
		10	–	100	200	
		15	–	75	150	
MINIMUM RESET PULSE WIDTH	PW_R	5	–	100	200	ns
		10	–	40	80	
		15	–	30	60	
RESET REMOVAL TIME	t_{rem}	5	–	150	300	ns
		10	–	65	125	
		15	–	40	75	

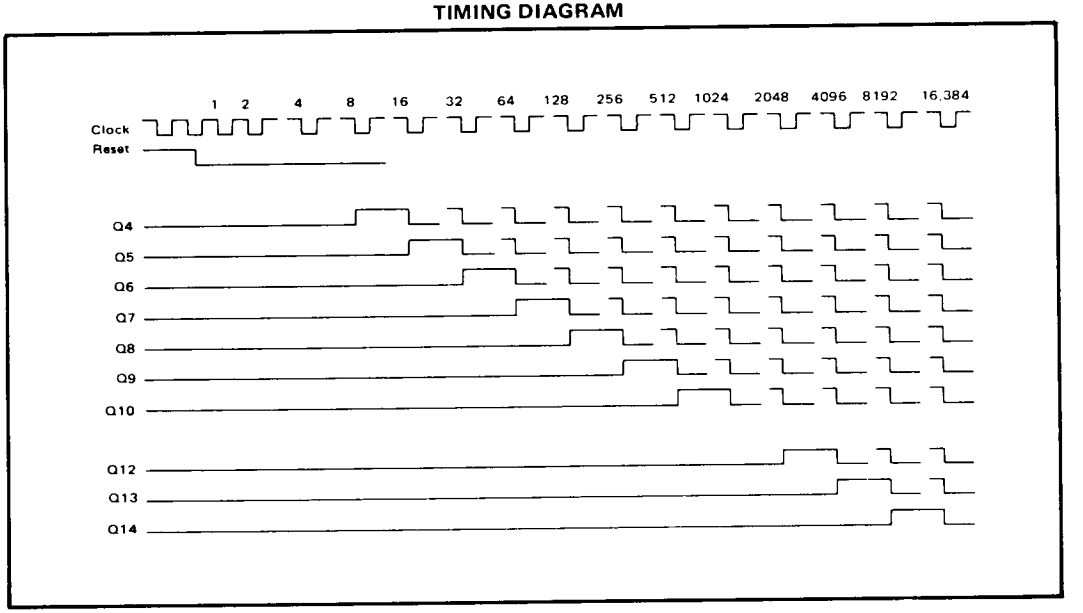


Typical P-Channel
Source Current Characteristics

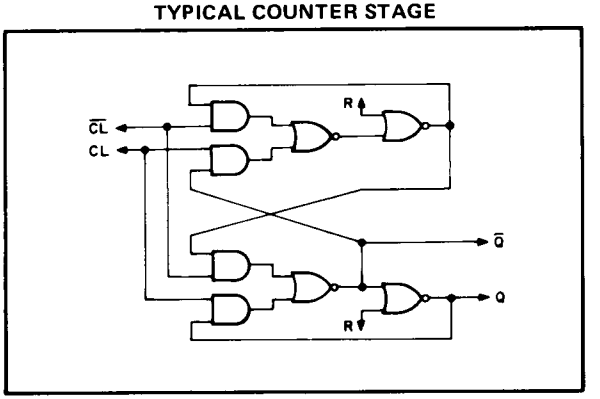


Typical N-Channel
Sink Current Characteristics

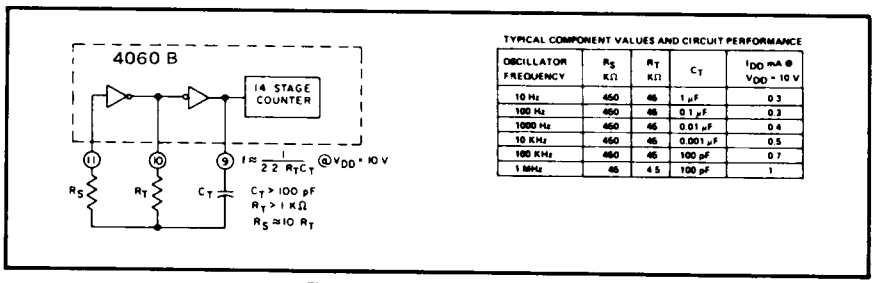
TIMING DIAGRAM



TYPICAL COUNTER STAGE



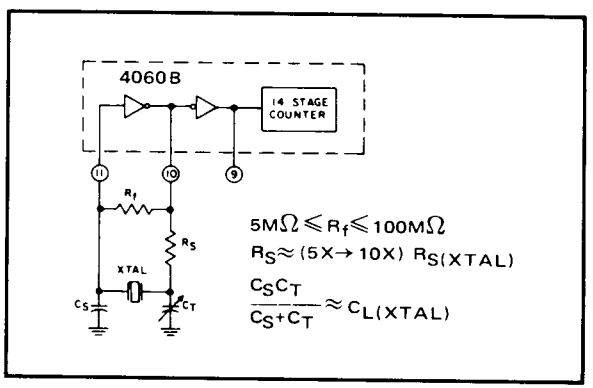
APPLICATIONS INFORMATION



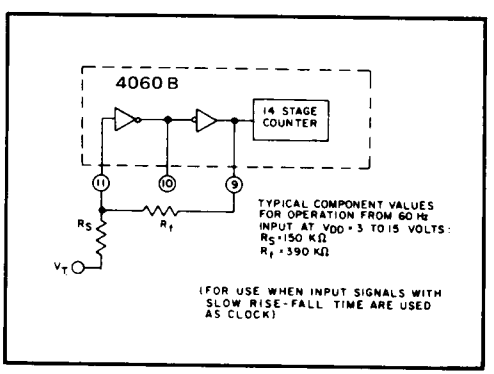
TYPICAL COMPONENT VALUES AND CIRCUIT PERFORMANCE

OSCILLATOR FREQUENCY	R_S KΩ	R_T KΩ	C_T	I_{DD} mA @ V_{DD} = 10 V
10 Hz	450	45	1 μF	0.3
100 Hz	450	45	0.1 μF	0.3
1000 Hz	450	45	0.01 μF	0.4
10 KHz	450	45	0.001 μF	0.5
100 KHz	450	45	100 pF	0.7
1 MHz	45	4.5	100 pF	1

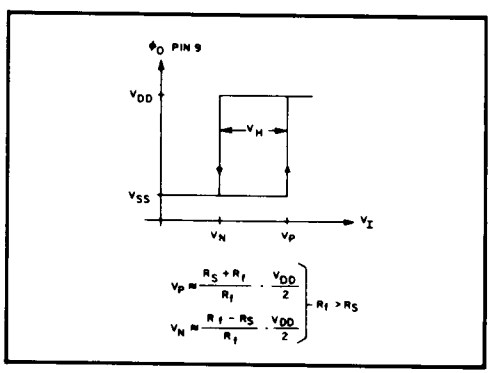
Typical RC oscillator circuit



Typical crystal oscillator circuit



Input pulse-shaping circuit (Schmitt trigger)



Input circuit characteristics for pulse-shaping circuit.