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ECL Products	

100160

Dual Parity Generator/8–Bit Comparator

FEATURES

- **Typical propagation delay: 1.8ns**
- **Typical supply current ($-I_{EE}$): 78mA**

DESCRIPTION

The 100160 acts as both a dual parity bit generator and an eight–bit comparator. The part accepts two eight–bit words as inputs (DA and DB). The parity bit QA (or QB) takes on a logic level such that the number of bits among DA and QA (DB and QB) that are high is odd. Thus the nine–bit word comprising DA and QA (DB and QB) possesses the property of odd parity. The Expansion Input XA (XB) can be used to expand the allowable word size of DA (or DB). Then parity bits can be generated for input words of 16 bits or more. The comparator function determines whether two 8–bit input words are equivalent or not. If each pair of Exclusive–OR gate inputs agree, then the comparator output $\overline{C}$ goes low. (See Logic Diagram.)

All unused inputs can be left open due to integrated pull–down resistors.

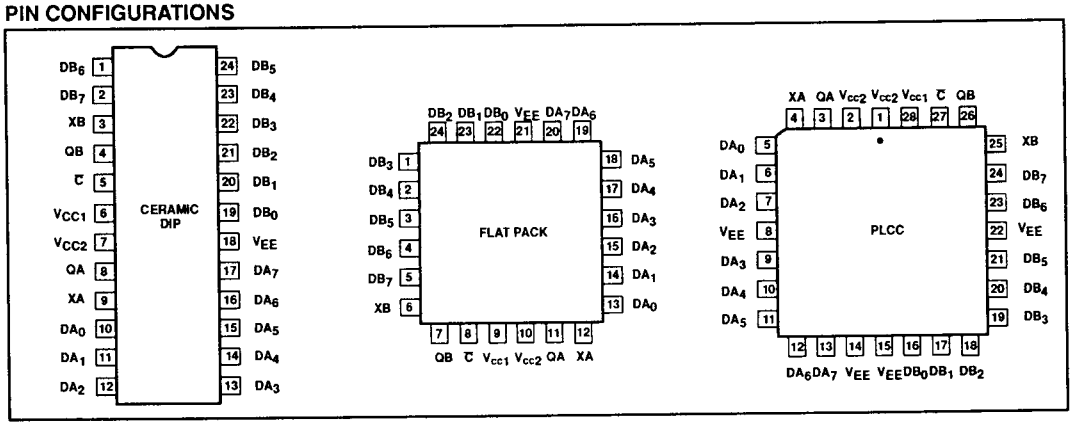
PIN DESCRIPTION

PINS	DESCRIPTION
DA_n, DB_n	Data Inputs
XA, XB	Expansion Inputs
$\overline{C}$	Compare Output
QA, QB	Odd Parity Outputs

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
24–Pin Ceramic DIP (400 mils wide)	100160F
24–Pin Ceramic Flat Pack	100160Y
28–Pin PLCC	100160A

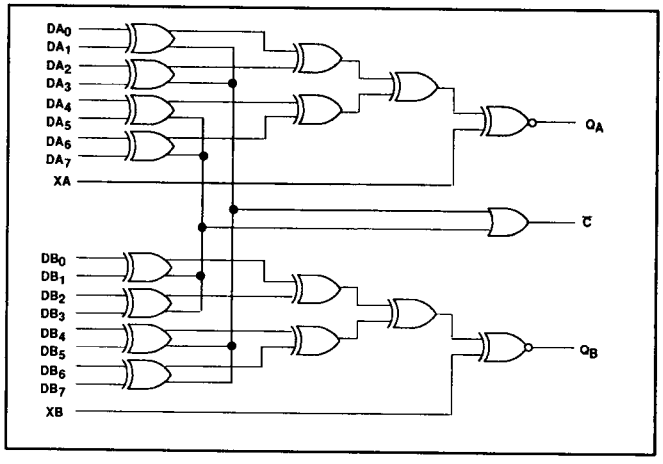
PIN CONFIGURATIONS



Parity Generator / Comparator

100160

LOGIC DIAGRAM



FUNCTION TABLE FOR PARITY BIT GENERATION

INPUTS	OUTPUT
DA_n	QA
DB_n	QB
Odd number of bits are high	L
Even number of bits are high	H

NOTES:
H = High voltage level
L = Low voltage level

FUNCTION TABLE FOR COMPARATOR ACTION

INPUTS	OUTPUT
DAn and DBn	$\overline{C}$
$DA_0 = DA_1$, and $DA_2 = DA_3$ and $DA_4 = DA_5$ and $DA_6 = DA_7$ and $DB_0 = DB_1$, and $DB_2 = DB_3$ and $DB_4 = DB_5$ and $DB_6 = DB_7$	L
All other combinations	H

NOTES:
H = High voltage level
L = Low voltage level

ABSOLUTE MAXIMUM RATINGS $V_{CC1} = V_{CC2}$ = ground, T_A = 0°C to +85°C unless otherwise specified.

SYMBOL	PARAMETER	LIMITS	UNIT
V_{EE}	Supply voltage range	–7.0 to +0.5	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})	V_{EE} to +0.5	V
I_O	Output source current (continuous)	–55	mA
T_S	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN.	NOM.	MAX.	
V_{CC1}, V_{CC2}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage		–4.8	–4.5	–4.2	V
V_{EE}	Supply voltage when operating with the 10K or the 10KH ECL family		–5.7			V
V_{IH}	High level input voltage	V_{EE} = –4.2V	–1150		–880	mV
		V_{EE} = –4.5V	–1165			
		V_{EE} = –4.8V	–1165			
V_{IL}	Low level input voltage	V_{EE} = –4.2V	–1810		–1475	mV
		V_{EE} = –4.5V			–1475	mV
		V_{EE} = –4.8V			–1490	mV
T_A	Operating ambient temperature range		0	+25	+85	°C

NOTE:
When operating at other than the specified V_{EE} voltages (–4.2V, –4.5V, –4.8V), the DC and AC electrical characteristics will vary slightly from their specified values.

DC ELECTRICAL CHARACTERISTICS

V_{CC1} = V_{CC2} = ground, V_{EE} = –4.8V to –4.2V, T_A = 0°C to +85°C unless otherwise specified[1,3,4]

SYMBOL	PARAMETER	TEST CONDITIONS[2]			LIMITS			UNIT
					MIN.	TYP.	MAX.	
V_{OH}	High level output voltage	Outputs loaded with 50Ω to –2.0V ±0.010V	Inputs at V_{IHMAX} or V_{ILMIN}	V_{EE} = –4.2V	–1020		–870	mV
				V_{EE} = –4.5V	–1025	–955	–880	mV
				V_{EE} = –4.8V	–1035		–880	mV
V_{OHT}	High level output threshold voltage		Apply V_{IHMIN} or V_{ILMAX} to one input at a time. Other inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V	–1030			mV
				V_{EE} = –4.5V	–1035			mV
				V_{EE} = –4.8V	–1045			mV
V_{OLT}	Low level output threshold voltage		Apply V_{IHMIN} or V_{ILMAX} to one input at a time. Other inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V			–1595	mV
				V_{EE} = –4.5V			–1610	mV
				V_{EE} = –4.8V			–1610	mV
V_{OL}	Low level output voltage		Inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V	–1810		–1605	mV
				V_{EE} = –4.5V	–1810	–1705	–1620	mV
				V_{EE} = –4.8V	–1830		–1620	mV
I_{IH}	High level input current	One input under test at V_{IHMAX}. Other inputs at V_{ILMIN}.					240	µA
I_{IL}	Low level input current	One input under test at V_{ILMIN}. Other inputs at V_{IHMAX}.			0.5			µA
$-I_{EE}$	V_{EE} supply current	All inputs at V_{IHMAX}			57	78	115	mA

NOTES:
1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC electrical characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC operating conditions table.
4. The device can function down to V_{EE} = –5.7V, allowing operation with either the 10K or the 10KH family. Correction factors can be used to calculate new DC limits for the extended V_{EE} range. For more information, see Chapters 5 and 10, Section 4.

AC ELECTRICAL CHARACTERISTICS

Ceramic DIP $V_{CC1} = V_{CC2}$ = ground, V_{EE} = –4.8V to –4.2V

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			T_A = 0°C		T_A = +25°C		T_A = +85°C		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay DA_n, DB_n to QA, QB	Waveform 1	1.30 1.30	4.30 4.30	1.30 1.30	4.10 4.10	1.30 1.30	4.30 4.30	ns ns
t_{PLH} t_{PHL}	Propagation delay XA, $\overline{XB}$ to QA, $\overline{QB}$		0.50 0.50	1.60 1.60	0.50 0.50	1.60 1.60	0.50 0.50	1.60 1.60	ns ns
t_{PLH} t_{PHL}	Propagation delay DA_n, DB_n to $\overline{C}$		1.20 1.20	3.30 3.30	1.20 1.20	3.10 3.10	1.20 1.20	3.30 3.30	ns ns
t_{TLH} t_{THL}	Transition time QA, QB, $\overline{C}$		0.40 0.40	1.70 1.70	0.40 0.40	1.65 1.65	0.40 0.40	1.65 1.65	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC ELECTRICAL CHARACTERISTICS

Ceramic DIP $V_{CC1} = V_{CC2}$ = ground, V_{EE} = –5.2V ± 5%

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			T_A = 0°C		T_A = +25°C		T_A = +85°C		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay DA_n, DB_n to QA, QB	Waveform 1	1.30 1.30	4.30 4.30	1.30 1.30	4.10 4.10	1.30 1.30	4.30 4.30	ns ns
t_{PLH} t_{PHL}	Propagation delay XA, XB to QA, QB		0.50 0.50	1.60 1.60	0.50 0.50	1.60 1.60	0.50 0.50	1.60 1.60	ns ns
t_{PLH} t_{PHL}	Propagation delay DA_n, DB_n to $\overline{C}$		1.20 1.20	3.30 3.30	1.20 1.20	3.10 3.10	1.20 1.20	3.30 3.30	ns ns
t_{TLH} t_{THL}	Transition time QA, QB, $\overline{C}$		0.40 0.40	1.70 1.70	0.40 0.40	1.65 1.65	0.40 0.40	1.65 1.65	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC ELECTRICAL CHARACTERISTICS

Flat Pack and PLCC $V_{CC1} = V_{CC2}$ = groind, V_{EE} = –4.8V to –4.2V

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			T_A = 0°C		T_A = +25°C		T_A = +85°C		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay DA_n, DB_n to QA, QB	Waveform 1	1.30 1.30	4.10 4.10	1.30 1.30	3.90 3.90	1.30 1.30	4.10 4.10	ns ns
t_{PLH} t_{PHL}	Propagation delay XA, XB to QA, QB		0.50 0.50	1.40 1.40	0.50 0.50	1.40 1.40	0.50 0.50	1.40 1.40	ns ns
t_{PLH} t_{PHL}	Propagation delay DA_n, DB_n to $\overline{C}$		1.20 1.20	3.10 3.10	1.20 1.20	2.90 2.90	1.20 1.20	3.10 3.10	ns ns
t_{TLH} t_{THL}	Transition time QA, QB, $\overline{C}$		0.40 0.40	1.70 1.70	0.40 0.40	1.65 1.65	0.40 0.40	1.65 1.65	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

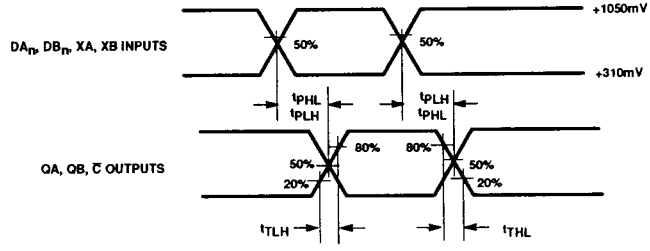
AC ELECTRICAL CHARACTERISTICS

Flat Pack and PLCC $V_{CC1} = V_{CC2} = \text{ground}$, $V_{EE} = -5.2V \pm 5\%$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay DA_n, DB_n to QA, QB	Waveform 1	1.30 1.30	4.10 4.10	1.30 1.30	3.90 3.90	1.30 1.30	4.10 4.10	ns ns
t_{PLH} t_{PHL}	Propagation delay XA, XB to QA, QB		0.50 0.50	1.40 1.40	0.50 0.50	1.40 1.40	0.50 0.50	1.40 1.40	ns ns
t_{PLH} t_{PHL}	Propagation delay DA_n, DB_n to $\overline{C}$		1.20 1.20	3.10 3.10	1.20 1.20	2.90 2.90	1.20 1.20	3.10 3.10	ns ns
t_{TLH} t_{THL}	Transition time QA, QB, $\overline{C}$		0.40 0.40	1.70 1.70	0.40 0.40	1.65 1.65	0.40 0.40	1.65 1.65	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC WAVEFORMS



Waveform 1. Propagation Delay and Transition Times

NOTE:
All power and signal voltages shifted up 2.0V for AC bench test purposes.