ISSUE B

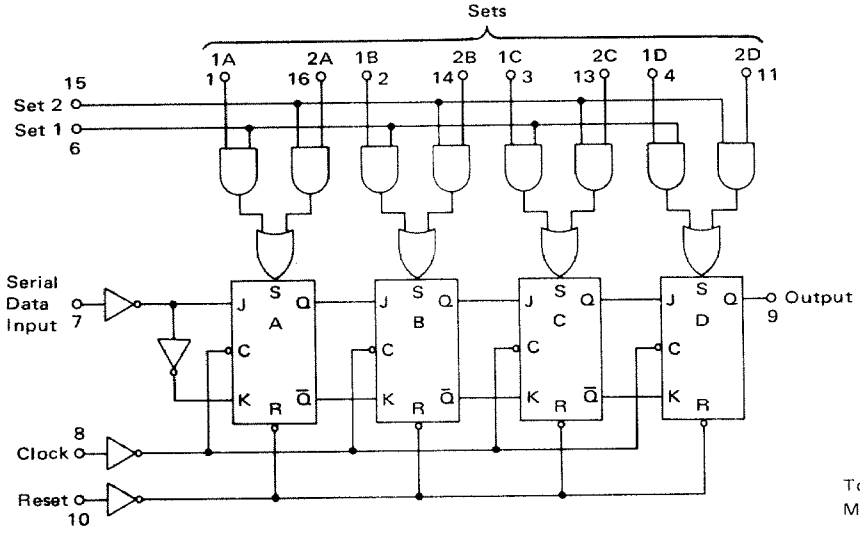
MC5494 • MC7494
MC9394 • MC8394

Add Suffix L for 16-pin ceramic dual in-line package (Case 620).
Suffix P for 16-pin plastic dual in-line package (Case 648) MC7494/MC8394 only.

This 4-bit register is designed for serial-out operation. Information can be accepted either serially or in parallel and then transferred to the slave-flip-flop on the positive edge of the clock.

A "1" level on the reset line forces all flip-flops to the "0" state resetting the register and inhibiting operation. The flip-flop can also be forced to the "1" level by placing the "1" levels on the necessary set inputs.

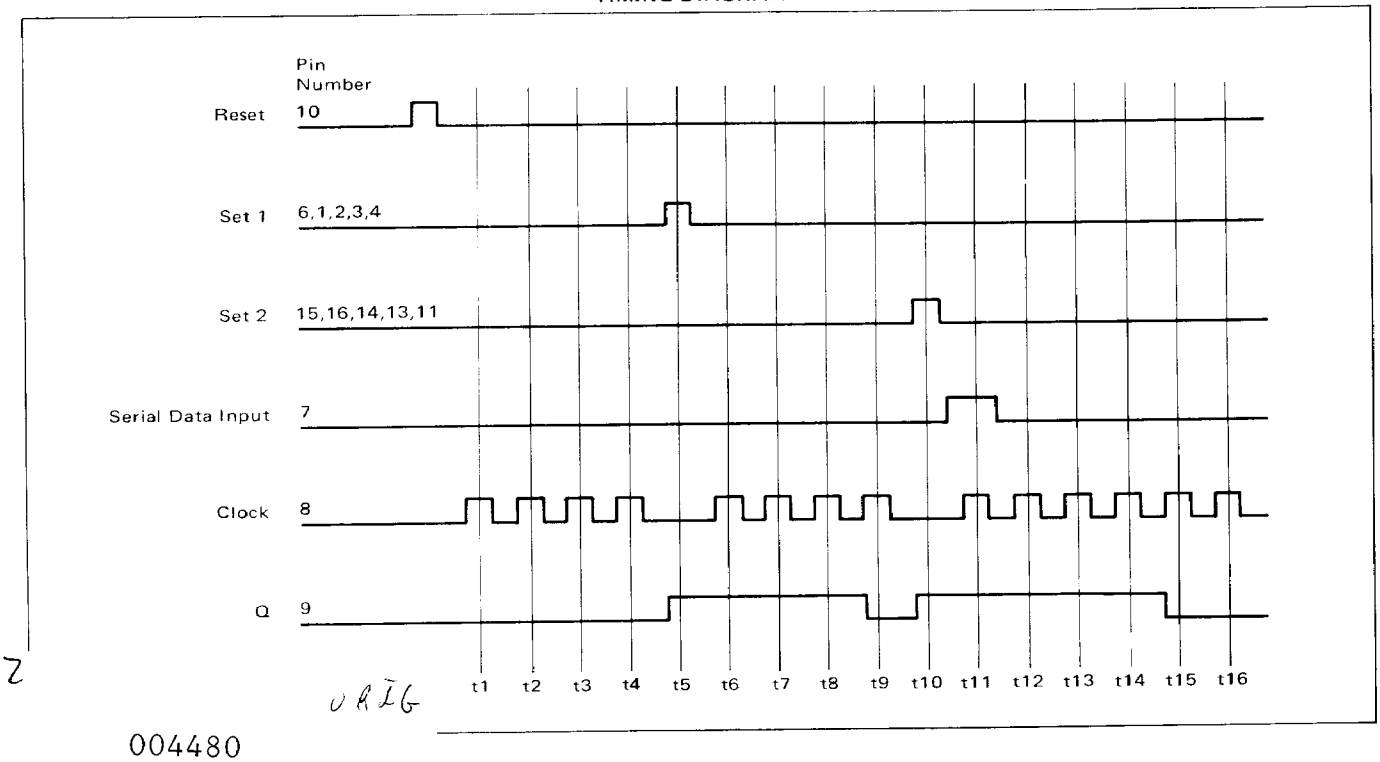
For serial-in operation, the information is entered through the serial-input and for parallel-in operation the flip-flops are set to the desired state by the proper use of the set and reset inputs. The reset input is independent of the clock, and the set inputs are independent of the clock and reset inputs.



V_{CC} = Pin 5
Gnd = Pin 12

Total Power Dissipation = 175 mW typ/pkg
Maximum Toggle Frequency = 10 MHz

TIMING DIAGRAM



ORIG

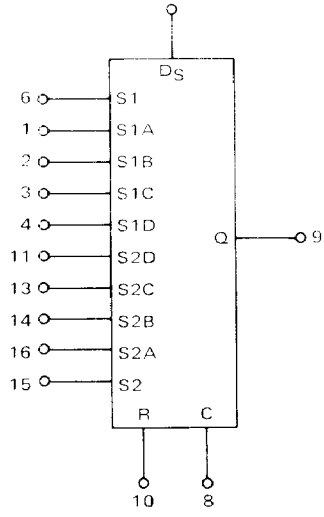
004480

4480

MOT

ELECTRICAL CHARACTERISTICS

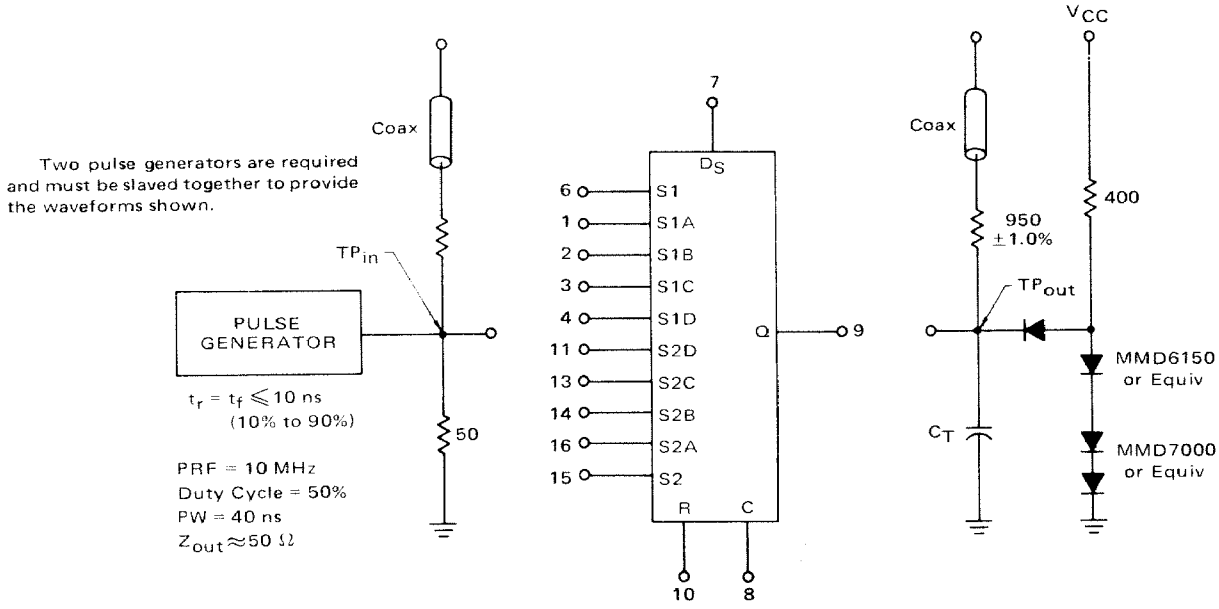
Test procedures are shown for only Set 1 and 1A inputs. The other inputs are tested in the same manner.



									TEST CURRENT/VOLTAGE (All Temperatures)									
									mA		Volts							
									I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_{IHH}	V_{ILT}	V_{IHT}	V_{CCL}	V_{CCH}	
								MC5494, MC9394	16	-0.4	0.4	2.4	5.5	0.8	2.0	4.5	5.5	
								MC7494, MC8394	16	-0.4	0.4	2.4	5.5	0.8	2.0	4.75	5.25	
Characteristic	Symbol	Pin Under Test	MC5494/MC9394 Test Limits -55 to +125°C			MC7494/MC8394 Test Limits 0 to +75°C			TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:									Gnd
			Min	Max	Unit	Min	Max	Unit	I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_{IHH}	V_{ILT}	V_{IHT}	V_{CCL}	V_{CCH}	
Input																		
Forward Current	I_{IL}	1		-1.6	mAdc		-1.6	mAdc			1					6	5	12
		6		-6.4	mAdc		-6.4	mAdc		–	6			–	–	1,2,3,4	5	12
Leakage Current	I_{IH}	1		40	µAdc		40	µAdc				1					5	6,12
		6		160	µAdc		160	µAdc				6				–	5	1,2,3,4,12
	I_{IHH}	1		1.0	mAdc		1.0	mAdc					1				5	6,12
		6		1.0	mAdc		1.0	mAdc					6				5	1,2,3,4,12
Output																		
Output Voltage	V_{OL}	9		0.4	Vdc		0.4	Vdc	9	–			–	6,15	10	5	–	12
	V_{OH}	9	2.4		Vdc	2.4		Vdc		9				–	4,6,11,15	5		12
Short Circuit Current	I_{OS}	9	-20	-57	mAdc	-18	-57	mAdc								4,6,11,15	5	9,12
Power Requirements (Total Device) Power Supply Drain	I_{CC}*	5		50	mAdc		58	mAdc								1,2,3, 7,8,11, 13,14,16	5	12
									Pulse In	Pulse Out								
Switching Parameters Clock to Q	f_{max}	8,9	10		MHz	10		MHz	7,8	9	–					–	5	6,10*,12,15
Propagation Delay Time Clock to Q	t_{PLH},t_{PHL}	9	–	40	ns	–	40	ns	7,8	9	–	–	–			–	5	6,12,10,15
Set to Q	t_{PLH2}	9		35	ns	–	35	ns	6,10	9				–	–	1,2,3,4	5	12,15
Reset to Q	t_{PHL2}	9	–	40	ns	–	40	ns	6,10	9	–			–	–	1,2,3,4	5	12,15

*Momentarily hold Reset at 4.5 V, then ground and test.

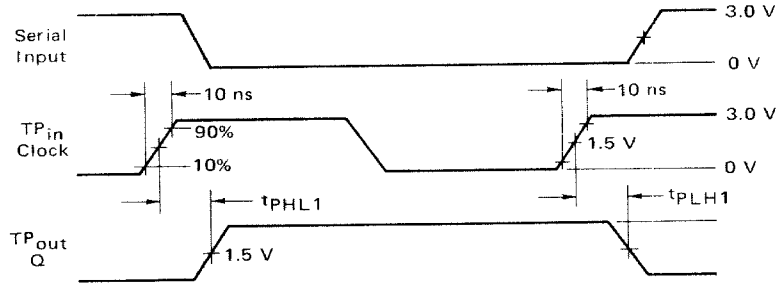
SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



C_T = 15 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe.

PROPAGATION DELAY – CLOCK TO OUTPUT



PROPAGATION DELAY – SET TO OUTPUT