SSI 32F8020A/8022A/8021/8023
Low-Power Programmable Electronic Filter

December 1993

DESCRIPTION

The SSI 32F8020A/8022A Programmable Electronic Filter provides an electronically controlled low–pass filter with a separate differentiated low–pass output. A seven–pole, 0.05° Equiripple-type linear phase, low–pass filter is provided along with a single-pole, single-zero differentiator. Both outputs have matched delays. The delay matching is unaffected by any amount of programmed equalization or bandwidth. The SSI 32F8021/8023 does not have differentiated outputs. This programability combined with low group delay variation makes the SSI 32F8020A/8022A/8021/8023 ideal for use in constant density recording applications. Double differentiation pulse slimming equalization is accomplished by a two–pole, low–pass with a two–pole, high–pass feed forward section to provide complimentary real axis zeros. A variable attenuator is used to program the zero locations.

The SSI 32F8020A/8022A programmable equalization and bandwidth characteristics can be controlled by external DACs or DACs provided in the SSI 32D4661

(continued)

FEATURES

- **Ideal for constant density recording applications**
- **Programmable filter cutoff frequency (fc = 1.5 to 8 MHz)**
- **Programmable pulse slimming equalization (0 to 9 dB boost at the filter cutoff frequency)**
- **Matched normal and differentiated low-pass outputs (SSI 32F8020A/8022A)**
- **Differential filter input and outputs**
- **±10% cutoff frequency accuracy**
- **±2% maximum group delay variation from 1.5 - 8 MHz**
- **Total harmonic distortion less than 1%**
- **No external filter components required**
- **+5V only operation**
- **16-pin SON and SOL package**

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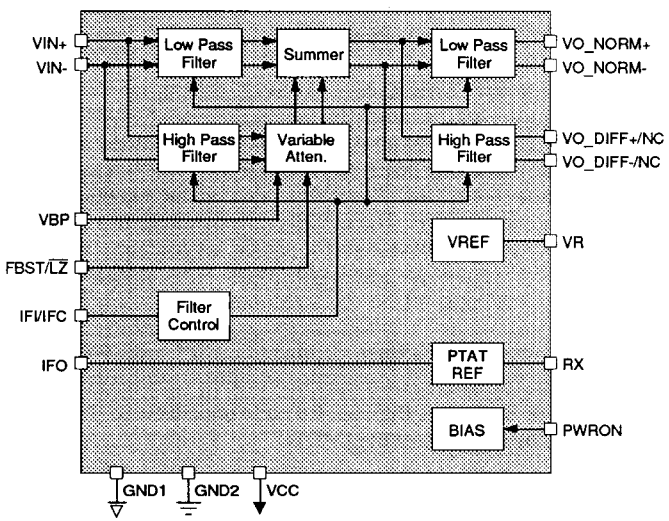
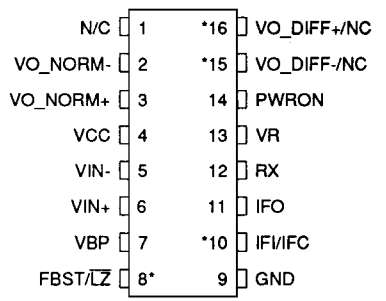
BLOCK DIAGRAM



PIN DIAGRAM



* Pin 8 = FBST - SSI 32F8020A/8021
LZ - SSI 32F8022A/8023

* Pin 10 = IFI - SSI 32F8020A/8022A
IFC - SSI 32F8021/8023

* Pin 15 & 16 = VO_DIFF - SSI 32F8020A/8022A
N/C - SSI 32F8021/8023

CAUTION: Use handling procedures necessary for a static sensitive component.

DESCRIPTION (continued)

SSI 32D4661 time base generator. Fixed characteristics are easily accomplished with three external resistors. External DACs are required for the SSI 32F8021/8023 to program the cutoff frequency. For the SSI 32F8020A/8021, equalization can be switched in or out by a logic signal. The input impedance of the SSI 32F8022A/8023 can be clamped low for fast recovery from input overload.

The SSI 32F8020A/8022A/8021/8023 require only a +5V supply and are available in 16-Lead SON and SOL packages.

FUNCTIONAL DESCRIPTION

The SSI 32F8020A/8022A/8021/8023 is a high performance programmable electronic filter. It features a 7-pole 0.05° phase equiripple filter with matched normal and differentiated outputs. The device has been optimized for usage with several Silicon Systems products, including the SSI 32D4661 Time Base Generator, the SSI 32P54X family pulse detectors, and the SSI 32P4720 combo chip (Data Separator and Pulse Detector).

CUTOFF FREQUENCY PROGRAMMING

The cutoff frequency, fc, of the SSI 32F8020A/8022A is defined as the -3dB filter bandwidth with no magnitude equalization applied, and is programmable from 1.5 MHz to 8 MHz.

The cutoff frequency is programmable with 3 pins: RX, IFO and IFI. At the RX pin, an external resistor to ground establishes a reference current:

$$IFO = \frac{0.75}{RX} \text{ at } T = 27°C$$

IFI should be made proportional to IFO for temperature stability. The cutoff frequency is related to the RX resistor, IFO and IFI currents as follows:

$$fc(MHz) = 8x\frac{IFI}{IFO}x\frac{1.25}{Rx(k\Omega)}$$

For a fixed cutoff frequency setting, IFO and IFI can be tied together. The cutoff frequency equation then reduces to:

$$fc(MHz) = 8x\frac{1.25}{Rx(k\Omega)}$$

For programmable cutoff frequency, an external current DAC can be used. The IFO should be the reference current into the DAC. The DAC output current drives IFI, which is then proportional to IFO. The DACF in the SSI 32D4661 Time Base Generator is designed to control fc of the Silicon Systems programmable filters. When the DACF, which has a 4X current from its reference to full scale output is used, a 5-kΩ RX is used. The fc is then given as follows:

$$fc(MHz) = 8x\frac{F\_Code}{127}$$

where F_Code is the decimal code equivalent to the 7-bit digital input for the DACF. The cutoff frequency programming for the SSI 32F8021/8023 is shown in Figure 3.

MAGNITUDE EQUALIZATION PROGRAMMING

The magnitude equalization, measured in dB, is the amount of high frequency peaking at the cutoff frequency relative to the original -3 dB point. For example, when 9 dB boost is applied, the magnitude response peaks up 6 dB above the DC gain.

The magnitude equalization is programmable with two pins: VR and VBP. The VR is a bandgap reference voltage, 2.3V typically. The voltage at the VBP pin determines the amount of high frequency boost. The boost function is as follows:

$$Boost(dB) = 20\log_{10}[1.884(\frac{VBP}{VR}) + 1]$$

For a fixed boost setting, a resistor divider between VR to ground can be used with the divided voltage at the VBP pin. For programmable equalization, an external voltage DAC can be used. VR should be the reference voltage to the DAC. The DAC output voltage is then proportional to VR. The DACS in the SSI 32D4661 is designed to control the magnitude equalization of Silicon Systems programmable filters. When DACS is used, the boost relation then reduces to:

$$Boost(dB) = 20\log_{10}[1.884(\frac{S\_Code}{127}) + 1]$$

where S_Code is the decimal code equivalent to the 7-bit digital input for the DACS.

For the SSI 32F8020A/8021, the equalization function can be disabled when FBST is pulled to logic 0. For the SSI 32F8022A/8023, the VBP pin should be grounded to achieve 0 dB boost.

LOW INPUT IMPEDANCE (SSI 32F8022A/8023 only)

When the LZ is at logic 1 or left open, the SSI 32F8022A/8023 input is at high impedance state. When the LZ is pulled to logic 0, the SSI 32F8022A/8023 input is clamped to a low impedance state, 200 Ω typical.

POWER ON/OFF

The SSI 32F8020A/8022A/8021/8023 support a power down mode for minimal Idle mode power dissipation. When PWRON is pulled up to logic 1, the device is in normal operation mode. When PWRON is pulled down to logic 0, or left open, the device is in the power down mode.

PIN DESCRIPTION

NAME	DESCRIPTION
VIN+, VIN-	DIFFERENTIAL SIGNAL INPUTS.
VO_NORM+, VO_NORM-	DIFFERENTIAL NORMAL OUTPUTS.
VO_DIFF+ VO_DIFF-	DIFFERENTIAL DIFFERENTIATED OUTPUTS.
RX	PTAT REFERENCE CURRENT SET. PTAT (proportional to absolute temperature) reference current IFO is equivalent to the current set on this pin.
IFO	PTAT CURRENT REFERENCE OUTPUT. This pin ouputs a PTAT reference current which is externally scaled for control input into IFI.
IFI	FREQUENCY PROGRAM INPUT. The filter cutoff frequency *fc*, is set by an external current IFI, injected into this pin. IFI must be proportional to current IFO. This current can be set with an external current generator such as a DAC, referenced to IFO.
VBP	FREQUENCY BOOST PROGRAM INPUT. The slimmer high frequency boost is set by an external voltage applied to this pin. VBP must be proportional to voltage VR. A fixed amount of boost can be set by an external resistor divider network connected from VBP to VR and GND. No boost is applied if the FBST pin is grounded, or at logic low.
FBST (32F8020A/8021)	FREQUENCY BOOST. A high logic level or open input enables the frequency boost circuitry. No boost is applied if the FBST pin is grounded, or at logic low.
$\overline{LZ}$ (32F8022A /8023)	LOW IMPEDANCE MODE. With a low logic level, the analog input impedance is switched low for fast recovery from input overload. With a high logic level or left open, the input is at high impedance state.
PWRON	POWER ON. A high logic level circuit enables the chip. A low level puts the chip in a low power state. A low or open circuit disables the chip.
VR	REFERENCE VOLTAGE. Internally generated reference voltage.
VCC	+5 VOLT SUPPLY.
GND	GROUND

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation above maximum ratings may damage the device.

PARAMETER	RATING
Storage Temperature	-65 to +150°C
Junction Operating Temperature, Tj	+130°C
Supply Voltage, VCC	-0.5 to 7V
Voltage Applied to Inputs	-0.5 to VCCV

RECOMMENDED OPERATING CONDITIONS

Supply voltage, VCC	4.50V < VCC < 5.50V
Ambient Temperature	0°C < Ta < 70°C

Power Supply Characteristics

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
ICC	Power Supply Current	PWRON ≤ 0.8V			0.5	mA
		PWRON ≥ 2.2V SSI 32F8021/8023		26	32	mA
		PWRON ≥ 2.2V SSI 32F8020A/8022A		35	41	mA
PD	Power Dissipation	PWRON ≤ 0.8V			3	mW
		PWRON ≥ 2.2V, VCC = 5V SSI 32F8021/8023		130	160	mW
		PWRON ≥ 2.2V, VCC = 5.5V SSI 32F8021/8023		143	176	mW
		PWRON ≥ 2.2V, VCC = 5V SSI 32F8020A/8022A		175	205	mW
		PWRON ≥ 2.2V, VCC = 5.5V SSI 32F8020A/8022A		193	226	mW

DC Characteristics

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
VIH	High Level Input Voltage	TTL input	2.0			V
VIL	Low Level Input Voltage				0.8	V
IIH	High Level Input Current	VIH = 2.7V			20	µA
IIL	Low Level Input Current	VIL = 0.4V	-1.5			mA
VICM	VIN± Input Common Mode Voltage		(V_{CC} -1.5) -0.3		(V_{CC} -1.5) +0.3	V
VOCM	VO_NORM± Output Common Mode Voltage		VCC-2.3 -0.5		VCC-2.3 +0.5	V
VOFF	VO_NORM± Output Offset	VIN± open	-0.4		+0.4	V

Filter Characteristics

fc	Filter Cutoff Frequency	Rx = 5kΩ $fc\ (MHz) = 8 \cdot \frac{IFI}{4 \cdot IFO}$ (32F8020A/8022A) $fc\ (MHz) = 8 \cdot \frac{IFC}{4 \cdot IFO}$ (32F8021/8023)	1.5		8.0	MHz
FCA	Filter fc Accuracy	fc (nominal) = 8 MHz	–10		+10	%
AO	VO_NORM Diff Gain	F = 0.67 fc, FB = 0 dB	0.8	1.0	1.2	V/V
AD	VO_DIFF Diff Gain (32F8020A/8022A)	F = 0.67 fc, FB = 0 dB	0.8AO		1.2AO	V/V
FB	Frequency Boost at fc	$FB(db)=20 \log\left[1.884\left(\frac{VBP}{VR}\right)+1\right]$ VBP = VR		9.2		dB
FBA	Frequency Boost Accuracy	FB (ideal) = 9.2 dB	–1		+1	dB
TGD0	Group Delay Variation Without Boost	fc = 8 MHz, VBP = 0V F = 0.2 fc to 1.75 fc	–1.3		+1.3	ns
		fc = 1.5 MHz - 8 MHz F = 0.2 fc to 1.75 fc, VBP = 0V	–2		+2	%
TGDB	Group Delay Variation With Boost	fc = 8 MHz, VBP = VR F = 0.2 fc to 1.75 fc	–1.3		+1.3	ns
		fc = 1.5 MHz - 8 MHz F = 0.2 fc to 1.75 fc, VBP = VR	–2		+2	%

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ELECTRICAL SPECIFICATIONS (continued)

Filter Characteristics (continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
VOF Filter Output Dynamic Range	THD = 1% max, F = 0.67 *fc*	1.0			Vpp
VOF Filter Output Dynamic Range	THD = 1.5%, F = 0.67 *fc* VO_DIFF±, *fc* =1.5 MHz, 0 < Ta < 10°C, THD = 2%, F = 0.67 *fc*	1.5			Vpp
RIN Filter Diff Input Resistance	32F8020A/8021 32F8022A/8023 LZ = 1 or open	3.0	4.0		kΩ
	32F8022A/8023 LZ = 0		200	400	Ω
CIN Filter Input Capacitance				7	pF
EOUT Output Noise Voltage Differentiated Output	BW = 100 MHz, Rs = 50Ω *fc* = 8 MHz, VBP = 0.0V (32F8020A/8022A)		6.3	7.5	mVRms
EOUT Output Noise Voltage Normal Output	BW = 100 MHz, Rs = 50Ω *fc* = 8 MHz, VBP = 0.0V		2.7	4.0	mVRms
EOUT Output Noise Voltage Differentiated Output	BW = 100 MHz, Rs = 50Ω *fc* = 8 MHz, VBP = VR (32F8020A/8020A)		9.4	11.0	mVRms
EOUT Output Noise Voltage Normal Output	BW = 100 MHz, Rs = 50Ω *fc* = 8 MHz, VBP = VR		3.7	4.5	mVRms
IO– Filter Output Sink Current		1.0			mA
IO+ Filter Output Source Current		2.0			mA
RO Filter Output Resistance (Single ended)	IO+ = 1.0 mA			60	Ω

Filter Control Characteristics

VR	Reference Voltage		2.2		2.45	V
VBP	Frequency Boost Control Voltage Range	VR = 2.3V FBOOST = 0 to 9.2 dB	0		2.3	V
VRX	PTAT Reference Current Set Output Voltage	TA = 25°C IRX = 0 - 0.6 mA Rx > 1.25 kΩ		750		mV
IFO	PTAT Reference Current, Output Current Range	TA = 25°C 1.25 kΩ < Rx < 6.8 kΩ IFO = VRX/Rx VRX = 750 mV	0.11		0.6	mA
RIFO	IFO Output Impedance		50			kΩ
VIFO	IFO Voltage Compliance		0		Vcc -1	V

Filter Control Characteristics

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
IFI	PTAT Programming Current Range	TA = 25°C, VRX = 750 mV 32F8020A/8022A	0.11		0.6	mA
RIFI	IFI Input Impedance	32F8020A/8022A	1.0		2.5	kΩ
VIFI	IFI Voltage Compliance	32F8020A/8022A	0.5		2.5	V
IFC	PTAT Programming Current Range	TA = 25 °C, VRX = 750 mV 32F8021/8023	0.11		0.6	mA
TPWR	Power On Recovery Time	DC voltages within 20 mV of final values			500	ns
TBST	Boost Change Recovery	DC voltages within 20 mV of final values			500	ns
TFBW	Bandwidth Change Recovery	DC voltages within 20 mV of final values			500	ns

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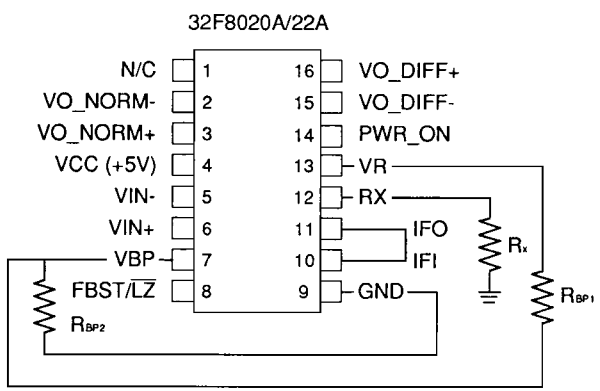


VR = 2.3V

VRX = 750 mV @25°C

IFO = VRX/Rx

IFI range: 0.11 mA to 0.60 mA @25°C

(1.5 to 8 MHz NO BOOST)

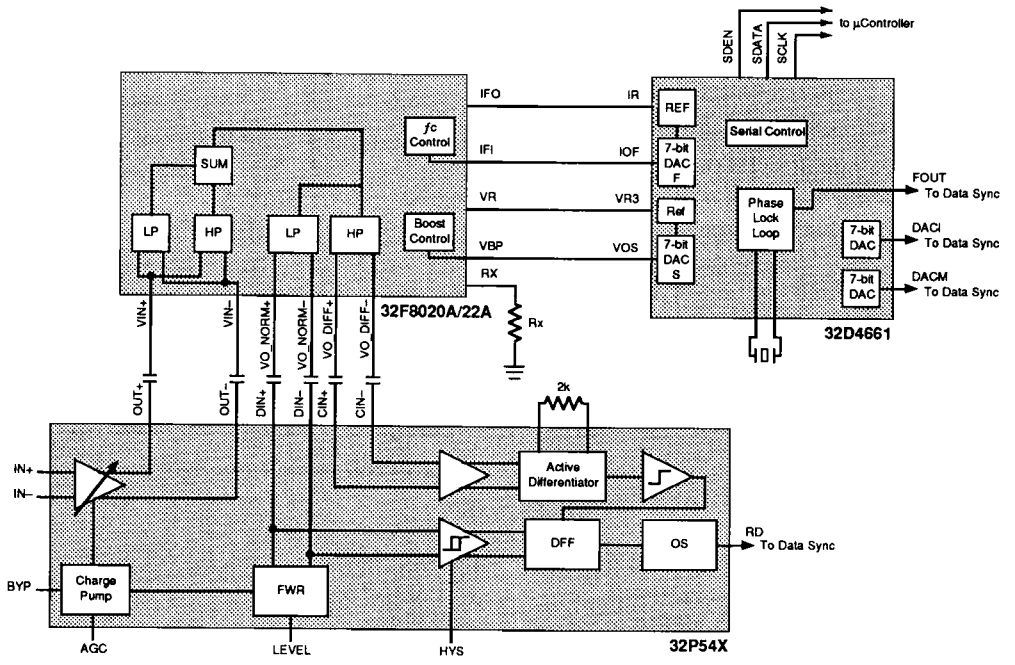
Fixed frequency programming is accomplished as shown in the drawing above. In this case IFI (programming current) is equivalent to IFO (reference current). Programming current is then set by VRX/Rx.

where: fc = 8.0 MHz then

IFI = IFO = 0.60 mA @25 °C

Rx = 750 mV/0.60 mA = 1.25 kΩ

FIGURE 1: 32F8020A/8022A Applications Setup



VR = 2.3V

VRX = 750 mV @25°C

IFO = VRX/Rx

IFI range: 0.11 mA to 0.60 mA @25°C

(1.5 to 8 MHz NO BOOST)

In this case the IFI (programming current) is scaled from IFO (reference current) through DACF on the 32D4661. DACF has a current gain of 4; therefore, the reference current should be set to 25% of the maximum desired IFI (programming current).

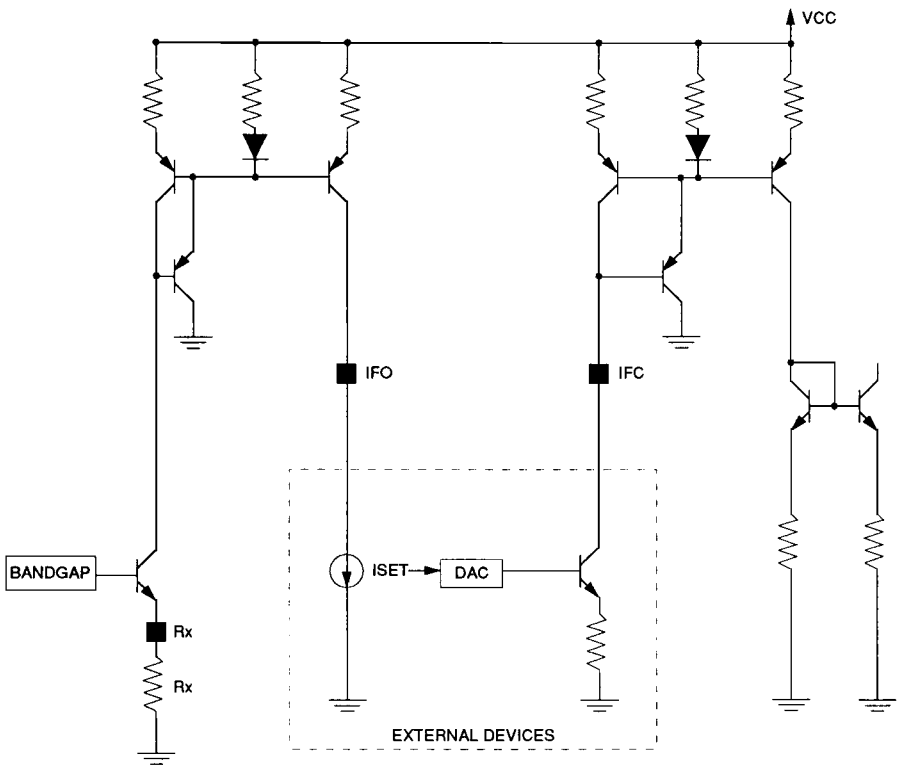
where: fc (max) = 8.0 MHZ then

IFI (max) = 0.60 mA @25°C

IFO (max) = 0.15 mA

therefore Rx = 750 mV/0.15 mA = 5 kΩ

FIGURE 2: Applications Setup, Constant Density Recording 32F8020A/8022A, 32P54X, 32D4661



VRX = 750 mV @25°C

IRX = IFO

IFC programming range: 0.11 mA to 0.60 mA @25°C
(1.5 to 8.0 MHz: No Boost)

The IFC (programming current) is scaled from IFO (reference current) by the set-up shown above. Assuming the DAC current gain = 4.0, then programming is accomplished as follows:

MAX programming current required: IFC = 0.6 mA (fc = 8.0 MHz) @25°C

IFO = IFC/8 = 0.075 mA (MAX) @25°C

IRX = IFO

IRX = 750mV/Rx @25°C

Rx = 5 kΩ

FIGURE 3: 32F8021/8023 Frequency Programming

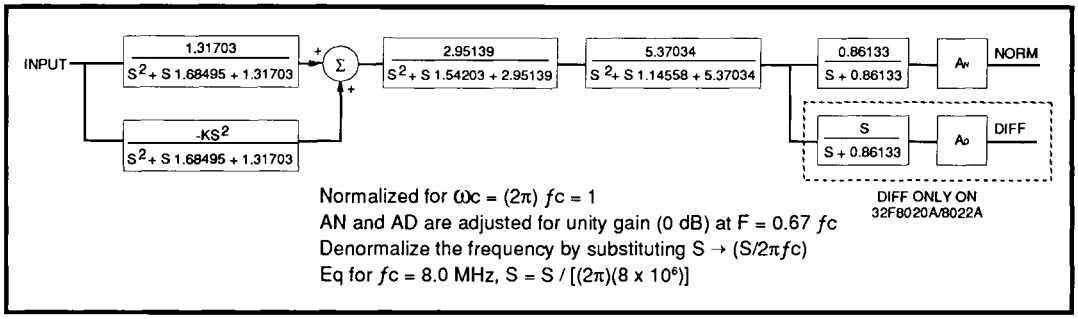


FIGURE 4: 32F8020A/8022A/8021/8023 Normalized Block Diagram

TABLE 1: 32F8020A/8022A Frequency Boost Calculations. $K = 1.31703\,(10^{\frac{\text{BOOST (dB)}}{20}} - 1)$

Assuming 9.2 dB boost for **VBP = VR**

$$\frac{VBP}{VR} \cong \frac{\left(10^{(FB/20)}\right) - 1}{1.884}$$

Boost	VBP/VR	K
1 dB	0.065	0.16
2 dB	0.137	0.34
3 dB	0.219	0.54
4 dB	0.310	0.77
5 dB	0.413	1.03
6 dB	0.528	1.31
7 dB	0.658	1.63
8 dB	0.802	1.99
9 dB	0.965	2.40

or,

$$\text{boost in dB} \cong 20 \log \left[1.884 \left(\frac{VBP}{VR} \right) + 1 \right]$$

VBP/VR	Boost
0.1	1.499 dB
0.2	2.777 dB
0.3	3.891 dB
0.4	4.879 dB
0.5	5.765 dB
0.6	6.569 dB
0.7	7.305 dB
0.8	7.984 dB
0.9	8.613 dB
1.0	9.200 dB

TABLE 2: Calculations
Typical change in f-3 dB point and frequency peak with boost.

Boost (dB)	Gain@fc (dB)	Gain@peak (dB)	$f$peak/fc	f-3 dB/fc
0	-3	0.00	no peak	1.00
1	-2	0.00	no peak	1.21
2	-1	0.00	no peak	1.51
3	0	0.15	0.70	1.80
4	1	0.99	1.05	2.04
5	2	2.15	1.23	2.20
6	3	3.41	1.33	2.33
7	4	4.68	1.38	2.43
8	5	5.94	1.43	2.51
9	6	7.18	1.46	2.59

NOTES: 1. fc is the original programmed cutoff frequency with no boost.

2. f-3 dB is the new -3 dB value with boost implemented.

3. $f$peak is the frequency where the magnitude peaks when boost is implemented.

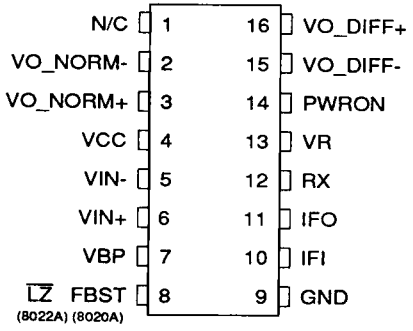
i.e., fc = 8 MHz when boost = 0 dB if boost is programmed to 5 dB then

f-3 dB = 17.6 MHz

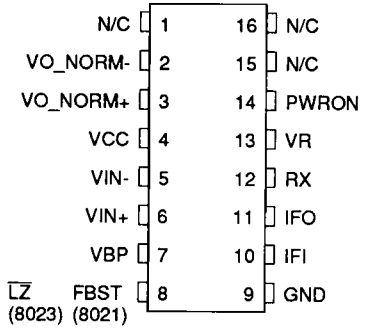
$f$peak = 9.84 MHz

SSI 32F8020A/8022A/8021/8023
Low-Power Programmable Electronic Filter

PACKAGE PIN DESIGNATIONS
(Top View)



32F8020A/8022A
16-Lead SON, SOL



32F8021/8023
16-Lead SON, SOL

THERMAL CHARACTERISTICS: θja

16-Lead SON, SOL (150 mil)	105° C/W

CAUTION: Use handling procedures necessary for a static sensitive component.

ORDERING INFORMATION

PART DESCRIPTION		ORDER NUMBER	PACKAGE MARK
SSI 32F8020A	16-Lead SON	32F8020A-CN	32F8020A-CN
	16-Lead SOL	32F8020A-CL	32F8020A-CL
SSI 32F8022A	16-Lead SON	32F8022A-CN	32F8022A-CN
	16-Lead SOL	32F8022A-CL	32F8022A-CL
SSI 32F8021	16-Lead SON	32F8021-CN	32F8021-CN
	16-Lead SOL	32F8021-CL	32F8021-CL
SSI 32F8023	16-Lead SON	32F8023-CN	32F8023-CN
	16-Lead SOL	32F8023-CL	32F8023-CL

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680-7022 (714) 573-6000, FAX (714) 573-6914