HARRIS SEMICONDUCTOR

HI2559, CXD2559

NOT RECOMMENDED FOR NEW DESIGNS

October 1997

1-Bit D/A Converter For Audio Application

Features

- Two-Channel D/A Converter and Oversampling Digital Filter Into a Single Chip
- Distortion . . . . . 0.012% or Less
- S/N Ratio . . . . . 96dB or More
- Master Clock. . . . . $384F_S$ or $256F_S$

Applications

- CD Player and CD-ROM Player, etc.

Functions

- Data Can Be Input at Rate of 1 x F_S with a Built-In Digital Filter
- The 24-/32-Slot Serial Data Interface Enables Independent Selection of Data Frontward Truncation/Rearward Truncation and MSB First/LSB First
- Two Channels Can Be Attenuated Independently in 255 Steps
- The Output From Two Channels (L/R/L + R/Mute) Can Be Selected Independently
- Digital Emphasis

Description

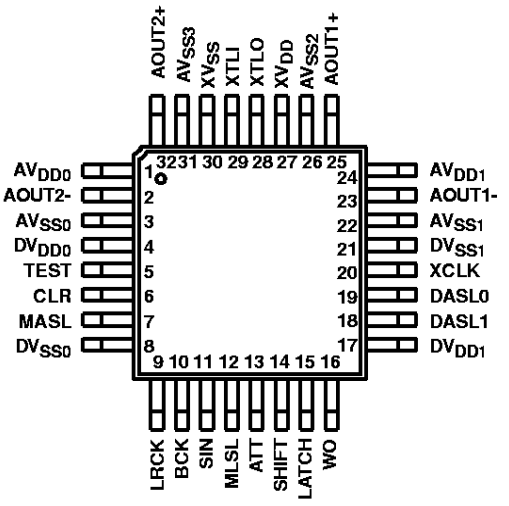
The HI2559, CXD2559 is a 1-bit stereo D/A converter featuring a 2nd-order $\Delta\Sigma$ system noise shaper. This good cost performance LSI has functions such as digital attenuator and digital de-emphasis and others.

Ordering Information

PART NUMBER	TEMP. RANGE (^oC)	PACKAGE	PKG. NO.
HI2559JCQ	-20 to 75	32 Ld MPQF	Q32.7x7-S
CXD2559Q	-20 to 75	32 Ld MPQF	Q32.7x7-S

Pinout

HI2559, CXD2559
(MQFP)
TOP VIEW



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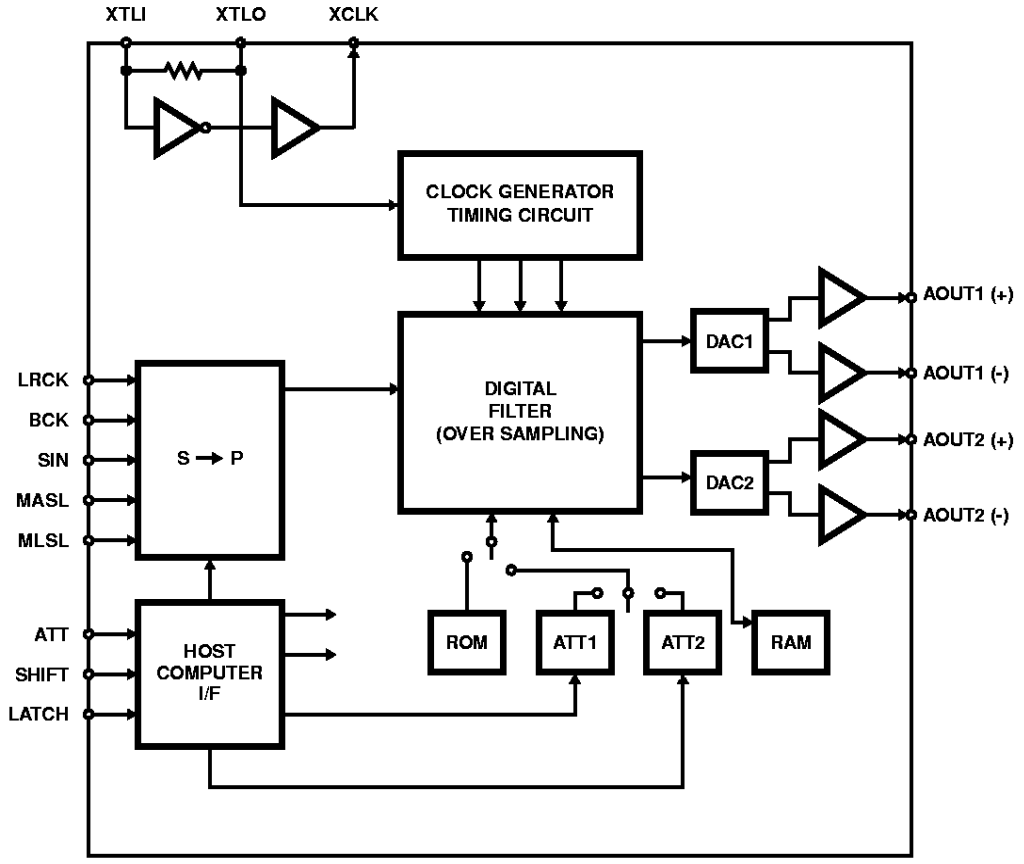
Block Diagram



Pin Descriptions

PIN NO.	SYMBOL	I/O	DESCRIPTION
1	AV_{DD0}	-	Analog power supply for Channel 2 output.
2	AOUT2(–)	O	Analog reversed phase output for Channel 2.
3	ADV_{SS0}	-	Analog GND for Channel 2 output.
4	DV_{DD0}	-	Digital power supply.
5	TEST	I	IC measurement. Fixed to Low.
6	CLR	I	System clear input. Cleared when low. Equipped with a pull-up resistor.
7	MASL	I	Selects whether 16-bit serial data is placed in the first 16-bit or the second 16-bit slot of the serial IN 32-bit slots. Frontward truncation when High; rearward truncation when low. Equipped with a pulldown resistor.
8	DV_{SS0}	-	Digital GND.
9	LRCK	I	Serial IN sampling frequency clock. Transfers Channel-1 data when High; Channel-2 data when low.
10	BCK	I	Serial bit transfer clock 48 F_S or 64 F_S in serial IN. The serial input data is retrieved at the rising edge.
11	SIN	I	Two channels per sampling serial data input. Data format is represented by 2's complements, and consists of 24-bit or 32-bit slots.
12	MLSL	I	Selects whether 16-bit serial data SIN (Pin 15) of serial IN at LSB first or MSB first. MSB-first when High; LSB-first when Low. Equipped with a pull-up resistor.

Pin Descriptions (Continued)

PIN NO.	SYMBOL	I/O	DESCRIPTION
13	ATT	I	Data input of the microcomputer interface. Attenuation data, output selection setting value, and de-emphasis on/off data re-input in serial mode.
14	SHIFT	I	Shift clock input of the microcomputer interface.
15	LATCH	I	Latch input of the microcomputer interface. Latched at the rising edge.
16	WO	I	Synchronization window control. Window open when Low (forced synchronization).
17	DV_{DD1}	-	Digital power supply.
18	DASL1	I	IC measurement. Fixed to Low.
19	DASL0	I	IC measurement. Fixed High.
20	XCLK	O	Inversion output of the clock input from XTLI (Pin 1).
21	DV_{SS1}	-	Digital GND.
22	AV_{SS1}	-	Analog GND for Channel 1 output.
23	AOUT1 (-)	O	Analog reversed phase output for Channel 1.
24	AV_{DD1}	I	Analog power supply for Channel 1 output.
25	AOUT1 (+)	O	Analog positive phase output for Channel 1.
26	AV_{SS2}	-	Analog GND for Channel 1 output.
27	XV_{DD}	-	Digital power supply for the master clock.
28	XTLO	O	Crystal oscillator output. Connects the master clock 256 F_S or 384 F_S crystal oscillator, which is identified automatically.
29	XTLI	I	Crystal oscillator input. Connects the master clock 256 F_S or 384 F_S crystal oscillator, which is identified automatically. External clock pulse is input at this pin.
30	XV_{SS}	-	Digital GND for master clock
31	AV_{SS3}	-	Analog GND for Channel 2 output.
32	AOUT2 (+)	O	Analog positive phase output for Channel 2.

Absolute Maximum Ratings $T_A = 25^oC$, $V_{SS} = 0V$

Supply Voltage (V_{DD}) . . . . . V_{SS} -0.5V to 7.0V
Input Voltage (V_I) . . . . . V_{SS} -0.5V to V_{DD} +0.5V
Output Voltage (V_0) . . . . . V_{SS}- 0.5V to V_{DD} +0.5V
Operating Temperature (TOPR) . . . . . -20°C to 75°C
Storage Temperature (T_{STG}) . . . . . -55°C to 150°C

Operating Conditions

Supply Voltage (V_{DD}) . . . . . 4.5V to 5.5V
Operating Temperature (T_A) . . . . . 20°C to 75°C
Sampling Frequency (F_S) . . . . . 7kHz to 50kHz

Input/Output Capacitance

Input Pin (C_{IN}) . . . . . 9pF (Max.)
Output Pin (C_{OUT}) . . . . . 11pF (Max.)
Measurement conditions: $V_{DD} = V_I = 0V$, f = 1MHz

Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS	APPLICABLE PIN
DC Electrical Specifications							
Input Voltage	V_{IH}		0.7 V_{DD}	-	-	V	Note 1
	V_{IL}		-	-	0.3 V_{DD}		
	V_{IH}		2.2	-	-	V	Note 2
	V_{IL}						
Output Voltage	V_{OH}	I_{OH} = -2mA	V_{DD} -0.8	-	0.4	V	Note 3
	V_{OL}	I_{OL} = 4mA	-	-	0.4		
	V_{OH}	I_{OH} = -1mA	V_{DD} /2	-	-	V	Note 4
	V_{OL}	I_{OL} = 1mA	-	-	V_{DD} /2		
	V_{OH}	I_{OH} = -4mA	V_{DD} -0.8	-	-	V	Note 5
	V_{OL}	I_{OL} = 4mA	0	-	-		
Input Leakage Current 1	I_{IL1}	$V_{IN} = V_{SS}$ or V_{DD}	-10	-	10	µA	Note 6
Input Leakage Current 2	I_{IL2}	$V_{IN} = V_{SS}$ or V_{DD}	-40	-	40	µA	Note 7
Input Leakage Current 3	I_{IL}	$V_{IL} = V_{SS}$	-40	-100	-240	µA	Note 8
Input Leakage Current 4	I_{IH}	$V_{IH} = V_{DD}$	40	100	240	µA	Note 9
Feedback Resistance	R_{FB}	$V_{IN} = V_{SS}$ or V_{DD}	250k	1M	2.5M	Ω	Note 12

NOTES:

1. Input pins except for *2t
2. ATT, SHIFT, LATCH
3. XCLK
4. XLO
5. AOUT1 (+), AOUT1 (-), AOUT2 (+), AOUT2 (-)
6. ATT, SHIFT, LATCH, LRCK, BCK, SINt
7. WO
8. CLR, MLSLt
9. MASL
10. XTLI

AC Electrical Specifications $V_{DD} = 5.0 \pm 10\%$, TOPR = -20°C to 75°C

PARAMETER		SYMBOL						
Oscillation Frequency	256 F_S	fx		2	-	13	MHz	
	384 F_S			2	-	20		
External Clock Pulse Input High Level Width	258 F_S	t_{CWH}		38	-	250	ns	
	384 F_S			25	-	250	ns	

AC Electrical Specifications V_{DD} = 5.0 ±10%, TOPR = -20°C to 75°C

PARAMETER		SYMBOL						
External Clock Pulse Input Low Level Width	256 F_S	t_{CWL}		38	-	250	ns	
	384 F_S			25	-	250	ns	
External Clock Pulse Input Pulse Cycle (Note 2)	256 F_S	t_{CYC}		76	-	500	ns	
	384 F_S			50	-	500	ns	
Input BCK Frequency		f_{BCK}		-	-	3.1	MHz	
Input BCK Pulse Width		t_{WIB}		100	-	-	ns	
Input Data Setup Time		t_{IDS}		10	-	-	ns	
Input Data Hold Time		t_{IDH}		15	-	-	ns	
Input LRCK Setup Time		t_{ILRS}		10	-	-	ns	
Input LRCK Hold Time		t_{ILRH}		15	-	-	ns	
Program Input Basic Time		t_{PR}		100	-	-	ns	
Latch Input Pulse Width		t_{WLT}		200	-	-	ns	
ATT Setup Time		t_{SET}		5	-	-	ns	
ATT Hold Time		t_{HOLD}		100	-	-	ns	
ATT Interval		t_{INT}		300	-	-	ns	

NOTE:

11. Always input an external clock after turning the power on.

ANALOG CHARACTERISTICS						
MEASUREMENT CONDITIONS	T_A = 25°C, V_{DD} = 5.0V, F_S = 44kHz, signal frequency = 1kHz, measurement band = 4Hz to 20kHz, Master Clock 384F_S.					
S/N		(EIAJ) *1	96	100	-	dB
THD + N		(EIAJ)	-	0.010	0.012	%
Dynamic Range		(EIAJ) *1, *2	91	93	-	dB
Channel Separation		(EIAJ)	-	90	-	dB
Output Level			-	2.58	-	V (ms)
Gain Difference Between Channels			-	-	0.1	dB

NOTES:

12. A-weighting filter used.

13. -60dB, 1kHz input.

The analog characteristics are measured with the following circuit:

Test Circuits

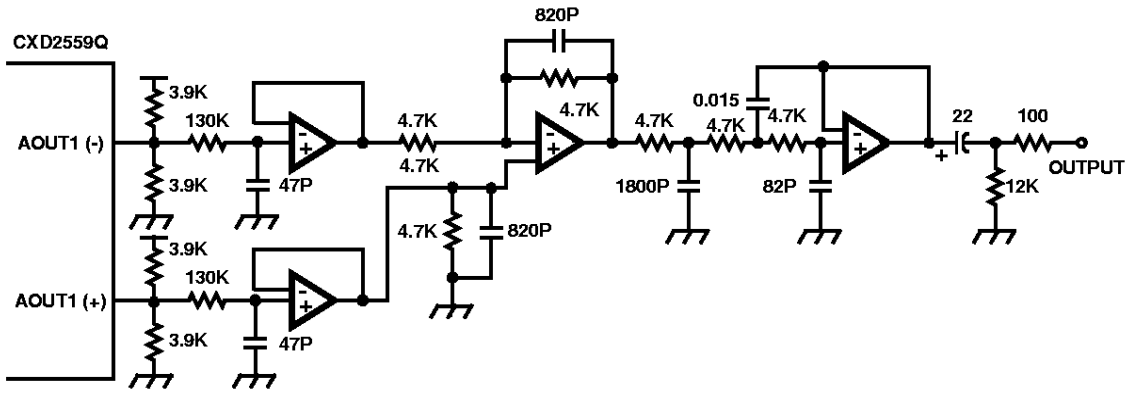


FIGURE 1. ANALOG CHARACTERISTICS

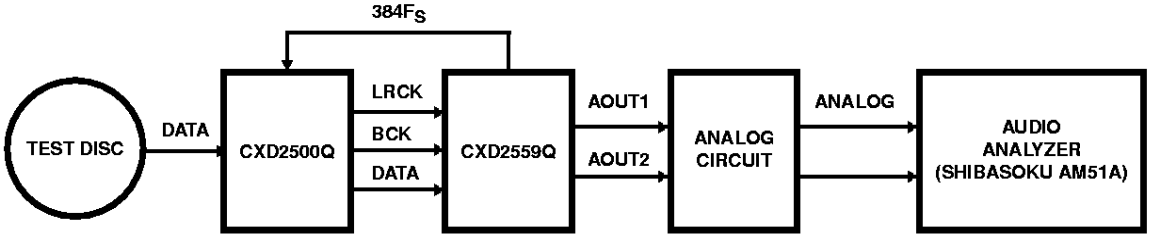


FIGURE 2.

Timing Diagrams

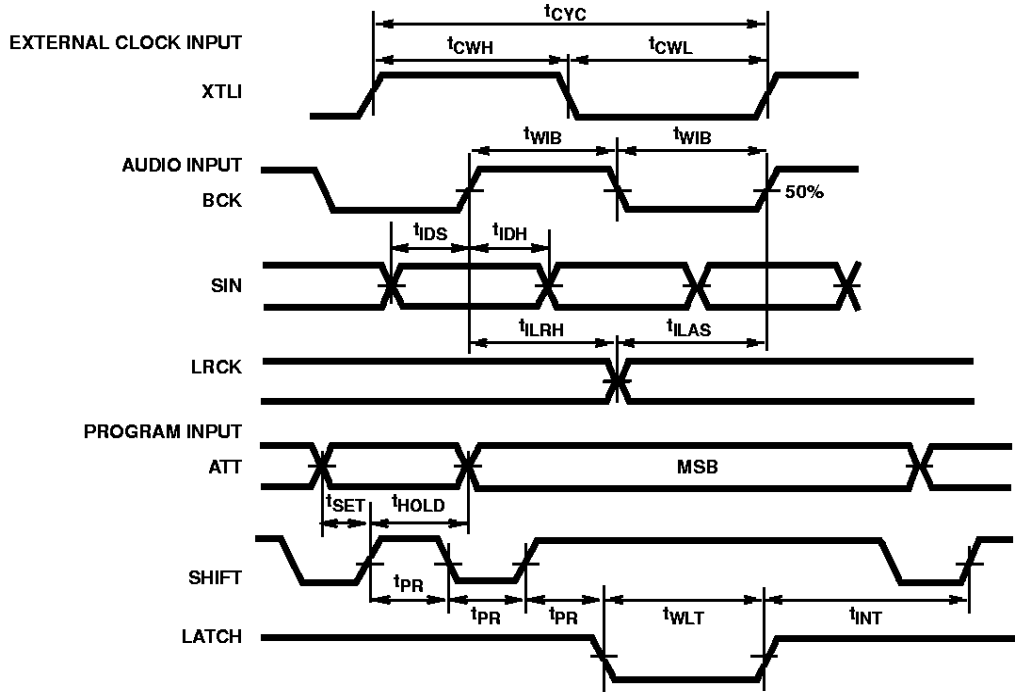


FIGURE 3. TIMING CHART

Timing Diagrams (Continued)

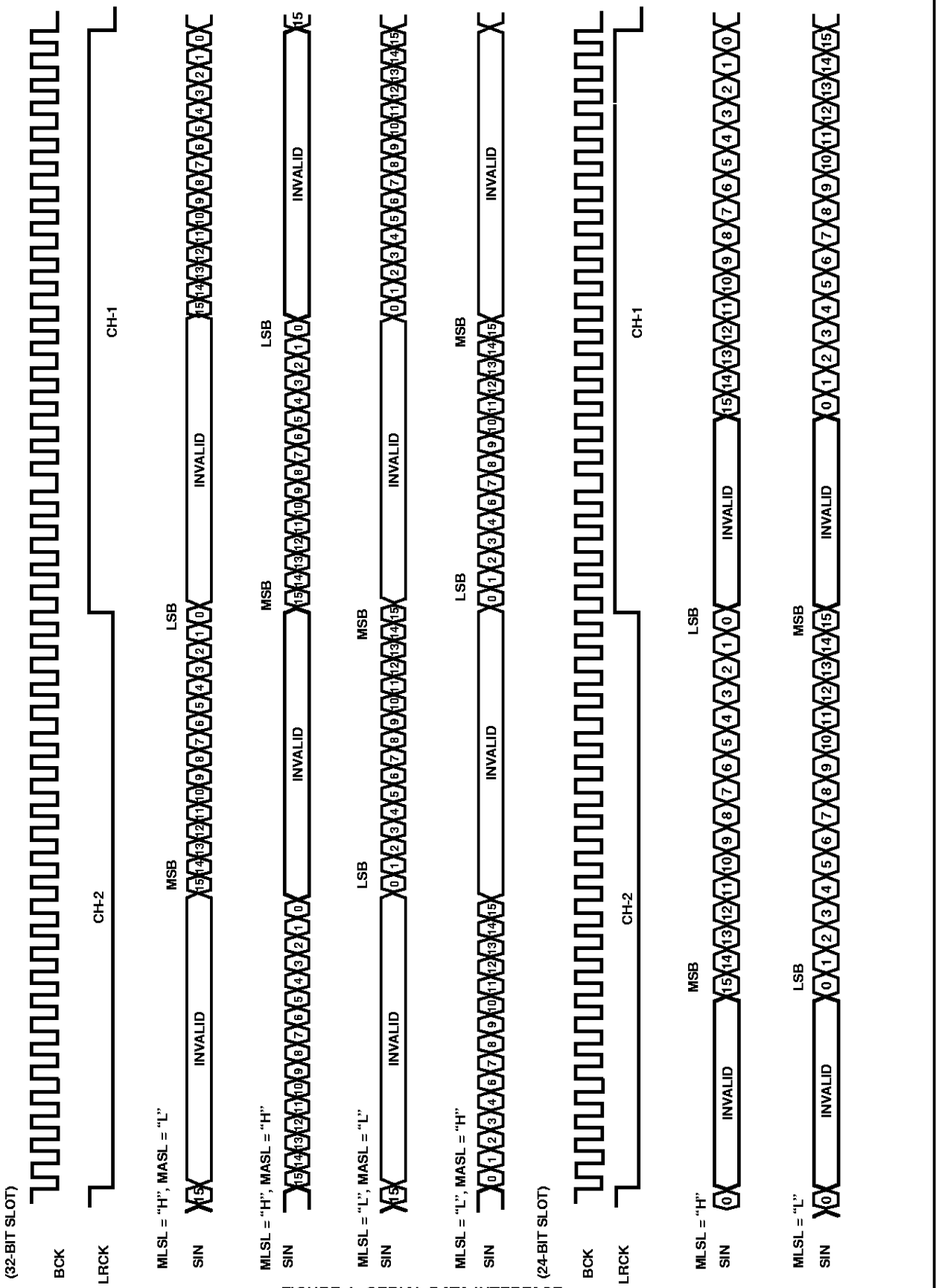


FIGURE 4. SERIAL DATA INTERFACE

Timing Diagrams (Continued)

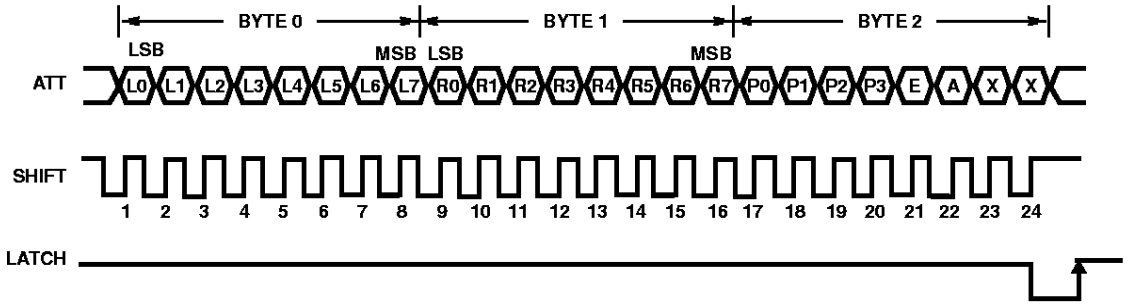


FIGURE 5.

Description of Functions

A. Crystal Oscillator Frequency Selection

[Related pins] XTLI, XTLO, XCLK, BCK, SIN

Although the 384 F_S or 256 V_S crystal oscillator can be connected to XTLI and XTLO, the selection is determined depending on whether the input serial data is 24-bit or 32-bit slot. The frequency of the crystal oscillator is output from XCLK as it is.

SERIAL DATA INPUT BIT RATE	CRYSTAL OSCILLATOR FREQUENCY	XCLK OUTPUT
24-Bit Slot (48F_S)	384F_S	384F_S
32-Bit Slot (64F_S)	256F_S	256F_S

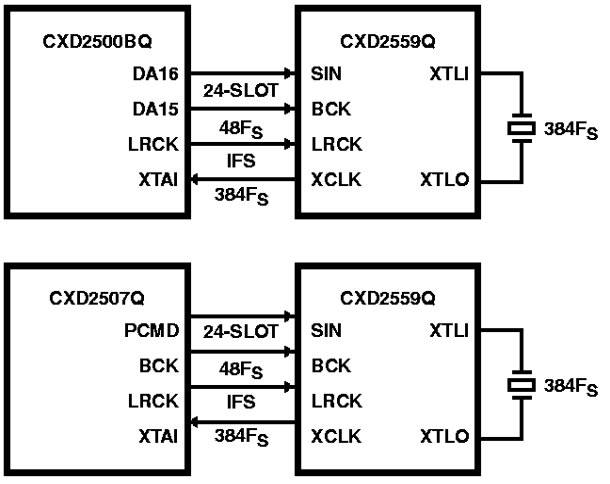


FIGURE 6. CONNECTION EXAMPLE FOR THE CD DSP

B. Serial Data Interface

[Related pins] LRCK, BCK, SIN, MASL, MLSL

The serial data format consists of two channels per sampling serial data represented by 2's complement. In each channel, the data is processed as a 24-bit slot when the crystal oscillator frequency is 384 F_S, and as a 32-bit slot when the crystal oscillator frequency is 256 F_S. 16 of these bits are used as data.

MSL is used to select whether the serial data is arranged at LSB first or MSB first. Also, MASL is used to select whether the 16-bits of valid data is placed in the first or the second half of the 32-bit slot.

MSL	
H	MSB First
L	LSB First

MASL	24-BIT SLOT	32-BIT SLOT
H	Rearward Truncation	Frontward Truncation
L		Rearward Truncation

C. Control Mode

[Related pins] ATT, SHIFT, LATCH

The serial ports of ATT, SHIFT and LATCH are used to control functions such as the digital attenuator, output selection and digital de-emphasis.

Data consists of 24-bits (3 bytes), which have the following meanings:

CONTROL BIT	CONTROL	WHEN SYSTEM IS CLEARED
L7 TO L0	The L channel attenuation data.	FF (H)
R7 to R0	The R channel attenuation data.	FF (H)
P3 to P0	Output selection.	9 (H) Stereo
E	De-emphasis (High = on, Low = off) However, the time constant of the emphasis is γ 1 = 50μs and γ 2 = 15μs when F_S = 44.1kHz. The de-emphasis function cannot be used when F_S is not 44.1kHz.	OFF
A	Attenuate (Low = independent, High = common). However, the L channel attenuation value is used when the L and R channels are commonly attenuated.	Independent
X	Don't care.	

NOTE: When the data is more than three bytes are transferred to the ATT pin, only the three bytes transferred finally are effective.

D. Digital Attenuator

[Related pins] ATT, SHIFT, LATCH

The output data can be attenuated independently in the L and R channels, using the transfer data from the external microcomputer.

The ATT data of the L and R channels consist of eight bits each, and the L and R channels can be attenuated commonly using the ATT control bit. (The L channel attenuation value is used when the L and R channels are commonly attenuated).

(1) Command and Audio Output

The attenuation data of the L and R channels consist of eight bits, it can be set 255 ways. The following table shows the relationship between the commands and the outputs.

ATTENUATION DATA L7 TO L0/R7 TO R0	AUDIO OUTPUT
FF (H)	0dB
FE (H) ↓ 01 (H)	-0.034dB ↓ -48.131dB
00 (H)	- ∞

The attenuation values for 01 (H) to FE (H) can be obtained with the following equation:

ATT = 20log [Input data/255] dB

Ex. for attenuating data FA (H)

ATT = 20log [250/255] db = 0.172dB

E. Digital Attenuator

Suppose that there are attenuation data ATT1, ATT2 and ATT3, and their relationship is ATT1>ATT3>ATT2. When ATT2 is transferred before the level reaches the value of ATT1 (point A in the figure), the level keeps approaching to the value of ATT2. Next, when ATT3 is transferred before the level reaches the value of ATT2 (point B or C in the figure), the level starts approaching to the value of ATT3 from its level at that time (point B or C in the figure). The transition (0 dB to $\rightarrow -\infty$) between the attenuation data is $1024/F_S$ (F_S = 44kHz for CD).

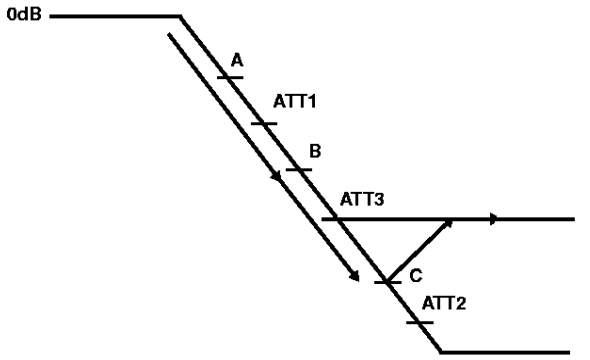


FIGURE 7. METHOD OF OBTAINING AN ATTENUATION VALUE

F. Output Selection

[Related pins] ATT, SHIFT, LATCH

The L and R channel outputs can be set in four combinations [L/RL + R/Mute] (16 ways in total) using the transfer data from the external microcomputer. The following table shows the relationship between the commands and the outputs.

P0	P1	P2	P3	L CHANNEL OUTPUT	R CHANNEL OUTPUT	REMARKS
0	0	0	0	Mute	Mute	Mute
0	0	0	1	Mute	R	
0	0	1	0	Mute	L	
0	0	1	1	Mute	L + R	
0	1	0	0	R	Mute	
0	1	0	1	R	R	
0	1	1	0	R	L	Reverse
0	1	1	1	R	L + R	
1	0	0	0	L	Mute	
1	0	0	1	L	R	Stereo
1	0	1	0	L	L	
1	-	1	1	L	L + R	
1	1	0	0	L + R	Mute	
1	1	0	1	L + R	R	
1	1	1	0	L + R	L	
1	1	1	1	L + R	L + R	Mono

NOTE: For L + R, the output data is (L + R)/2 to avoid overflow.

G. I/O Sync Circuit

[Related pins] LRCK and WO

(1) Operation (When the WO Pin is "H")

The synchronization circuit has the window of eight clocks of the master clock and it monitors whether the rising edge of LRCK is in the window.

If the rising edge of LRCK is out of the window, resynchronization is automatically performed.

(2) Forced Synchronization by WO Pin

Even if the rising edge of LRCK is within the window, it may not synchronize owing to the mixing of the external noises, etc. when the rising edge of LRCK is positioned near at both edges of the window.

When the power is turned on, it is necessary to set the rising edge of LRCK in the center of the window by performing the forced synchronization.

After the system is cleared, the forced synchronization is performed by setting WO pin to Low at $2/F_S$ or more. The forced synchronization is performed at the second rising edge of LRCK after the WO pin is turned to "Low."

NOTE: WO pin must be "H" except the forced synchronization.

H. System Clear When the Power is Turned ON.

[Related Pins] CLR

When the power is turned ON and the master clock more than 4 clocks is input to the XTLI pin, set the CLR pin from "L" to "H."