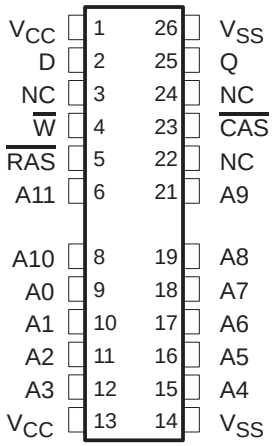
This data sheet is applicable to all TMS416100/Ps symbolized with Revision "B" and subsequent revisions as described on page 24.

- **Organization . . . 16 777 216 × 1**
- **Single 5-V Power Supply (±10% Tolerance)**
- **Performance Ranges:**

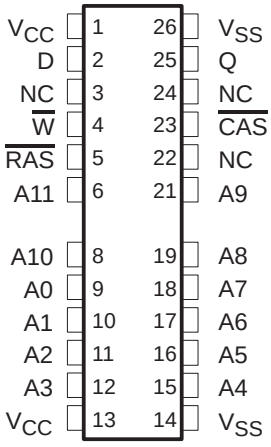
	ACCESS TIME t_{RAC} (MAX)	ACCESS TIME t_{CAC} (MAX)	ACCESS TIME t_{AA} (MAX)	READ OR WRITE CYCLE (MIN)
'416100-60	60 ns	15 ns	30 ns	110 ns
'416100-70	70 ns	18 ns	35 ns	130 ns
'416100-80	80 ns	20 ns	40 ns	150 ns

- **Enhanced Page Mode Operation for Faster Memory Access**
- **$\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ Refresh**
- **Long Refresh Period**
  - **4096 Cycle Refresh in 64 ms (TMS416100)**
  - **256 ms for Extended Refresh Version (TMS416100P)**
- **3-State Unlatched Output**
- **Low Power Dissipation (TMS416100P Only)**
  - **500-µA CMOS Standby Current**
  - **500-µA Self-Refresh Current**
  - **500-µA Extended Refresh Battery Backup Current**
- **All Inputs, Outputs and Clocks Are TTL Compatible**
- **Operating Free-Air Temperature Range: 0°C to 70°C**

DJ PACKAGE (TOP VIEW)



DGA PACKAGE (TOP VIEW)



PIN NOMENCLATURE

A0–A11	Address Inputs
$\overline{\text{CAS}}$	Column-Address Strobe
D	Data In
Q	Data Out
NC	No Internal Connection
$\overline{\text{RAS}}$	Row-Address Strobe
V_{CC}	5-V Supply
V_{SS}	Ground
$\overline{\text{W}}$	Write Enable

description

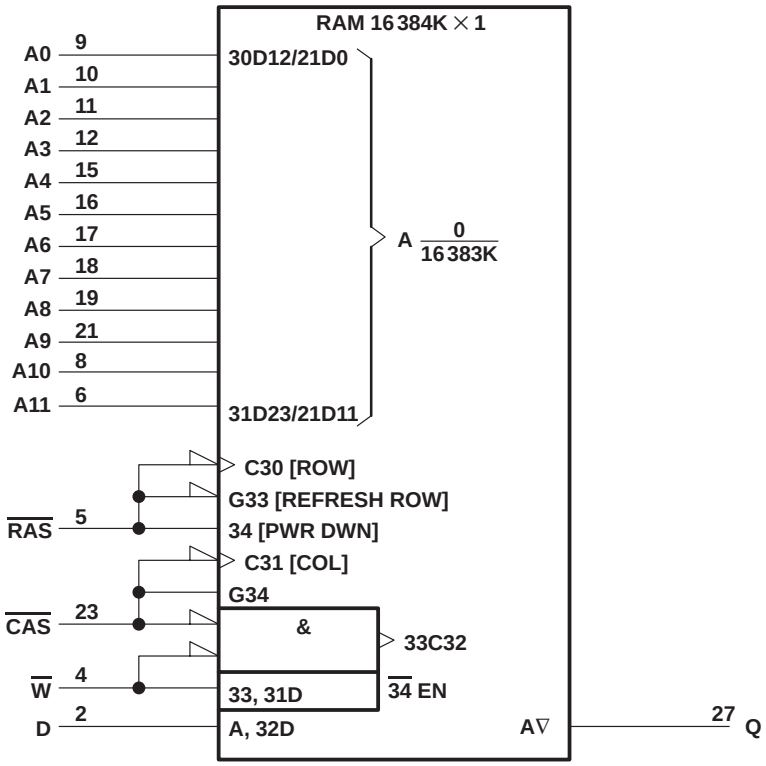
The TMS416100/P series are high-speed, 16777216-bit dynamic random-access memories, organized as 16777216 words of one bit each. The TMS416100P series feature self refresh and extended refresh. They employ state-of-the-art EPIC™ (Enhanced Performance Implanted CMOS) technology for high performance, reliability, and low power at a low cost.

These devices feature maximum $\overline{\text{RAS}}$ access times of 60 ns, 70 ns, and 80 ns. All inputs, outputs, and clocks are compatible with Series 74 TTL. All addresses and data-in lines are latched on chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The TMS416100/P are offered in 300-mil 24/26-lead plastic surface-mount SOJ packages (DJ suffix) and 24/26-lead plastic small-outline packages (DGA suffix). All packages are characterized for operation from 0°C to 70°C.

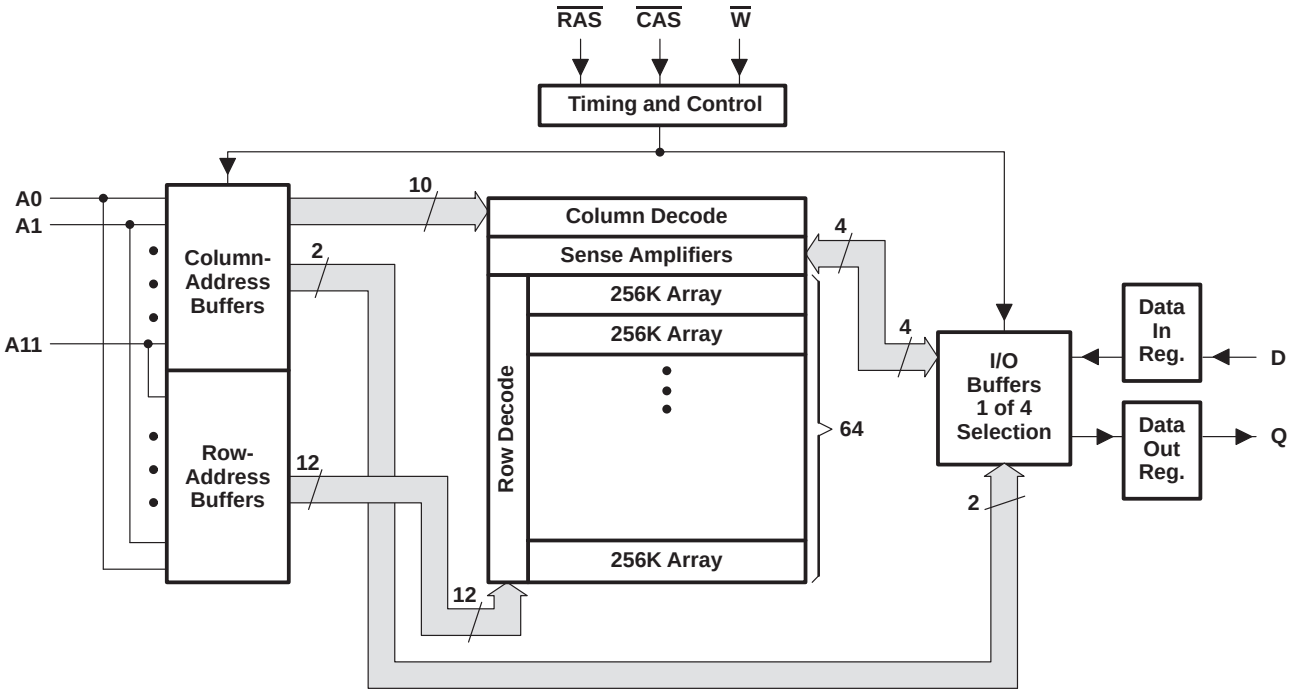
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DJ and DGA packages.

functional block diagram



operation

enhanced page mode

Enhanced page-mode operation allows faster memory access by keeping the same row address while selecting random column addresses. The time for row-address setup and hold and address multiplex is thus eliminated. The maximum number of columns that can be accessed is determined by t_{RASP}, the maximum $\overline{RAS}$-low time.

Unlike conventional page-mode DRAMs, the column-address buffers in this device are activated on the falling edge of $\overline{RAS}$. The buffers act as transparent or flow-through latches while $\overline{CAS}$ is high. The falling edge of $\overline{CAS}$ latches the addresses and enables the output. This feature allows the TMS416100/P to operate at a higher data bandwidth than conventional page-mode parts because retrieval begins as soon as the column address is valid rather than when $\overline{CAS}$ transitions low. This performance improvement is referred to as *enhanced page mode*. Valid column address can be presented immediately after row-address hold time has been satisfied, usually well in advance of the falling edge of $\overline{CAS}$. In this case, data is obtained after t_{CAC} max (access time from $\overline{CAS}$ low), if t_{AA} max (access time from column address) and t_{RAC} have been satisfied. In the event that the column address for the next cycle is valid at the time $\overline{CAS}$ goes high, access time for the next cycle is determined by the later occurrence of t_{CPA} or t_{CAC}.

address (A0 – A11)

Twenty-four address bits are required to decode 1 of 16 777 216 storage cell locations. Twelve row-address bits are set up on inputs A0 through A11 and latched during a normal access and during $\overline{RAS}$-only refresh as the device requires 4096 refresh cycles. Twelve column-address bits are set up on inputs A0 – A11 and latched onto the chip by $\overline{CAS}$. All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select, activating the output buffer as well as latching the address bits into the column-address buffer.

write enable ($\overline{W}$)

The read or write mode is selected through the write-enable ($\overline{W}$) input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pullup resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$ (early write), data out remains in the high-impedance state for the entire cycle, permitting common I/O operation.

data in (D)

Data is written during a write or read-modify-write cycle. Depending on the mode of operation, the falling edge of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latch. In an early-write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed-write or read-modify-write cycle, $\overline{CAS}$ is already low and the data is strobed in by $\overline{W}$ with setup and hold times referenced to this signal.

data out (Q)

The 3-state output buffer provides direct TTL compatibility (no pullup resistor required) with a fanout of two Series 74 TTL loads. The output is in the high-impedance (floating) state until $\overline{CAS}$ is brought low. In a read cycle, the output becomes valid at the latest occurrence of t_{RAC}, t_{AA}, t_{CAC}, or t_{CPA} and remains valid while $\overline{CAS}$ is low. $\overline{CAS}$ going high returns it to the high-impedance state.

refresh

A refresh operation must be performed at least once every 64 ms to retain data. This can be achieved by strobing each of the 4096 rows (A0–A11). A normal read or write cycle refreshes all bits in each row that is selected. A $\overline{RAS}$-only operation can be used by holding $\overline{CAS}$ at the high (inactive) level, conserving power as the output buffer remains in the high-impedance state. Externally generated addresses must be used for a $\overline{RAS}$-only refresh. Hidden refresh can be performed by holding $\overline{CAS}$ at V_{IL} after a read operation and cycling $\overline{RAS}$ after a specified precharge period, similar to a $\overline{RAS}$-only refresh cycle except with $\overline{CAS}$ held low. Valid data is maintained at the output throughout the hidden refresh cycle. An internal address provides the refresh address during hidden refresh.

$\overline{CAS}$-before-$\overline{RAS}$ refresh

$\overline{CAS}$-before-$\overline{RAS}$ (CBR) refresh is utilized by bringing $\overline{CAS}$ low earlier than $\overline{RAS}$ (see parameter t_{CSR}) and holding it low after $\overline{RAS}$ falls (see parameter t_{CHR}). For successive $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles, $\overline{CAS}$ remains low while cycling $\overline{RAS}$. For this mode of refresh, the external addresses are ignored and the refresh address is generated internally.

A low-power battery-backup refresh mode that requires less than 500 μA refresh current is available on the TMS416100P. Data integrity is maintained using $\overline{CAS}$-before-$\overline{RAS}$ refresh with a period of 62.5 μs while holding $\overline{RAS}$ low for less than 1 μs. To minimize current consumption, all input levels need to be at CMOS levels ($V_{IL} \leq 0.2$ V, $V_{IH} \leq V_{CC} - 0.2$ V).

power up

To achieve proper device operation, an initial pause of 200 μs followed by a minimum of eight initialization cycles is required after full V_{CC} level is achieved. These eight initialization cycles need to include at least one refresh ($\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$) cycle.

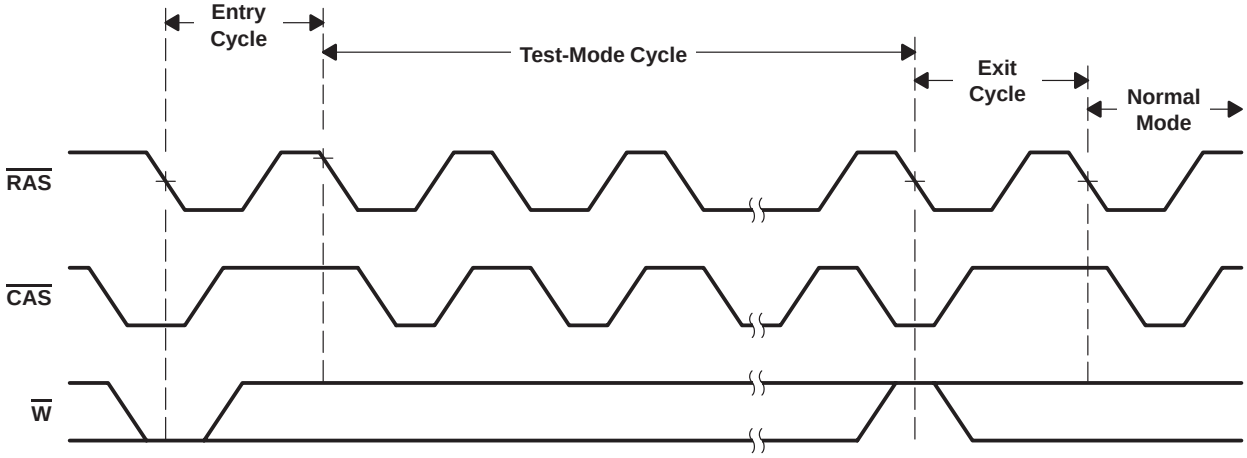
self refresh (TMS416100P)

The self-refresh mode is entered by dropping $\overline{CAS}$ low prior to $\overline{RAS}$ going low. $\overline{CAS}$ and $\overline{RAS}$ are both held low for a minimum of 100 µs. The chip is then refreshed by an on-board oscillator. No external address is required because the CBR counter is used to keep track of the address. To exit the self-refresh mode, both $\overline{RAS}$ and $\overline{CAS}$ are brought high to satisfy t_{CHS}. Upon exiting the self-refresh mode, a burst refresh (refresh a full set of row addresses) must be executed before continuing with normal operation. This ensures the DRAM is fully refreshed.

test mode

The test mode is initiated with a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle while simultaneously holding the $\overline{W}$ input low (WCBR). The entry cycle performs an internal refresh cycle while internally setting the device to perform parallel read or write on subsequent cycles. While in the test mode, any data sequence can be performed. The device exits the test mode if a $\overline{CAS}$-before-$\overline{RAS}$ (CBR) refresh cycle with $\overline{W}$ held high or a $\overline{RAS}$-only refresh (ROR) cycle is performed.

The device is configured as 1024K × 16 bits with a 16-bit parallel read-and-write data path in the test mode. Column addresses A0, A1, A10, and A11 are not used. During a read cycle, all 16 bits of the internal data bus are compared. If all bits are in the same data state, the output pin goes high. If one or more bits disagree, the output pin goes low. Test time is reduced by a factor of 16, compared to normal memory mode.



NOTE: The states of $\overline{W}$, data input, and address are defined by the type of cycle used during test mode.

Figure 1. Test-Mode Cycle

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . – 1 V to 7 V
Input voltage range (see Note 1) . . . . . – 1 V to 7 V
Short-circuit output current . . . . . 50 mA
Power dissipation . . . . . 1 W
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range . . . . . – 55°C to 125°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	–1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		'416100-60 '416100P-60		'416100-70 '416100P-70		'416100-80 '416100P-80		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA		2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA			0.4		0.4		0.4	V
I_I	Input current (leakage)†	V_I = 0 V to 6.5 V, All other pins = 0 V to V_{CC}			± 10		± 10		± 10	µA
I_O	Output current (leakage)†	V_O = 0 V to V_{CC}, $\overline{CAS}$ high			± 10		± 10		± 10	µA
I_{CC1}	Read- or write-cycle current (see Notes 3 and 5)	V_{CC} = 5.5 V, Minimum cycle			80		70		60	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.4 V (TTL)			2		2		2	mA
		After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, $V_{IH} = V_{CC}$ – 0.2 V (CMOS)	'416100		1		1		1	mA
			'416100P		500		500		500	µA
I_{CC3}	Average refresh current ($\overline{RAS}$-only or CBR) (see Notes 3 and 5)†	$\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$-only); $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)			80		70		60	mA
I_{CC4}	Average page current (see Notes 4 and 5)†	$\overline{RAS}$ low, $\overline{CAS}$ cycling			70		60		50	mA
I_{CC6}	Self-refresh current ('416100P only)	$\overline{CAS}$ and $\overline{RAS}$ < 0.2 V, Measured after t_{RASS} min			500		500		500	µA
I_{CC7}	Standby current, output enable (see Note 5)†	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL}, Data out = enabled			5		5		5	mA
I_{CC10}	Extended-refresh battery backup ('416100P only)	t_{RC} = 62.5 µs, t_{RAS} ≤ 1 µs, V_{CC} – 0.2 V ≤ V_{IH} ≤ 6.5 V, 0 V ≤ V_{IL} ≤ 0.2 V, $\overline{W}$ and $\overline{OE}$ = V_{IH}, Address and data stable			500		500		500	µA

† Minimum cycle, V_{CC} = 5.5 V

NOTES: 3. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}
4. Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}
5. Measured with no load connected

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 6)

PARAMETER		MIN	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs		5	pF
$C_{i(D)}$	Input capacitance, data inputs		5	pF
$C_{i(RC)}$	Input capacitance, strobe inputs		7	pF
$C_{i(W)}$	Input capacitance, write-enable input		7	pF
C_o	Output capacitance		7	pF

NOTE 6: V_{CC} = 5 V ± 0.5 V, and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		’416100-60 ’416100P-60		’416100-70 ’416100P-70		’416100-80 ’416100P-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{AA}	Access time from column address		30		35		40	ns
t_{CAC}	Access time from $\overline{CAS}$ low		15		18		20	ns
t_{CPA}	Access time from column precharge		35		40		45	ns
t_{RAC}	Access time from $\overline{RAS}$ low		60		70		80	ns
t_{CLZ}	$\overline{CAS}$ to output in low-impedance state	0		0		0		ns
t_{OH}	Output disable time, start of $\overline{CAS}$ high	3		3		3		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (see Note 7)	0	15	0	18	0	20	ns

NOTE 7: t_{OFF} is specified when the output is no longer driven.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		’416100-60 ’416100P-60		’416100-70 ’416100P-70		’416100-80 ’416100P-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Cycle time, random read or write (see Note 8)	110		130		150		ns
t_{RWC}	Cycle time, read-write (see Note 8)	130		153		175		ns
t_{PC}	Cycle time, page-mode read or write (see Notes 8 and 9)	40		45		50		ns
t_{PRWC}	Cycle time, page-mode read-write (see Note 8)	60		68		75		ns
t_{RASP}	Pulse duration, page-mode, $\overline{RAS}$ low (see Note 10)	60	100 000	70	100 000	80	100 000	ns
t_{RAS}	Pulse duration, nonpage-mode, $\overline{RAS}$ low (see Note 10)	60	10 000	70	10 000	80	10 000	ns
t_{CAS}	Pulse duration, $\overline{CAS}$ low (see Note 11)	15	10 000	18	10 000	20	10 000	ns
t_{CP}	Pulse duration, $\overline{CAS}$ high	10		10		10		ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	40		50		60		ns
t_{WP}	Pulse duration, $\overline{W}$ low	10		10		10		ns
t_{ASC}	Setup time, column address before $\overline{CAS}$ low	0		0		0		ns
t_{ASR}	Setup time, row address before $\overline{RAS}$ low	0		0		0		ns
t_{DS}	Setup time, data (see Note 12)	0		0		0		ns
t_{RCS}	Setup time, $\overline{W}$ high before $\overline{CAS}$ low	0		0		0		ns
t_{CWL}	Setup time, $\overline{W}$ low before $\overline{CAS}$ high	15		18		20		ns
t_{RWL}	Setup time, $\overline{W}$ low before $\overline{RAS}$ high	15		18		20		ns
t_{WCS}	Setup time, $\overline{W}$ low before $\overline{CAS}$ low (early-write operation only)	0		0		0		ns
t_{WRP}	Setup time, $\overline{W}$ high before $\overline{RAS}$ low ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		ns
t_{WTS}	Setup time, $\overline{W}$ low before $\overline{RAS}$ low (test mode only)	10		10		10		ns
t_{CAH}	Hold time, column address after $\overline{CAS}$ low	10		15		15		ns
t_{DH}	Hold time, data (see Note 12)	10		15		15		ns
t_{RAH}	Hold time, row address after $\overline{RAS}$ low	10		10		10		ns
t_{RCH}	Hold time, $\overline{W}$ high after $\overline{CAS}$ high (see Note 13)	0		0		0		ns
t_{RRH}	Hold time, $\overline{W}$ high after $\overline{RAS}$ high (see Note 13)	0		0		0		ns
t_{WCH}	Hold time, $\overline{W}$ low after $\overline{CAS}$ low (early-write operation only)	10		15		15		ns
t_{WRH}	Hold time, $\overline{W}$ high after $\overline{RAS}$ low ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		ns
t_{WTH}	Hold time, $\overline{W}$ low after $\overline{RAS}$ low (test mode only)	10		10		10		ns
t_{RHCP}	Hold time, $\overline{RAS}$ high from $\overline{CAS}$ precharge	35		40		45		ns
t_{CHS}	Hold time, $\overline{CAS}$ low after $\overline{RAS}$ high (self refresh)	– 50		– 50		– 50		ns

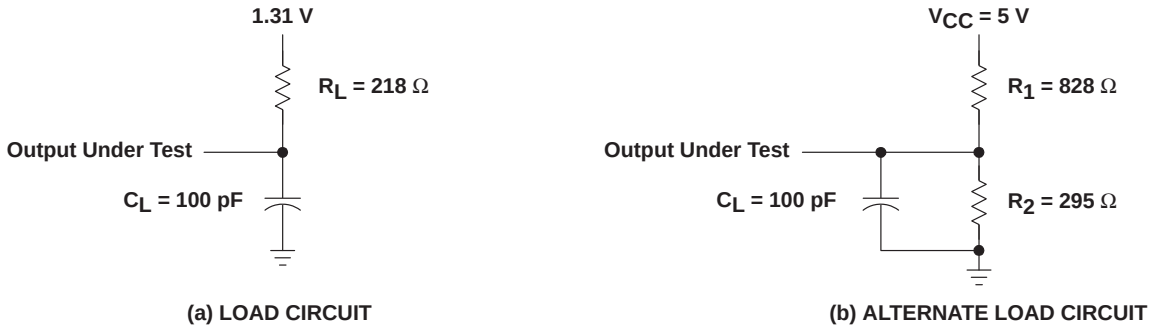
NOTES: 8. All cycle times assume t_T = 5 ns.
9. To assure t_{PC} min, t_{ASC} should be greater than or equal to t_{CP}.
10. In a read-write cycle, t_{RWD} and t_{RWL} must be observed.
11. In a read-write cycle, t_{CWD} and t_{CWL} must be observed.
12. Referenced to the later of $\overline{CAS}$ or $\overline{W}$ in write operations
13. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (continued)

			’416100-60 ’416100P-60		’416100-70 ’416100P-70		’416100-80 ’416100P-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{AWD}	Delay time, column address to $\overline{W}$ low (read-write operation only)		30		35		40		ns
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)		10		10		10		ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low		5		5		5		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high		60		70		80		ns
t_{CSR}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)		5		5		5		ns
t_{CWD}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (read-write operation only)		15		18		20		ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column address (see Note 14)		15	30	15	35	15	40	ns
t_{RAL}	Delay time, column address to $\overline{RAS}$ high		30		35		40		ns
t_{CAL}	Delay time, column address to $\overline{CAS}$ high		30		35		40		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 14)		20	45	20	52	20	60	ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low		0		0		0		ns
t_{RSH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high		15		18		20		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (read-write operation only)		60		70		80		ns
t_{CPW}	Delay time, $\overline{W}$ low after $\overline{CAS}$ precharge (read-write operation only)		35		40		45		ns
t_{RASS}	Pulse duration, self-refresh entry from $\overline{RAS}$ low		100		100		100		µs
t_{RPS}	Pulse duration, $\overline{RAS}$ precharge after self refresh		110		130		150		ns
t_{TAA}	Access time from address (test mode)		35		40		45		ns
t_{TCPA}	Access time from column precharge (test mode)		40		45		50		ns
t_{TRAC}	Access time from $\overline{RAS}$ (test mode)		65		75		85		ns
t_{REF}	Refresh time interval	’416100		64		64		64	ms
		’416100P		256		256		256	ms
t_T	Transition time		3	30	3	30	3	30	ns

NOTE 14: The maximum value is specified only to assure access time.

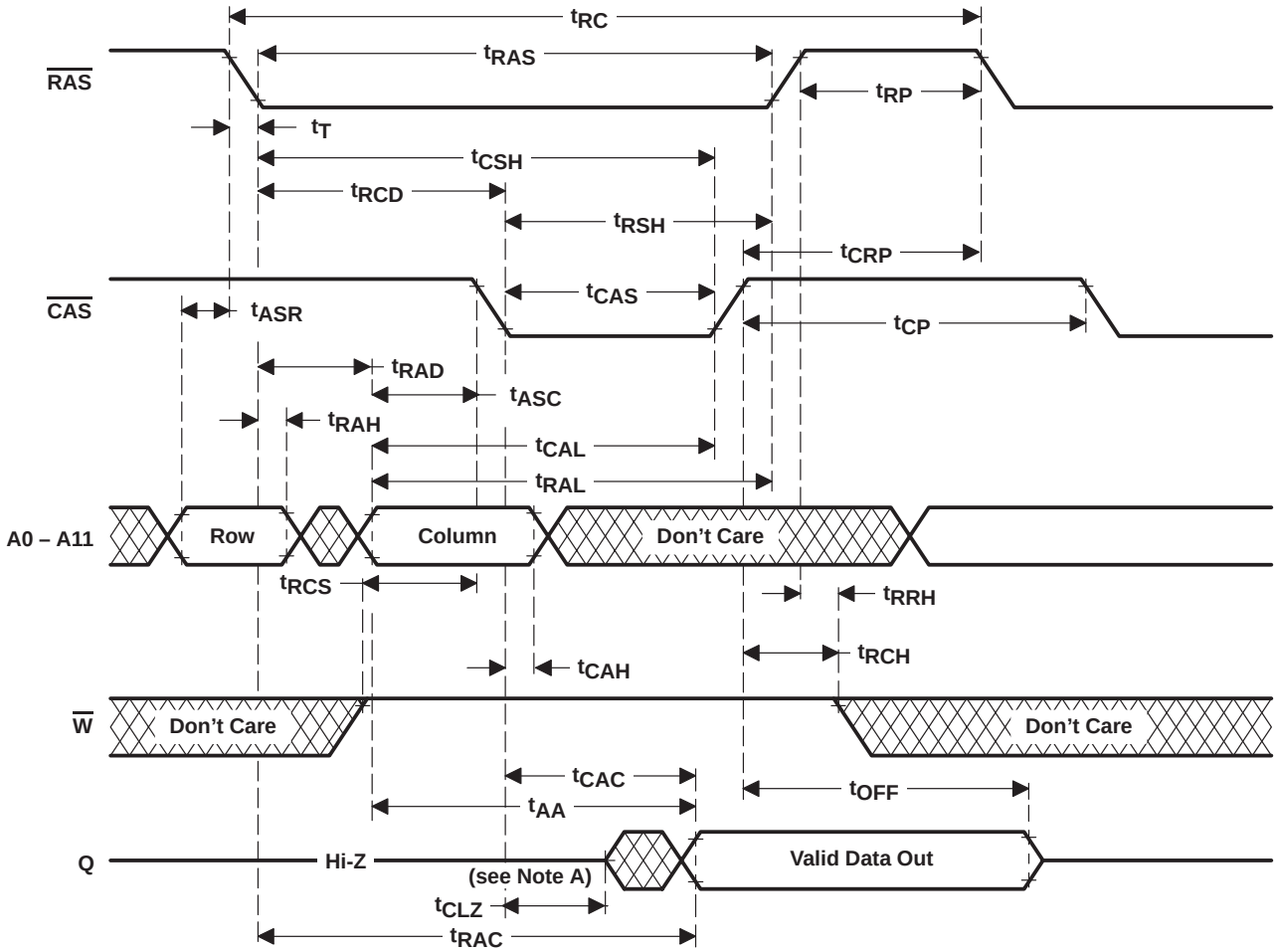
PARAMETER MEASUREMENT INFORMATION



(a) LOAD CIRCUIT **(b) ALTERNATE LOAD CIRCUIT**

Figure 2. Load Circuits

PARAMETER MEASUREMENT INFORMATION



NOTE A: Output can go from 3-state to an invalid data state prior to the specified access time.

Figure 3. Read-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

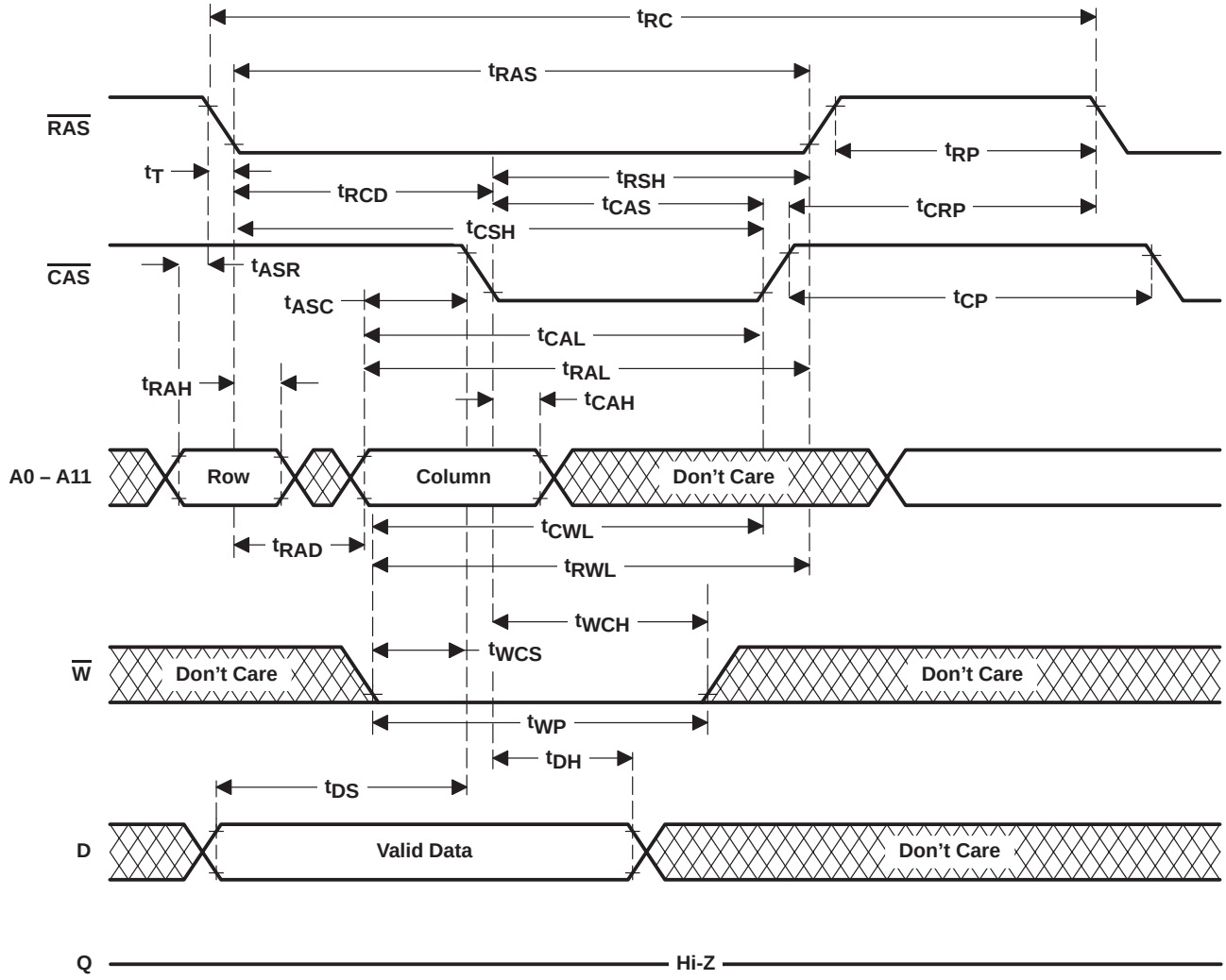


Figure 4. Early-Write-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

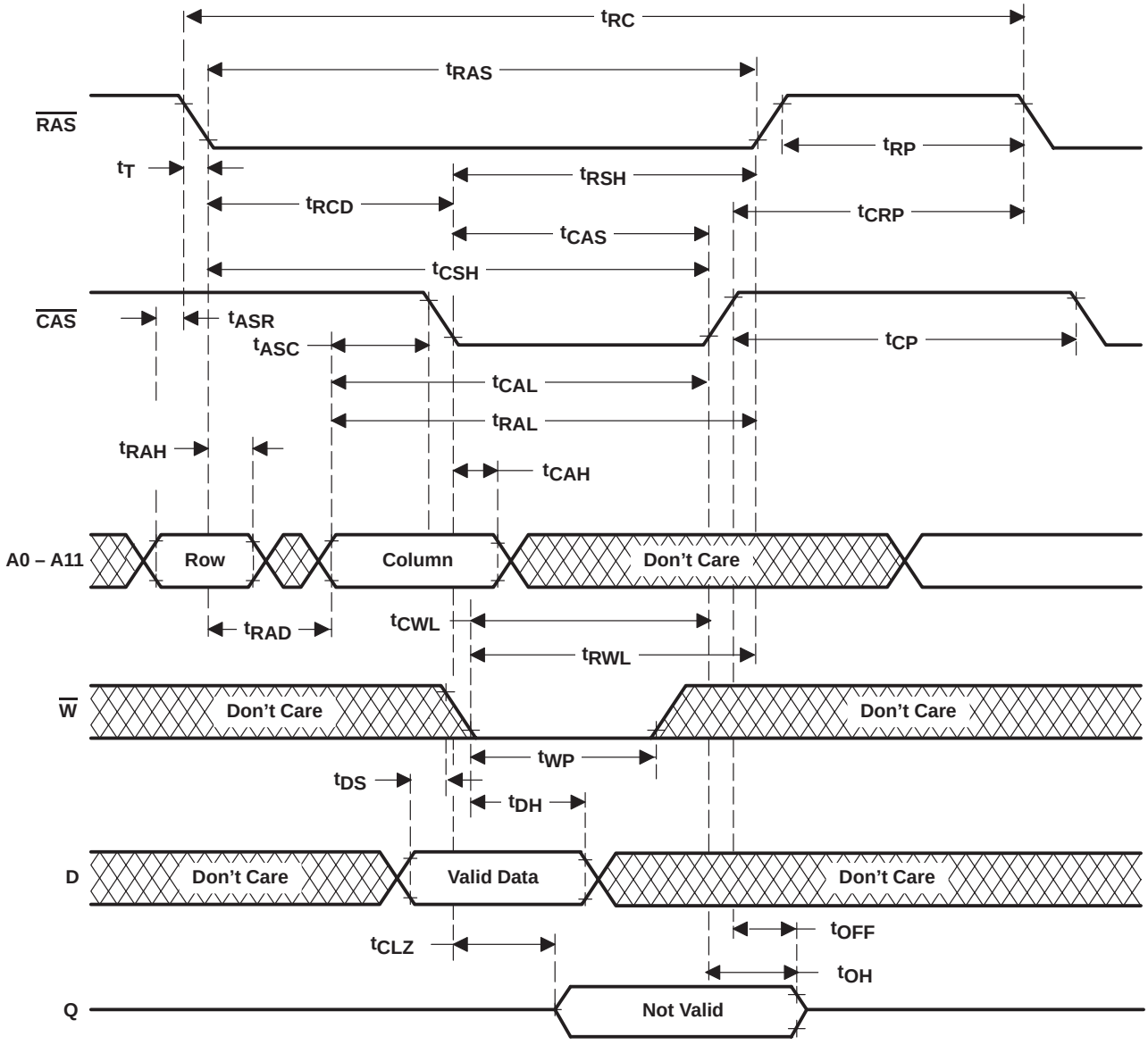
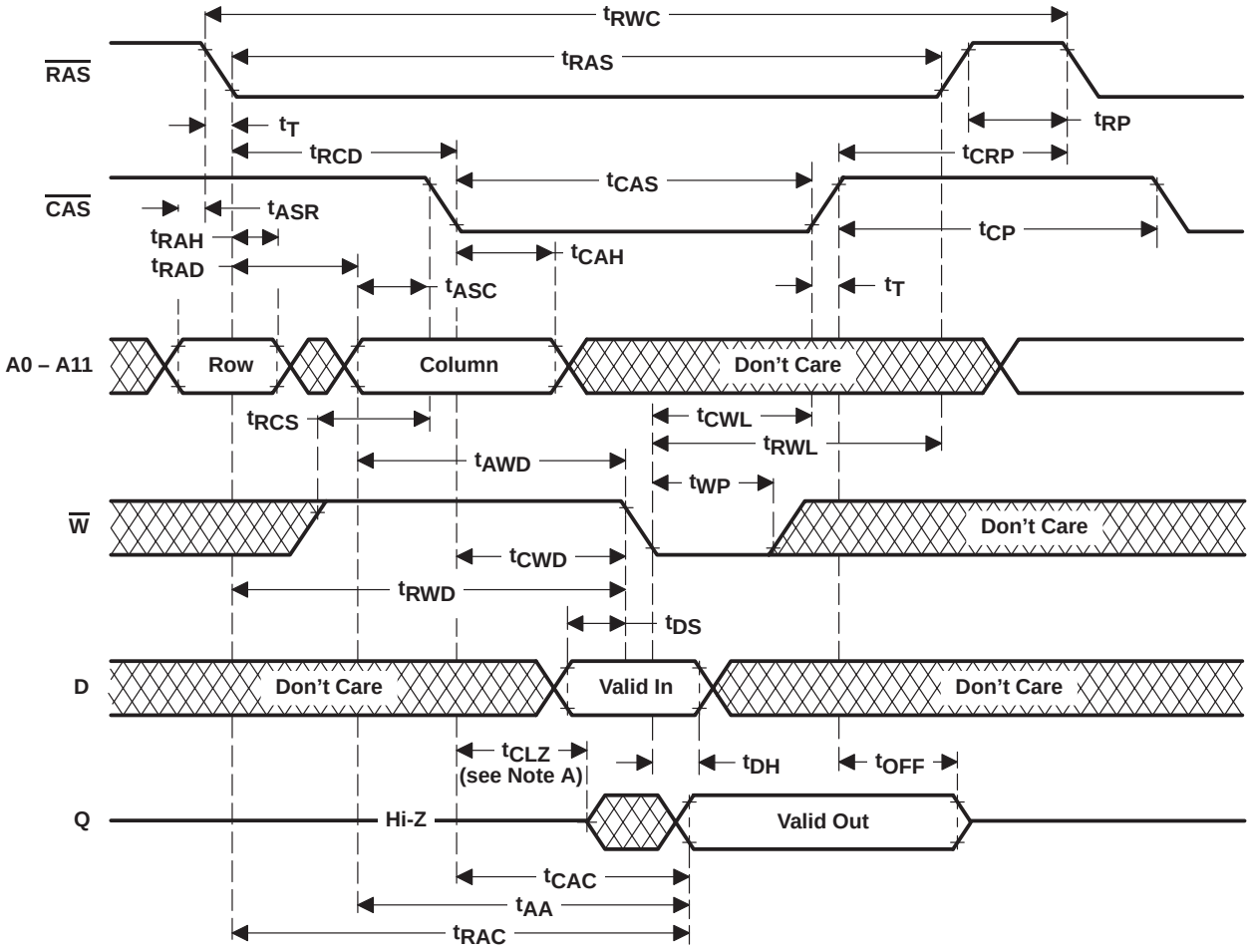


Figure 5. Write-Cycle Timing

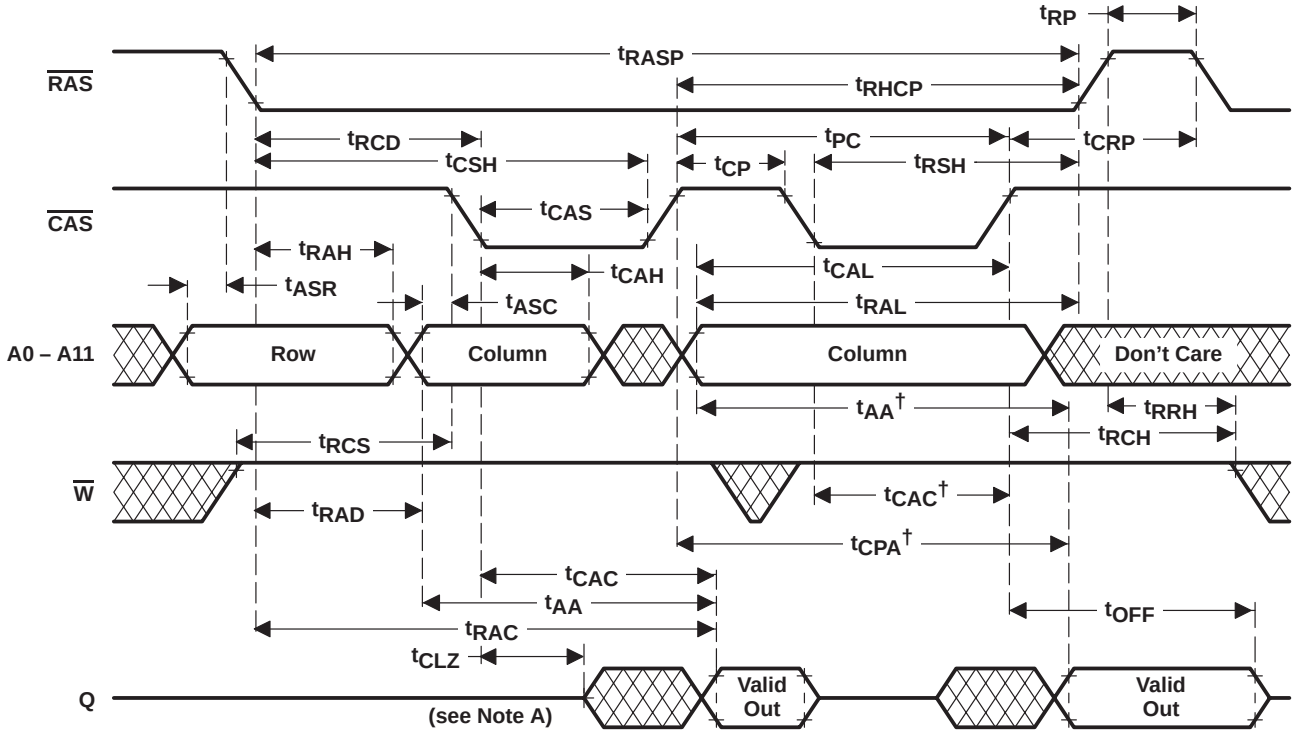
PARAMETER MEASUREMENT INFORMATION



NOTE A: Output can go from 3-state to an invalid data state prior to the specified access time.

Figure 6. Read-Write-Cycle Timing

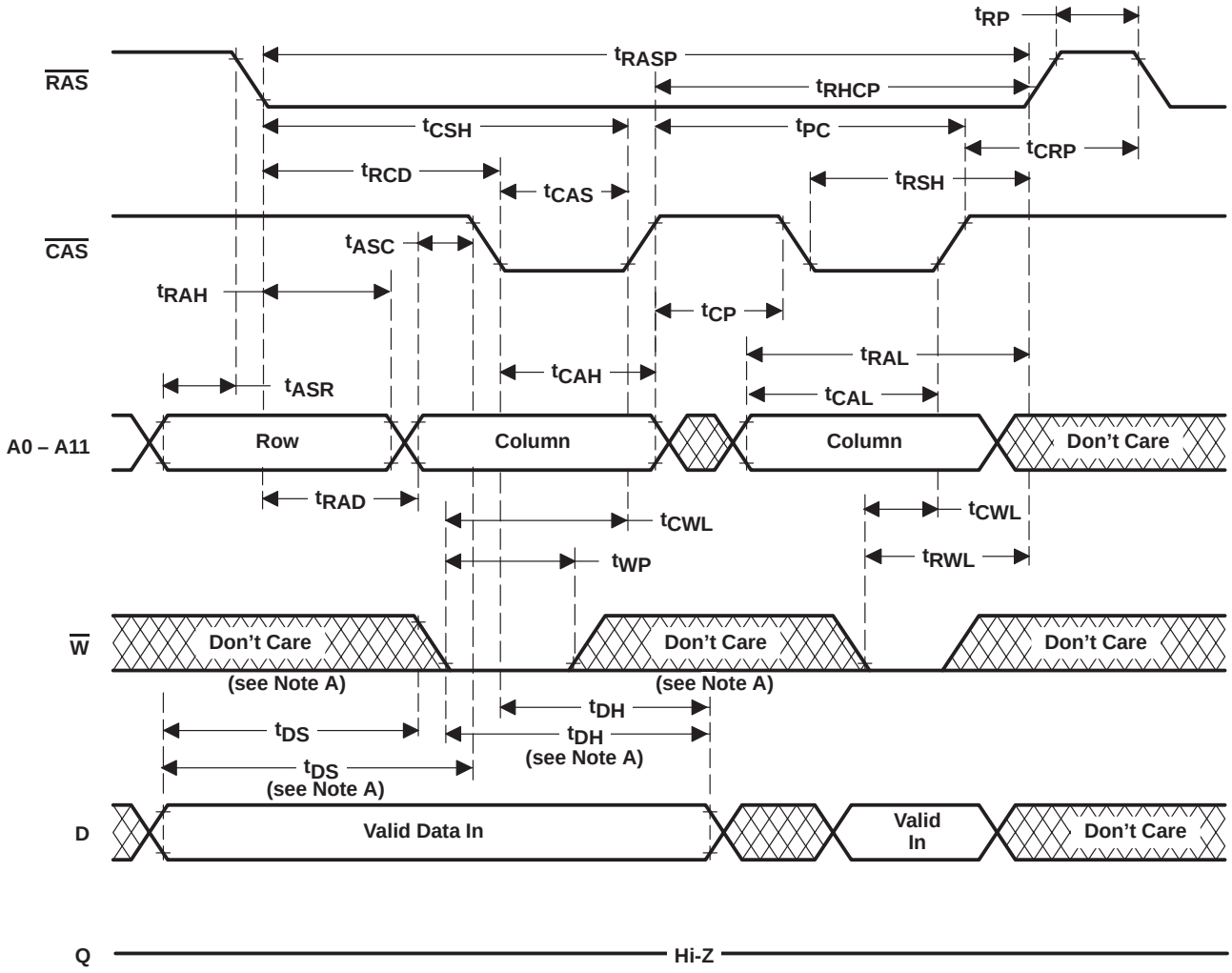
PARAMETER MEASUREMENT INFORMATION



† Access time is t_{CPA}, t_{CAC}, or t_{AA} dependent.
NOTE A: Output can go from 3-state to an invalid data state prior to the specified access time.

Figure 7. Enhanced-Page-Mode Read-Cycle Timing

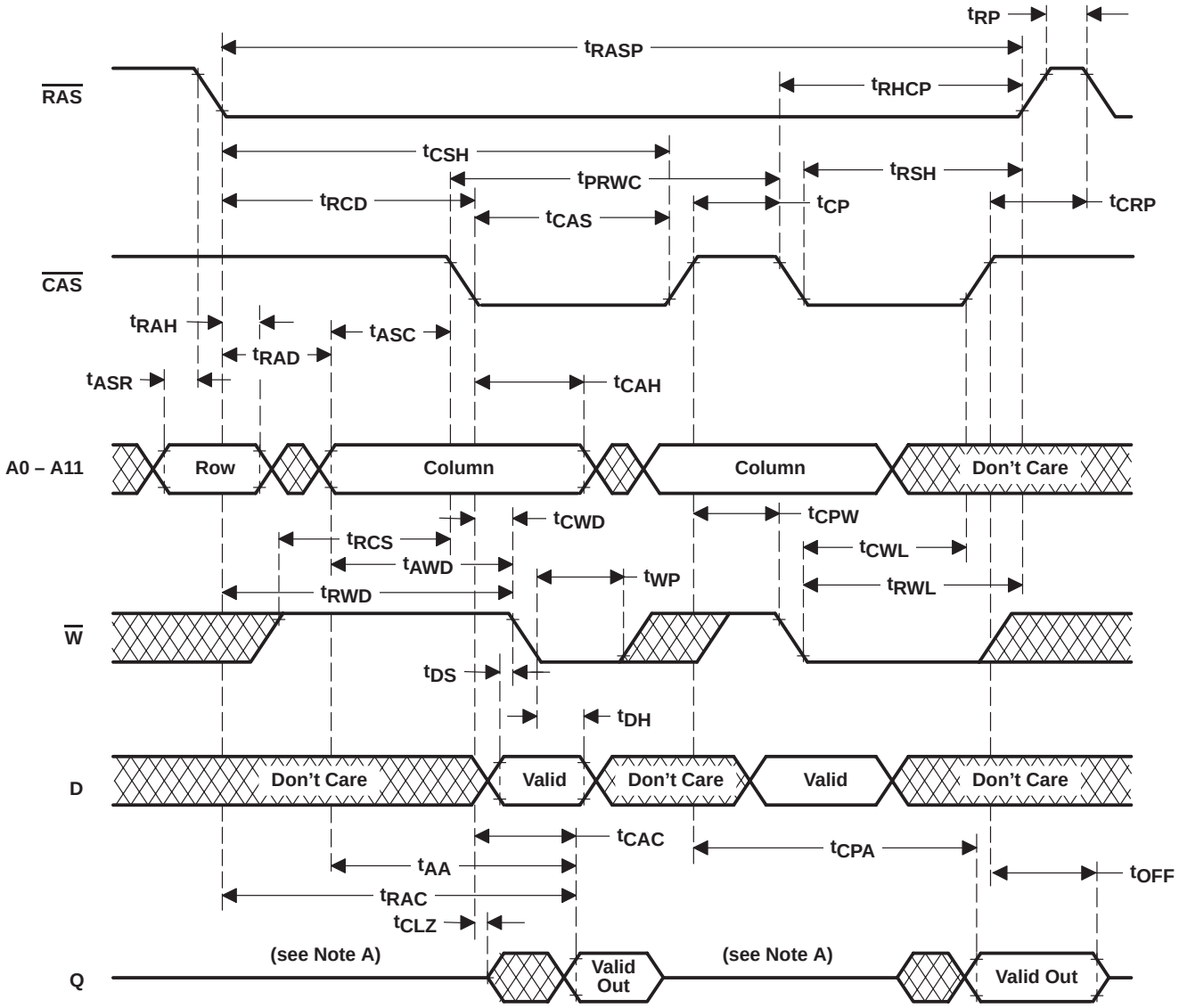
PARAMETER MEASUREMENT INFORMATION



NOTES: A. Referenced to $\overline{CAS}$ or $\overline{W}$, whichever occurs last
B. A read cycle or a read-write cycle can be intermixed with write cycles as long as read and read-write timing specifications are not violated.

Figure 8. Enhanced-Page-Mode Write-Cycle Timing

PARAMETER MEASUREMENT INFORMATION



NOTES: A. Output can go from 3-state to an invalid data state prior to the specified access time.
B. A read or write cycle can be intermixed with read-write cycles as long as the read and write timing specifications are not violated.

Figure 9. Enhanced-Page-Mode Read-Write-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

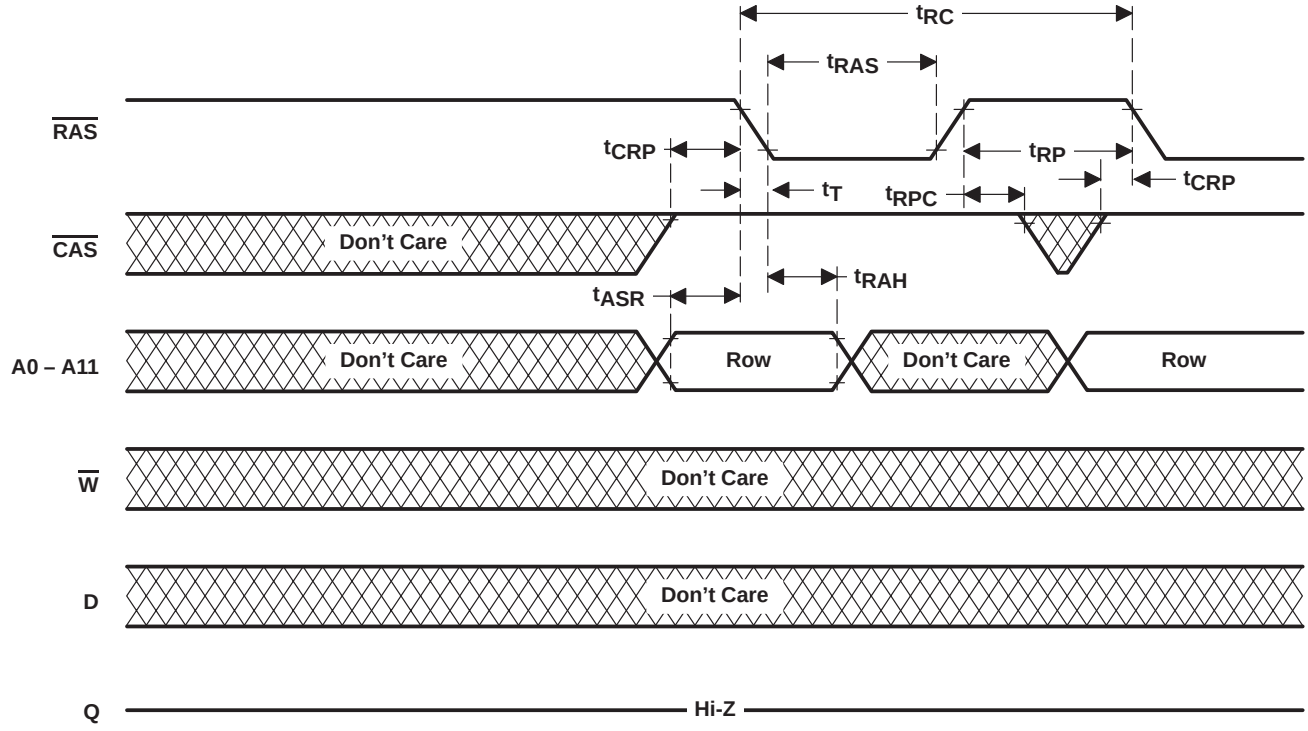


Figure 10. $\overline{\text{RAS}}$-Only-Refresh-Cycle Timing

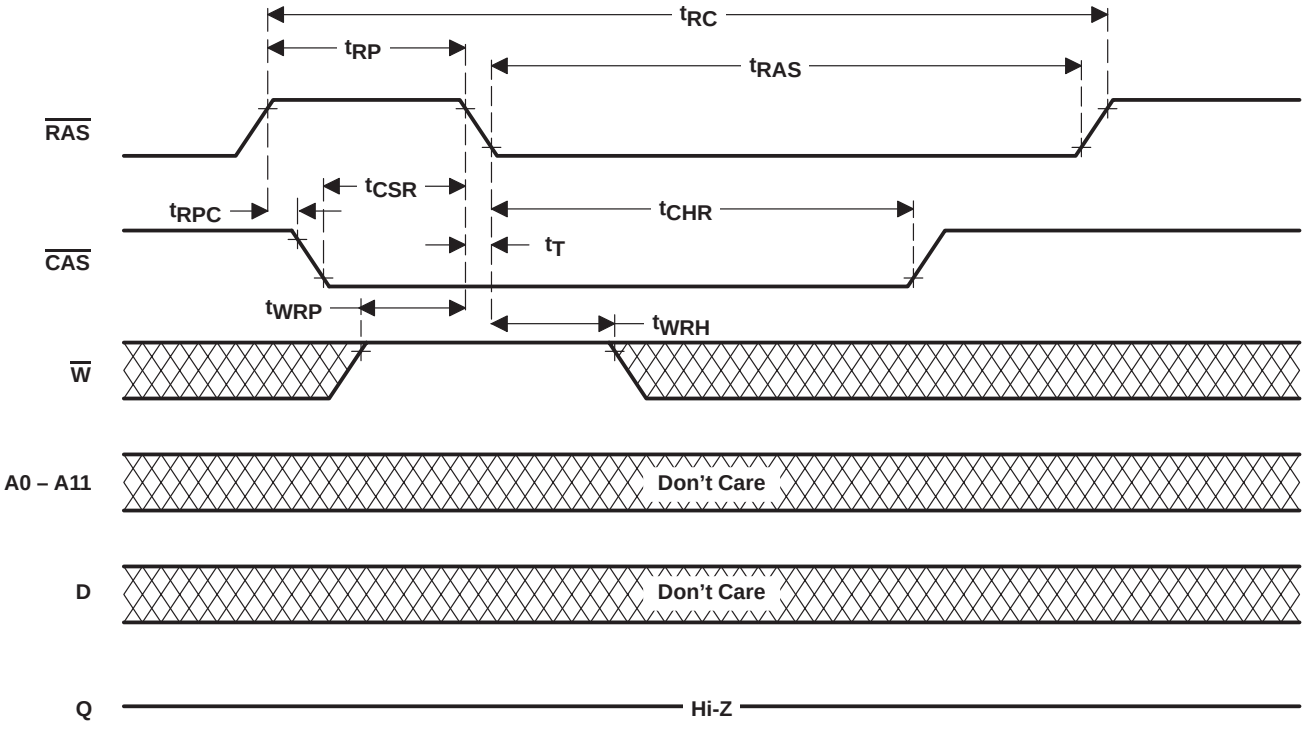


Figure 11. Automatic ($\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$) Refresh-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

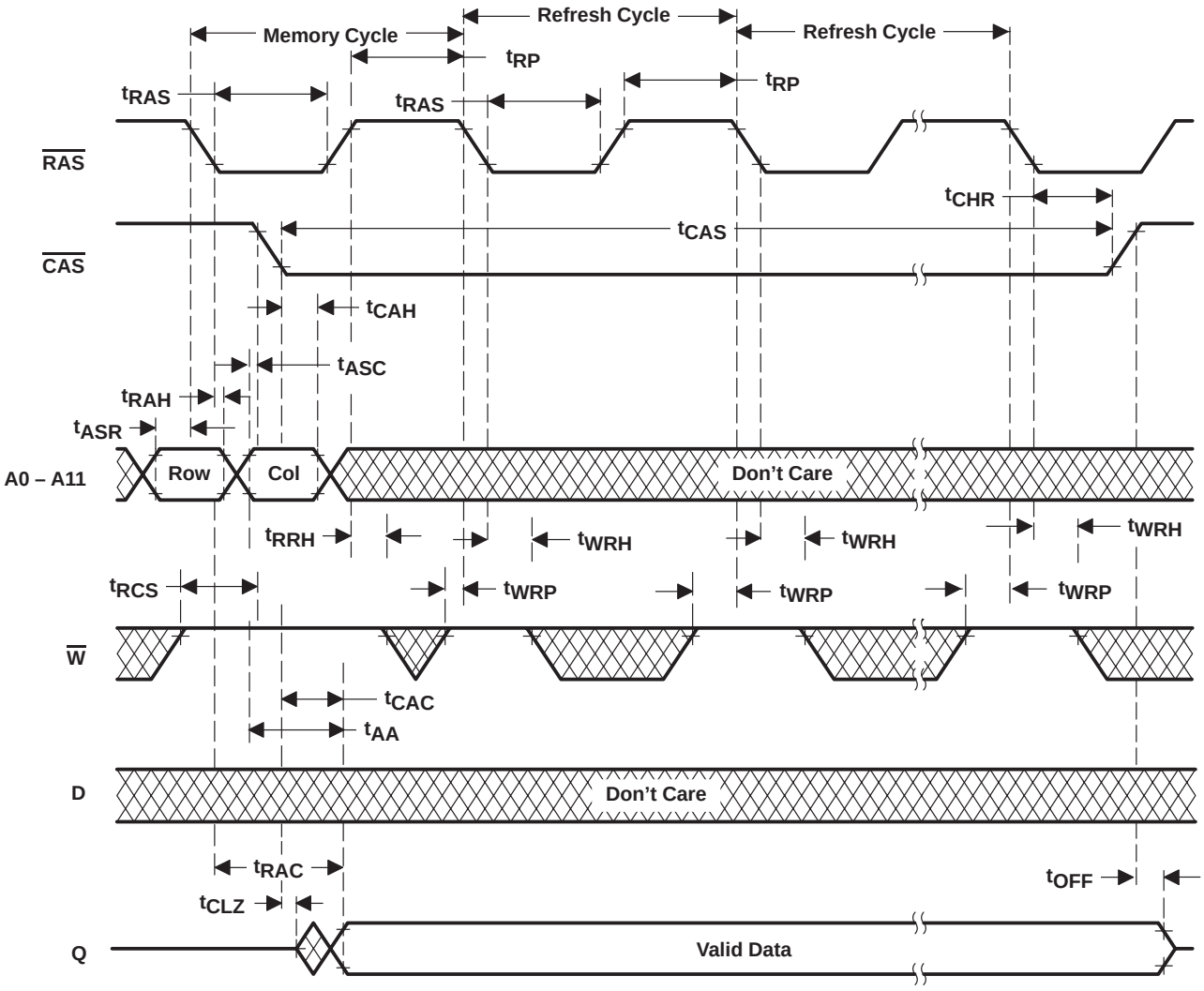


Figure 12. Hidden-Refresh-Cycle (Read) Timing

PARAMETER MEASUREMENT INFORMATION

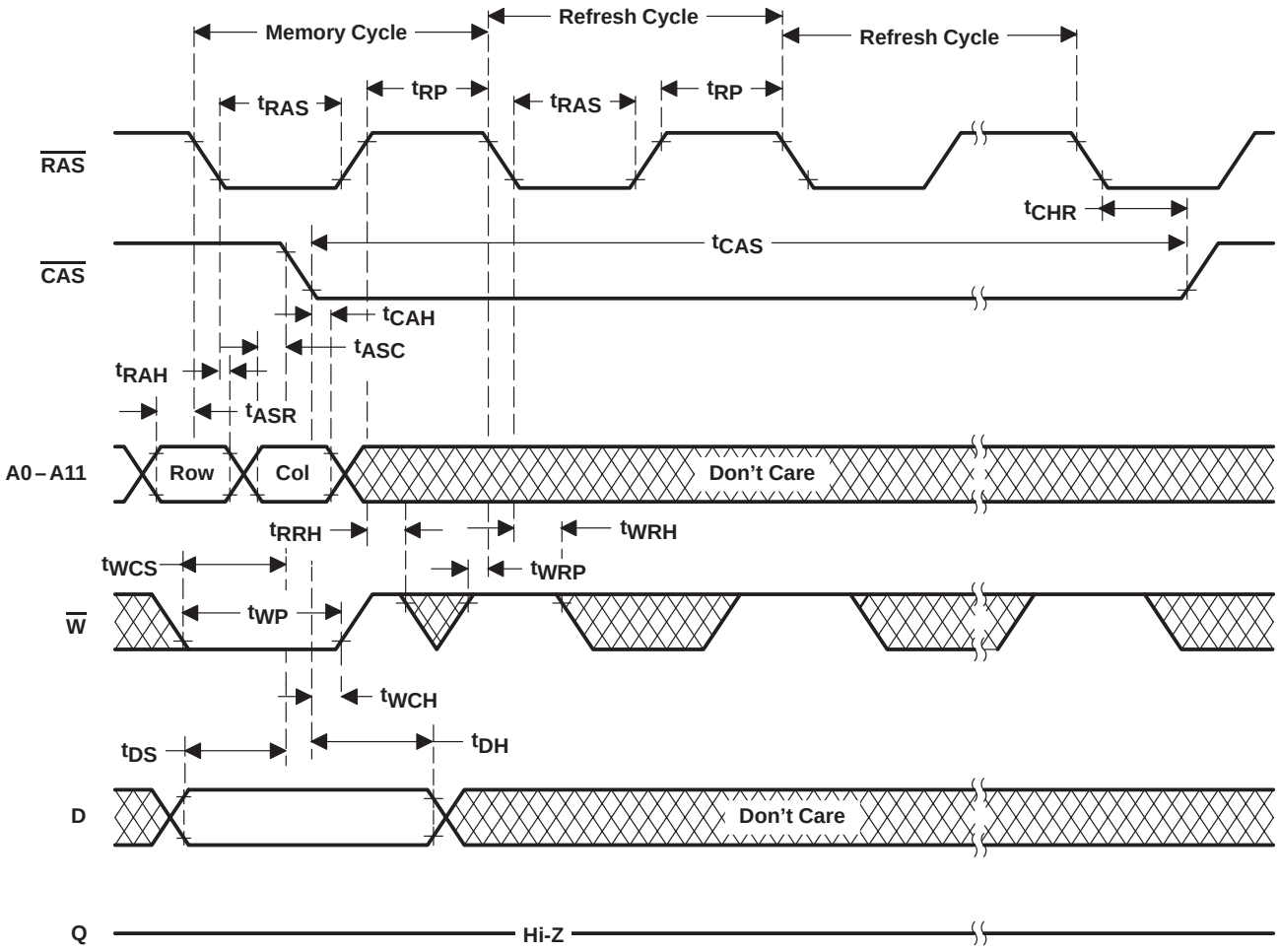


Figure 13. Hidden-Refresh-Cycle (Write) Timing

PARAMETER MEASUREMENT INFORMATION

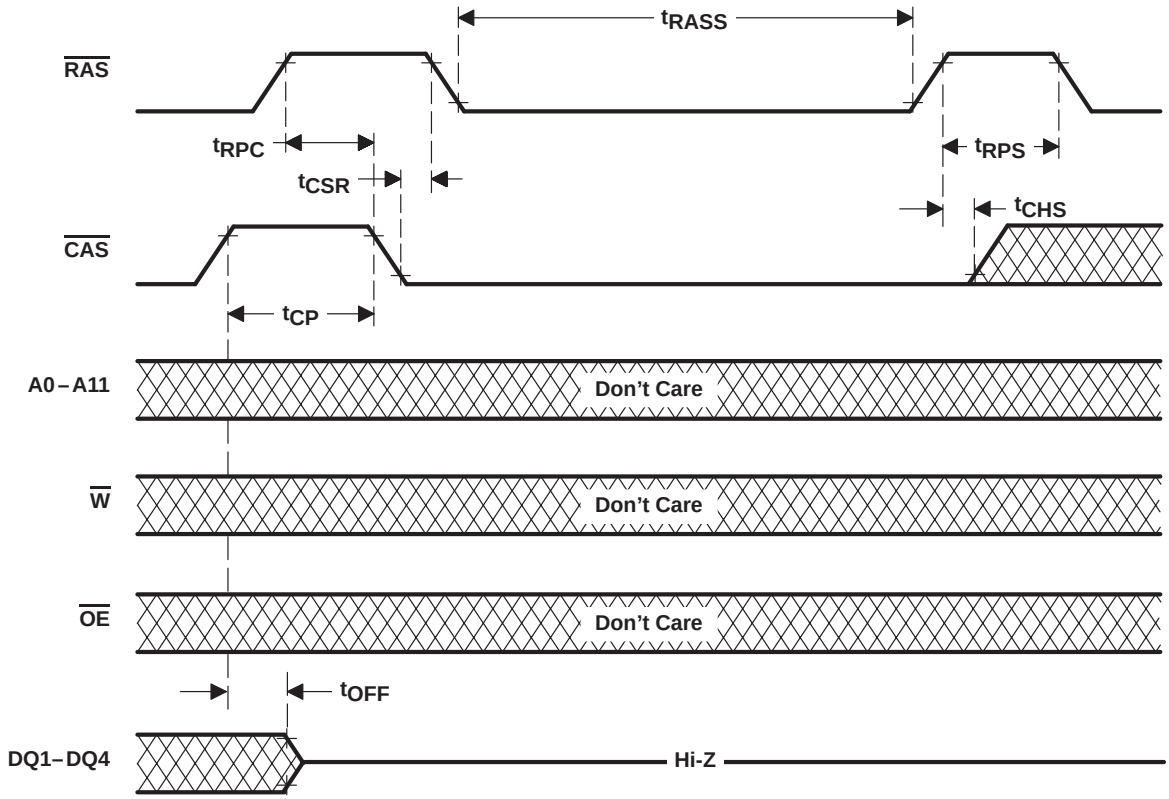


Figure 14. Self-Refresh-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

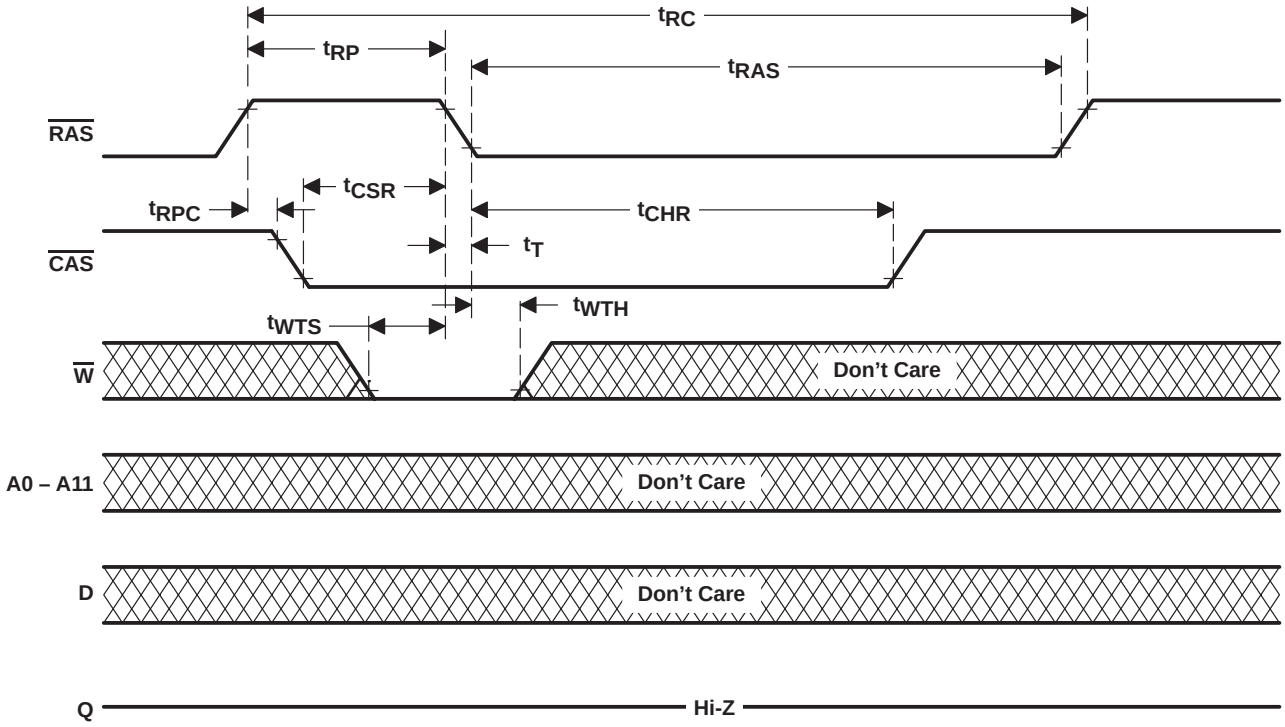


Figure 15. Test-Mode-Entry-Cycle Timing

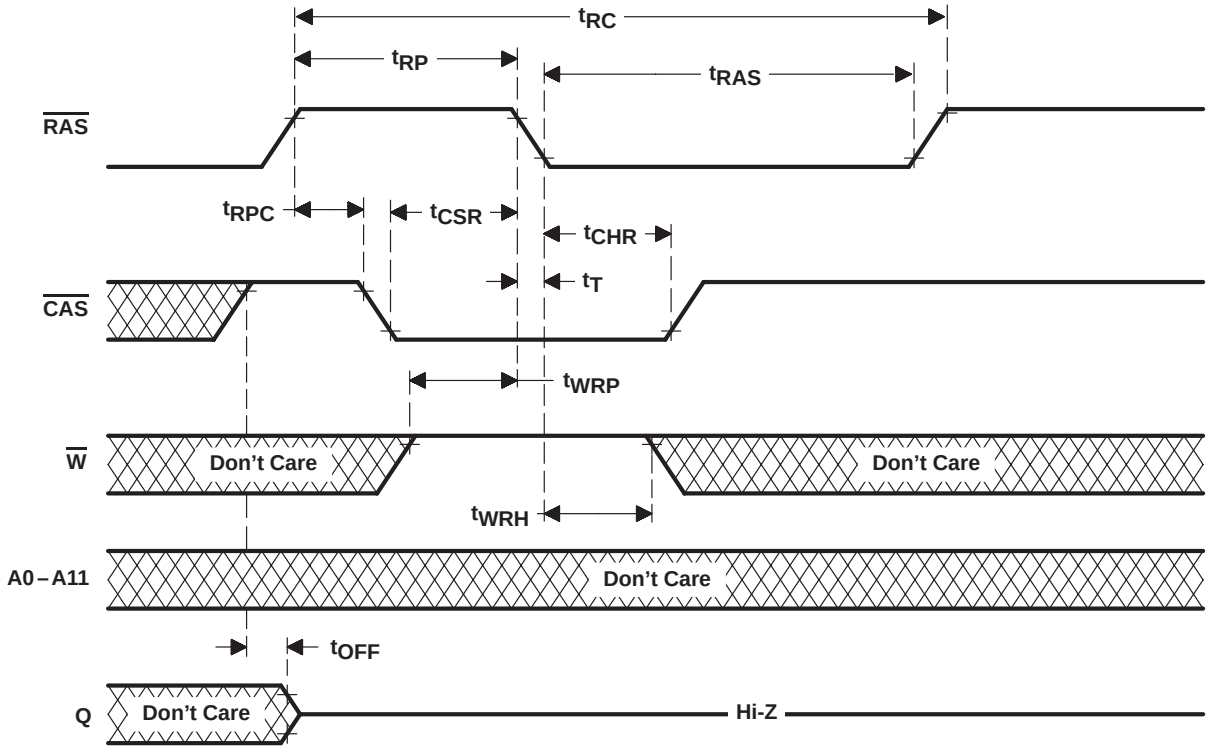
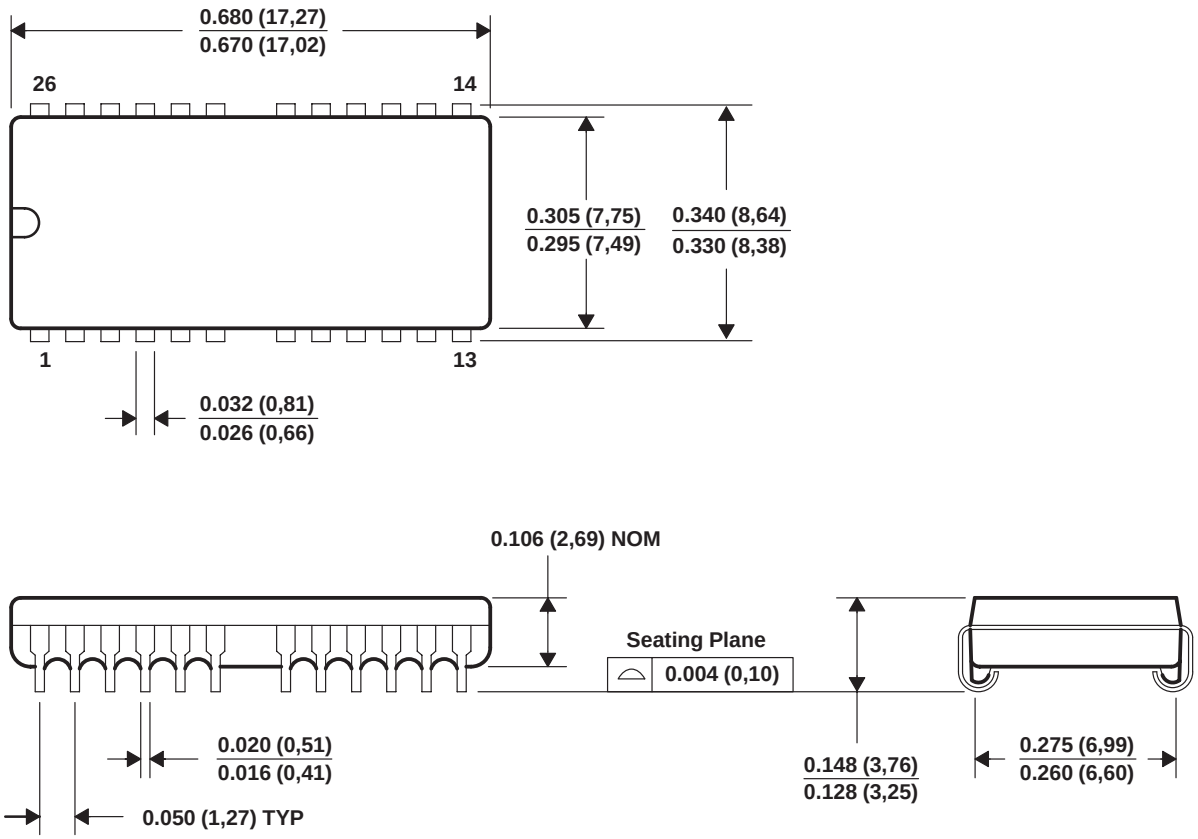


Figure 16. Test-Mode-Exit-Cycle ($\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ Refresh Cycle) Timing

MECHANICAL DATA

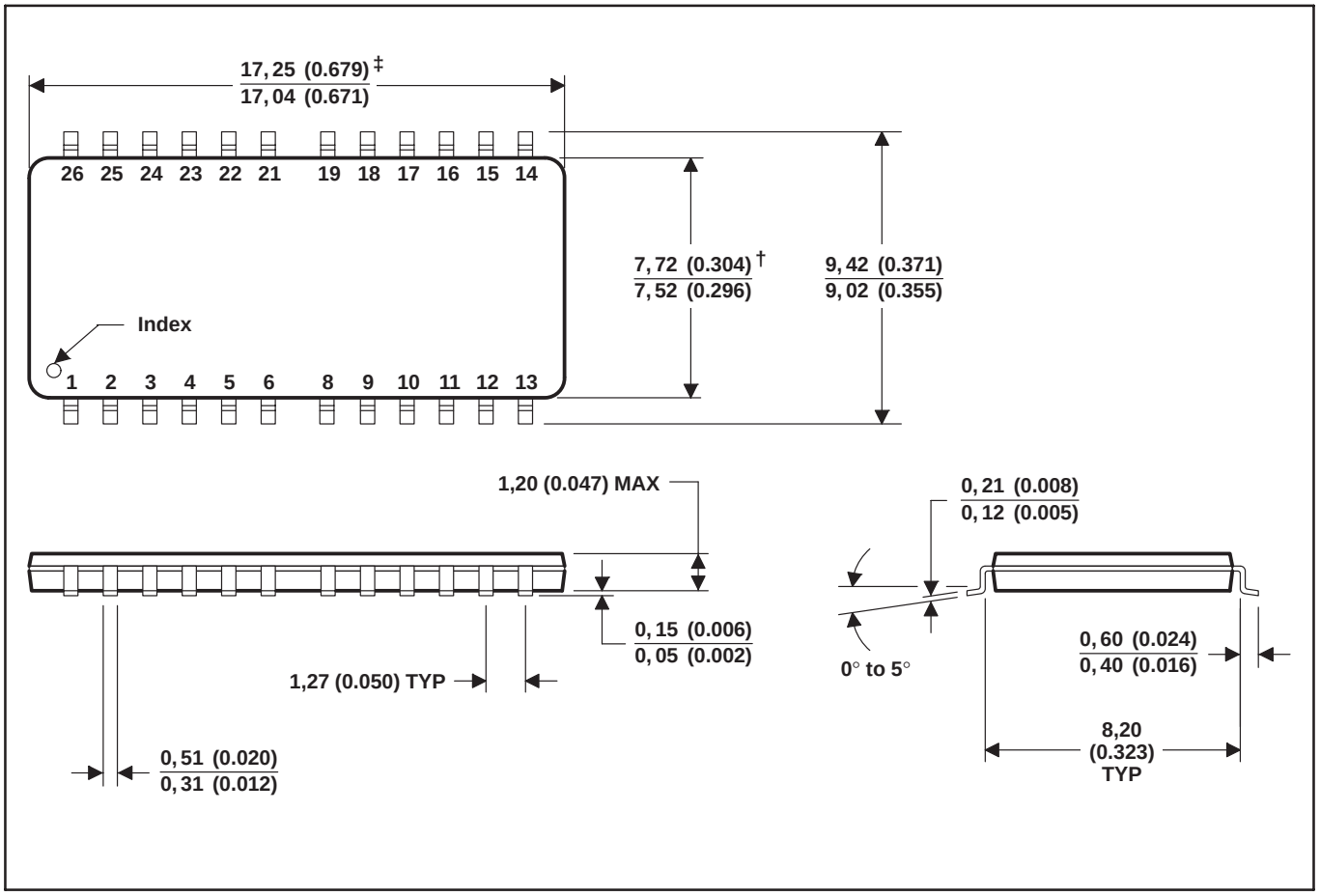
DJ–24/26 LEAD PLASTIC SMALL-OUTLINE J-LEAD PACKAGE R–PDSO–J24/26



NOTES: A. All linear dimensions are in inches (millimeters).
B. Plastic body dimensions do not include mold protrusion. Maximum mold protrusion is 0.005 (0,125).

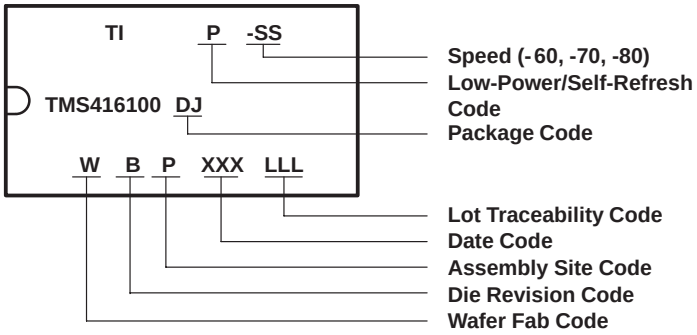
MECHANICAL DATA

DGA–24/26 LEAD PLASTIC THIN SMALL-OUTLINE PACKAGE — R–PDSO–G24/26



† Plastic body width does not include mold protrusion. Maximum mold protrusion is 0,25 (0.010) per side from the edge of the package bottom.
‡ Plastic body length does not include mold protrusion. Maximum mold protrusion is 0,15 (0.006) per side from the edge of the package bottom.
NOTE A: All linear dimensions are in millimeters and parenthetically in inches.

device symbolization



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