

TC74ACT299P/F/FW 8-BIT PIPO SHIFT REGISTER WITH ASYNCHRONOUS CLEAR

TC74ACT323P/F/FW 8-BIT PIPO SHIFT REGISTER WITH SYNCHRONOUS CLEAR

The TC74ACT299 and TC74ACT323 are advanced high speed CMOS 8-BIT PIPO SHIFT REGISTER fabricated with silicon gate and double-layer metal wiring C²MOS technology.

They achieve the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

These devices may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL, NMOS and CMOS output voltage levels.

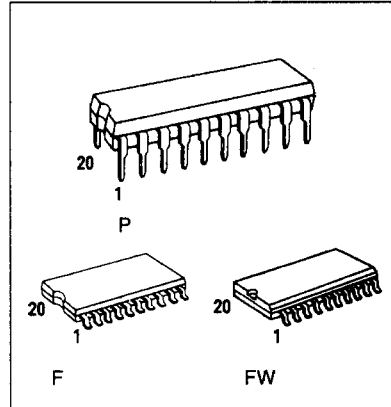
They have four modes (HOLD, SHIFT LEFT, SHIFT RIGHT and LOAD DATA) controlled by the two selection inputs (S0, S1).

When one or both enable ($\overline{G1}$, $\overline{G2}$) are high, the eight I/O outputs are forced to the high-impedance state; however, sequential operation or clearing of the register is not affected. Clear function on the ACT299 is asynchronous to CLOCK, while the ACT323 is cleared synchronous to CLOCK.

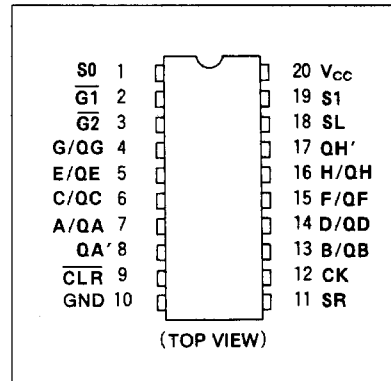
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

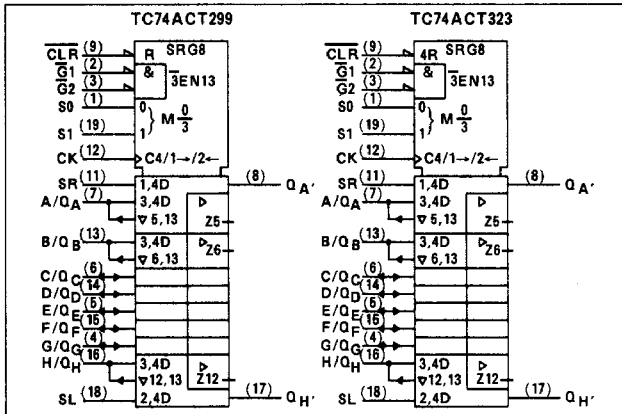
- High Speed $f_{max} =$ MHz (typ.) at $V_{CC}=5V$
- Low Power Dissipation $I_{CC}=4 \mu A$ (Max.) at $T_a=25^\circ C$
- Compatible with TTL outputs $V_{IL} = 0.8V$ (Max.)
 $V_{IH} = 2V$ (Min.)
- Symmetrical Output Impedance ... $|I_{OH}| = I_{OL} = 24mA$ (Min.)
Capability of driving 50 Ω transmission lines.
- Balanced Propagation Delays $t_{pLH} \approx t_{pHL}$
- Pin and Function Compatible with 74F299/323



PIN ASSIGNMENT



IEC LOGIC SYMBOL



APPLICATION NOTES

- 1) Do not apply a signal to any bus terminal when it is in the output mode. Damage may result.
- 2) All floating (high impedance) bus terminals must have their input levels fixed by means of pull up or pull down resistors or bus terminator IC's such as the TOSHIBA TC40117BP.

TC74ACT299, T323P/F/FW-1

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ~ 7.0	V
DC Input Voltage	V_{IN}	-0.5 ~ V_{CC} + 0.5	V
DC Output Voltage	V_{OUT}	-0.5 ~ V_{CC} + 0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±50	mA
DC Output Current	I_{OCT}	±50	mA
DC V_{CC} /Ground Current	I_{CC}	±250	mA
Power Dissipation	P_D	500(DIP)* / 180(SOP)	mW
Storage Temperature	T_{stg}	-65 ~ 150	°C
Lead Temperature 10sec	T_L	300	°C

*500mW in the range of $T_a = -40^{\circ}\text{C} \sim 65^{\circ}\text{C}$. From $T_a = 65^{\circ}\text{C}$ to 85°C a derating factor of $-10\text{mW}/^{\circ}\text{C}$ should be applied up to 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	4.5 ~ 5.5	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	-40 ~ 85	°C
Input Rise and Fall Time	dt/dv	0 ~ 10	ns/v

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	$T_a = 25^{\circ}\text{C}$			$T_a = -40 \sim 85^{\circ}\text{C}$		UNIT	
				MIN.	TYP.	MAX.	MIN.	MAX.		
High-Level Input Voltage	V_{IH}		4.5 } 5.5	2.0	-	-	2.0	-	V	
Low-Level Input Voltage	V_{IL}		4.5 } 5.5	-	-	0.8	-	0.8	V	
High-Level Output Voltage	V_{OH}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -50 \mu\text{A}$	4.5	4.4	4.5	-	4.4	-	V
			$I_{OH} = -24\text{mA}$	4.5	3.94	-	-	3.80	-	
			$I_{OH} = -75\text{mA}^*$	5.5	-	-	-	3.85	-	
Low-Level Output Voltage	V_{OL}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 50 \mu\text{A}$	4.5	-	0.0	0.1	-	0.1	V
			$I_{OL} = 24\text{mA}$	4.5	-	-	0.36	-	0.44	
			$I_{OL} = 75\text{mA}^*$	5.5	-	-	-	-	1.65	
3-State Output Off-State Current	I_{OZ}	$V_{IN} = V_{IH}$ or V_{IL} $V_{OUT} = V_{CC}$ or GND	5.5	-	-	±0.5	-	±5.0	μA	
Input Leakage Current	I_{IN}	$V_{IN} = V_{CC}$ or GND	5.5	-	-	±0.1	-	±1.0		
Quiescent Supply Current	I_{CC}	$V_{IN} = V_{CC}$ or GND	5.5	-	-	8.0	-	80.0		
	ΔI_{CC}	PER INPUT: $V_{IN} = 3.4\text{V}$ OTHER INPUT: V_{CC} or GND	5.5	-	-	1.35	-	1.5	mA	

*: This spec indicates the capability of driving 50Ω transmission lines.
One output should be tested at a time for a 10ms maximum duration.

TC74ACT299, T323P/F/FW-2

TRUTH TABLE

MODE	INPUTS									INPUTS/ OUTPUTS		OUTPUTS	
	CLR	FUNCTION SELECT		OUTPUT CONTROL		CK		SERIAL		A/QA	H/QH	QA'	QH'
		S1	S0	G1*	G2*	(299)	(323)	SL	SR				
CLEAR	L	H	H	X	X	X	⌋	X	X	Z	Z	L	L
	L	L	X	L	L	X	⌋	X	X	L	L	L	L
	L	X	L	L	L	X	⌋	X	X	L	L	L	L
HOLD	H	L	L	L	L	X	X	X	X	QA0	QH0	QA0	QH0
SHIFT	H	L	H	L	L		⌋	X	H	H	QGn	H	QGn
RIGHT	H	L	H	L	L		⌋	X	L	L	QGn	L	QGn
SHIFT	H	H	L	L	L		⌋	H	X	QBn	H	QBn	H
LEFT	H	H	L	L	L		⌋	L	X	QBn	L	QBn	L
LOAD	H	H	H	X	X		⌋	X	X	a	h	a	h

* When one or both output controls are high, the eight input/output terminals are in the high-impedance state; however sequential or clearing of the register is not affected.

Z : High Impedance

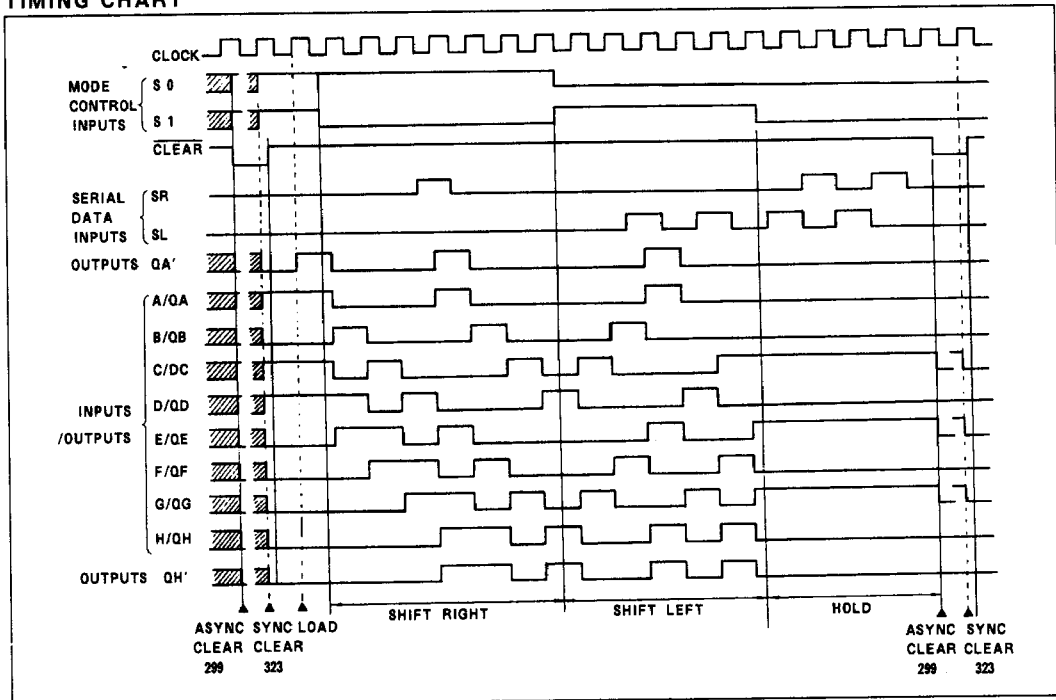
Qn0 : The level of An before the indicated steady-state input conditions were established.

Qnn : The level of Qn before the most recent active transition indicated by ↓ or ↑.

a,h : The level of the steady-state inputs A, H, respectively.

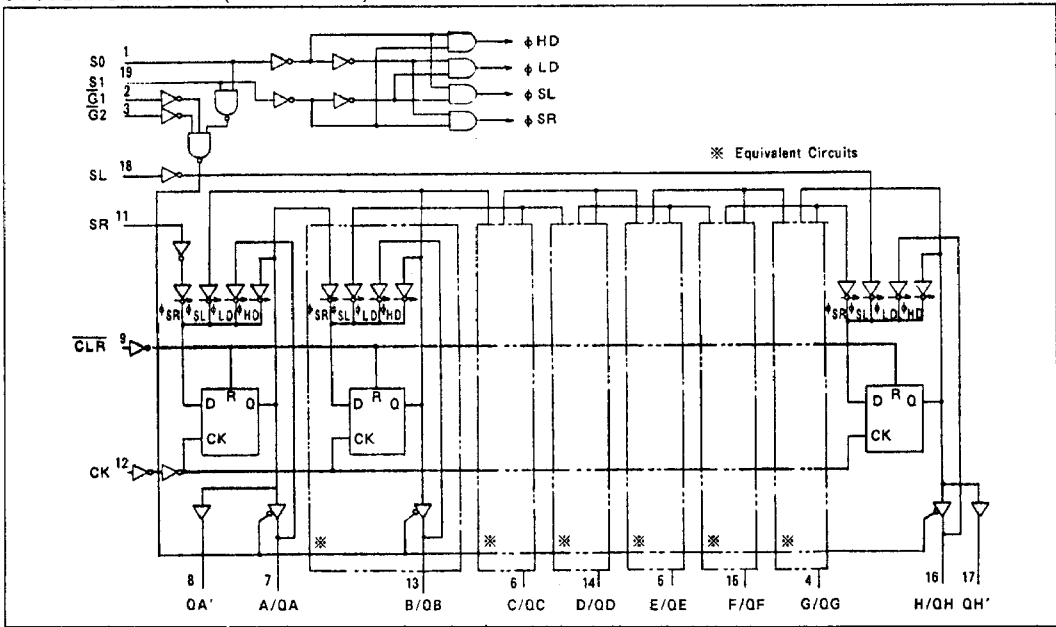
X : Don't care

TIMING CHART

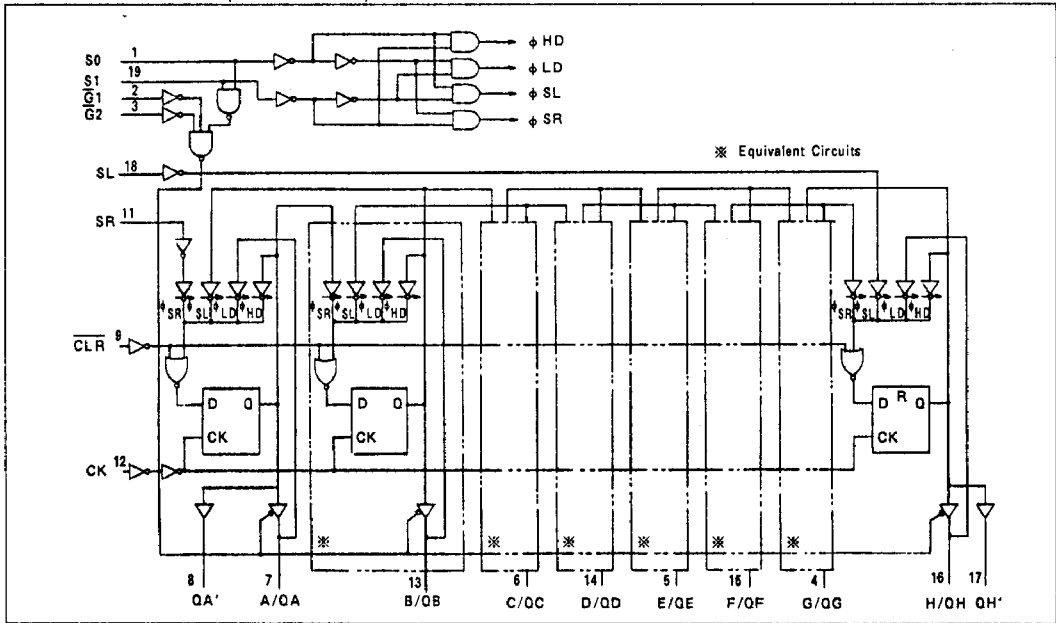


TC74ACT299, T323P/F/FW-3

SYSTEM DIAGRAM (TC74ACT299)



SYSTEM DIAGRAM (TC74ACT323)



TC74ACT299, T323P/F/FW-4

TIMING RECOMMENDED OPERATING CONDITIONS (Input $t_r=t_f=3ns$)

PARAMETER	SYMBOL	TEST CONDITION	Ta=25°C			Ta=-40 ~85°C	UNIT
			V _{CC}	TYP.	LIMIT	LIMIT	
Minimum Pulse Width (CK)	t _{w(H)} t _{w(L)}		5.0±0.5	-	5.0	5.0	ns
Minimum Pulse Width (CLR)*	t _{w(L)}		5.0±0.5	-	5.0	5.0	
Minimum Set-up Time (SL,SR,A~H)	t _s		5.0±0.5	-	3.5	3.5	
Minimum Set-up Time (S0,S1)	t _s		5.0±0.5	-	6.0	6.5	
Minimum Set-up Time (CLR)**	t _s		5.0±0.5	-	2.5	2.5	
Minimum Hold Time (SL,SR,A~H)	t _h		5.0±0.5	-	2.0	2.0	
Minimum Hold Time (S0,S1)	t _h		5.0±0.5	-	0	0	
Minimum Hold Time (CLR)**	t _h		5.0±0.5	-	2.5	2.5	
Minimum Removal Time (CLR)*	t _{rem}		5.0±0.5	-	2.0	2.0	

Note :* TC74ACT299 only

** TC74ACT323 only

TC74ACT299,T323P/F/FW-5

AC ELECTRICAL CHARACTERISTICS (CL =50pF,RL =500Ω, tr =tf =3ns)

PARAMETER	SYMBOL	TEST CONDITION	V _{CC}	T _a =25°C			T _a =-40~85°C		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time (CK-QA'QH')	t _{pHL} t _{pHL}		5.0±0.5	-	7.2	10.5	1.0	12.0	ns
Propagation Delay Time (CLR-QA'QH') *	t _{pHL}		5.0±0.5	-	6.0	10.0	1.0	11.5	
Propagation Delay Time (CK-QA~QH)	t _{pLH} t _{pLH}		5.0±0.5	-	7.4	11.4	1.0	13.0	
Propagation Delay Time (CLR-QA~QH) *	t _{pLH}		5.0±0.5	-	6.3	10.5	1.0	12.0	
Output Enable time	t _{pZL} t _{pZL}		5.0±0.5	-	7.4	11.4	1.0	13.0	
Output Disable time	t _{pLZ} t _{pLZ}		5.0±0.5	-	7.2	9.6	1.0	11.0	
Maximum Clock Frequency	f _{MAX}		5.0±0.5		120	-	80	-	MHz
Input Capacitance	C _{IN}			-	5	10	-	10	pF
Bus Input Capacitance	C _{I/O}			-	13	-	-	-	
Power Dissipation Capacitance	C _{PP(1)}			-	160	-	-	-	

Note(1) C_{PD} is defined as the value of the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC \text{ (pd)}} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

* TC74ACT299 only

** TC74ACT323 only

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