HIGH TEMPERATURE INTELLIGENT GATE DRIVER

FEATURES

- ▲ Operational beyond the -60°C to +230°C temperature range.
- ▲ Supply voltage from 4.5V to 40V.
- ▲ Integrated charge-pump inside pull-up drivers allowing 100% duty-cycle PWM control signal.
- ▲ Internal 5V LDO regulator.
- ▲ Safe start-up of normally-on devices.
- ▲ Isolated data transmission trough multi-channel transceiver.
- ▲ Half bridge cross-conduction protection.
- ▲ Double pull-up driver with possible pulsed operation with combined 6A capability.
- ▲ Pull-dow driver with 3A capability.
- ▲ On-chip active Miller clamp switch with 3A capability.
- ▲ Resistor-programmable Under voltage lockout (ULVO).
- ▲ Resistor-programmable drain desaturation detection.
- ▲ Resistor-programmable gate failure detection.
- ▲ Resistor-programmable over-current protection level.
- ▲ Capacitor-programmable pulsed operation of pull-up driver.
- ▲ Capacitor-programmable blanking time of protections.
- ▲ Capacitor programmable active Miller clamp.
- ▲ Latch-up free.
- ▲ Ruggedized SMT packages.
- ▲ Also available as bare die.

APPLICATIONS

- ▲ Reliability-critical, Automotive, Aeronautics & Aerospace, Down-hole, Energy Conversion, Solar.
- ▲ Intelligent Power Modules (IPM).
- ▲ Motor drives.
- ▲ Uninterruptible power supplies (UPS).
- ▲ Power inverters.
- ▲ Power conversion and power factor correction (PFC).
- ▲ DC/DC converters and switched mode power supplies (SMPS).

DESCRIPTION

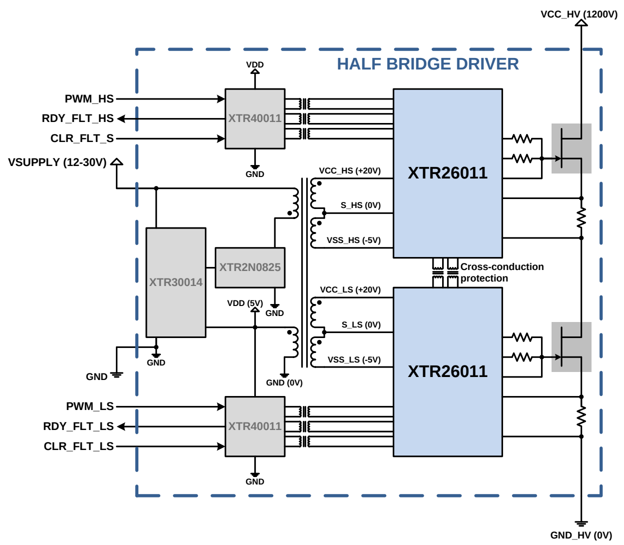
XTR26010 is a high-temperature, high reliability isolated power transistor driver integrated circuit, designed with a high focus on offering a robust, reliable, compact and efficient solution for driving a large variety of high-temperature, high-voltage, and high-efficiency power transistors. XTR26010 is able to drive normally-On and normally-Off power transistors in Silicon Carbide (SiC), Gallium Nitride (GaN) and standard silicon, including JFETs, MOSFETs, BJTs, SJTs and MESFETs.

The XTR26010 circuit implements an unprecedented functionality for high-temperature drivers allowing safe operation at system level by preventing any cross-conduction between high-side and low-side switches, through isolated communication between high-side and low-side drivers. Other features include internal voltage regulator, 5-channel transceiver (2 TX and 3 RX) for isolated data transmission with the microcontroller and between high side and low side drivers. To turn on some normally-off power transistors, the XTR26010 includes two independent pull-up gate-drive-channels (PU_DR1 and PU_DR2) capable of sourcing a typical 3A peak current, with a programmable pulse-width for DR1 channel. The XTR26010 includes two pull-down gate-drive-channels capable of sinking a typical 3A peak current (PD_DR and PD_MC). The PD_DR channel is used for the effective turn-off of the power transistor, while PD_MC channel is used for Active Miller Clamping (AMC) function thanks to its capacitor-programmable delay versus PD_DR channel.

The circuit includes soft shut-down capability that slowly shuts down the power transistor in case of fault. The XTR26010 is able to detect failures on the drain, gate and source of the power switch. In addition, safe start-up and cross-conduction protection are implemented to guarantee safe operation at system level.

The XTR26010 can be used standalone but also as a controller with multiplied drive capabilities using the XTR25010, which is the driver part of the XTR26010 without the other functions: internal regulator, transceiver, protection circuits,…

PRODUCT HIGHLIGHT



ORDERING INFORMATION

X → Source: X = X-REL Semi

TR → Process: TR = HiTemp, HiRel

26 → Part family

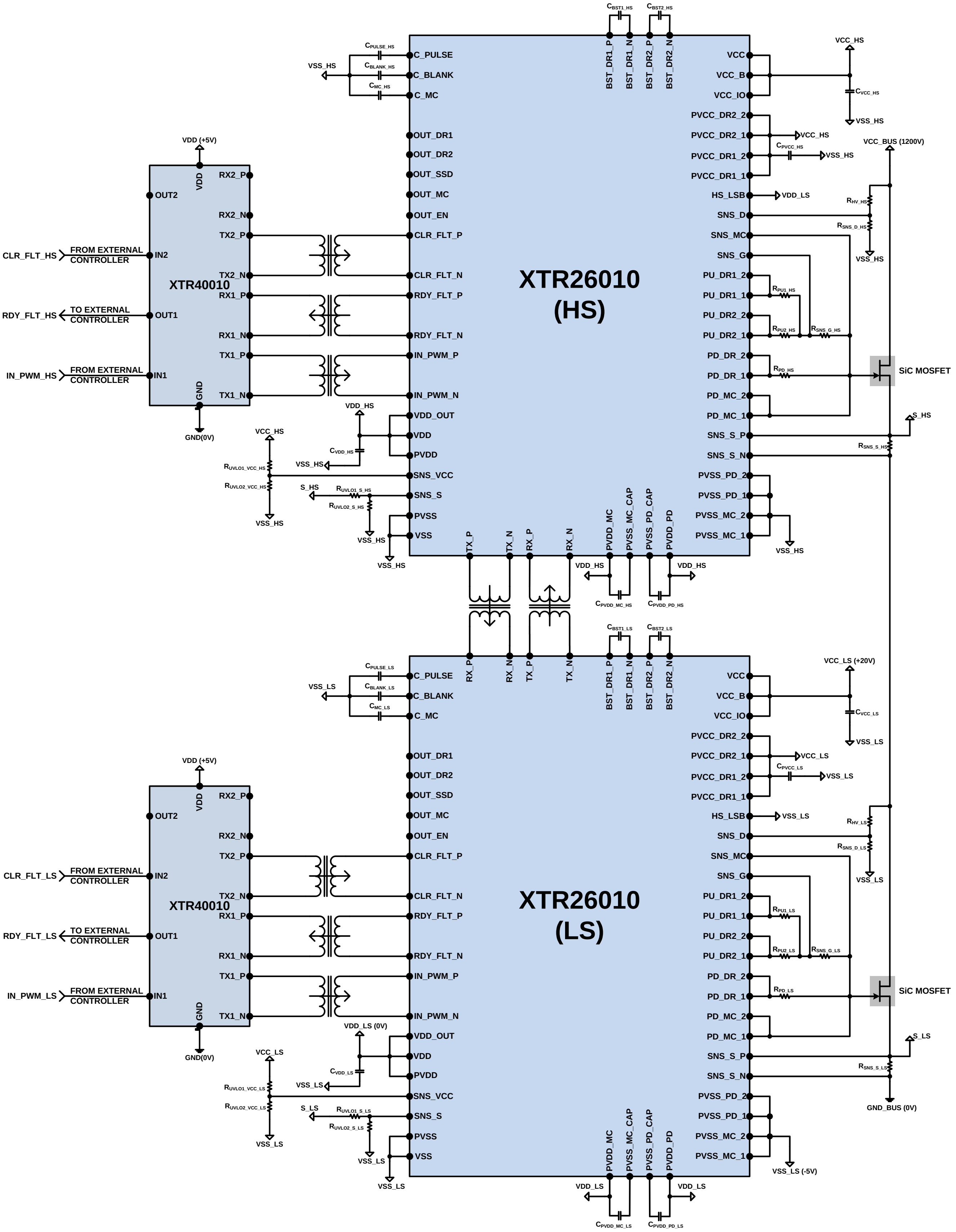
010 → Part number

Product Reference	Temperature Range	Package	Pin Count	Marking
XTR26010-BD	-60°C to +230°C	Bare die		
XTR26011-LJ	-60°C to +230°C	Ceramic LJCC68	68	**XTR26011**

Other packages and packaging configurations possible upon request.

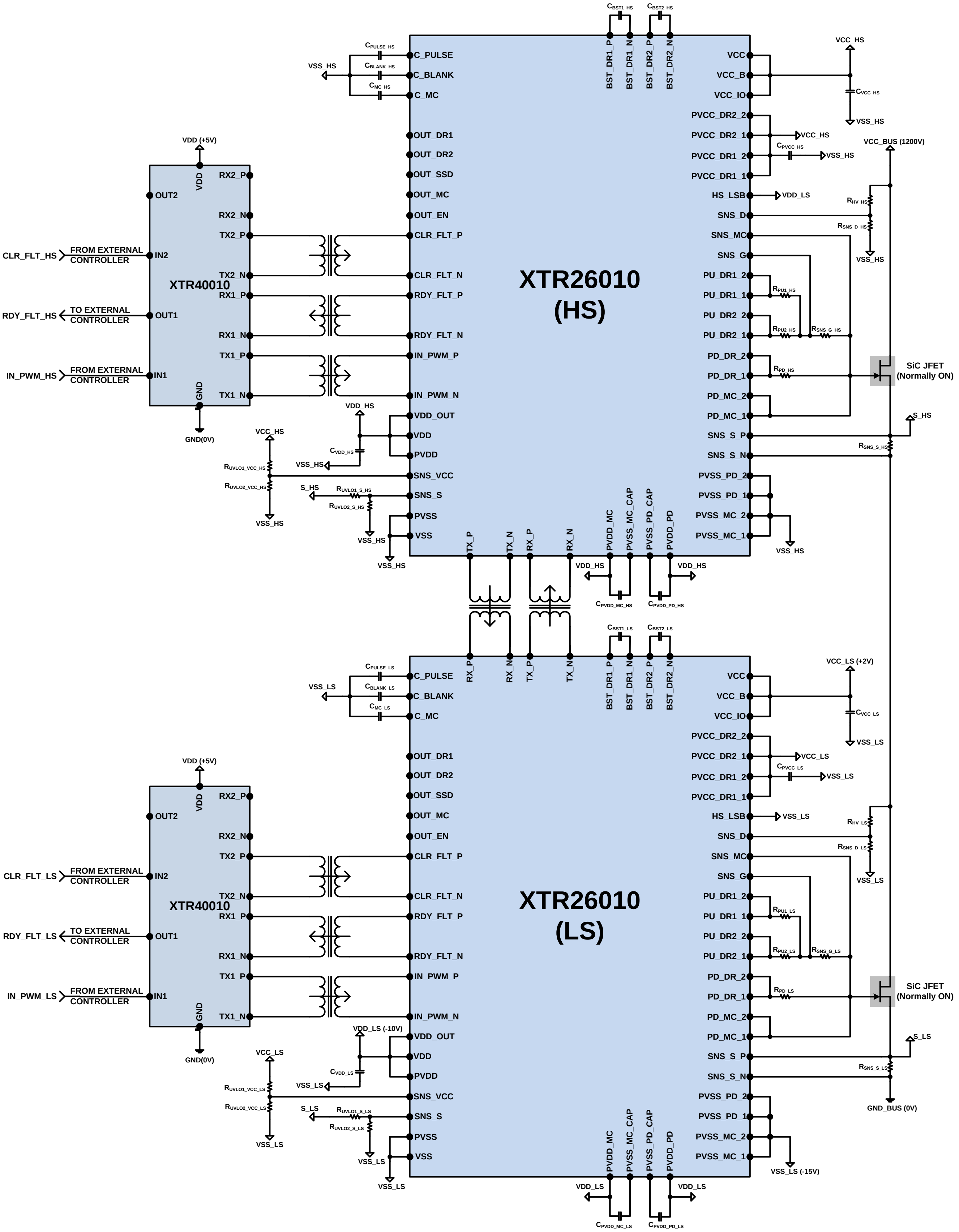
TYPICAL APPLICATIONS

Driving SiC MOSFET



TYPICAL APPLICATIONS (CONTINUED)

Driving Normally ON SiC JFET

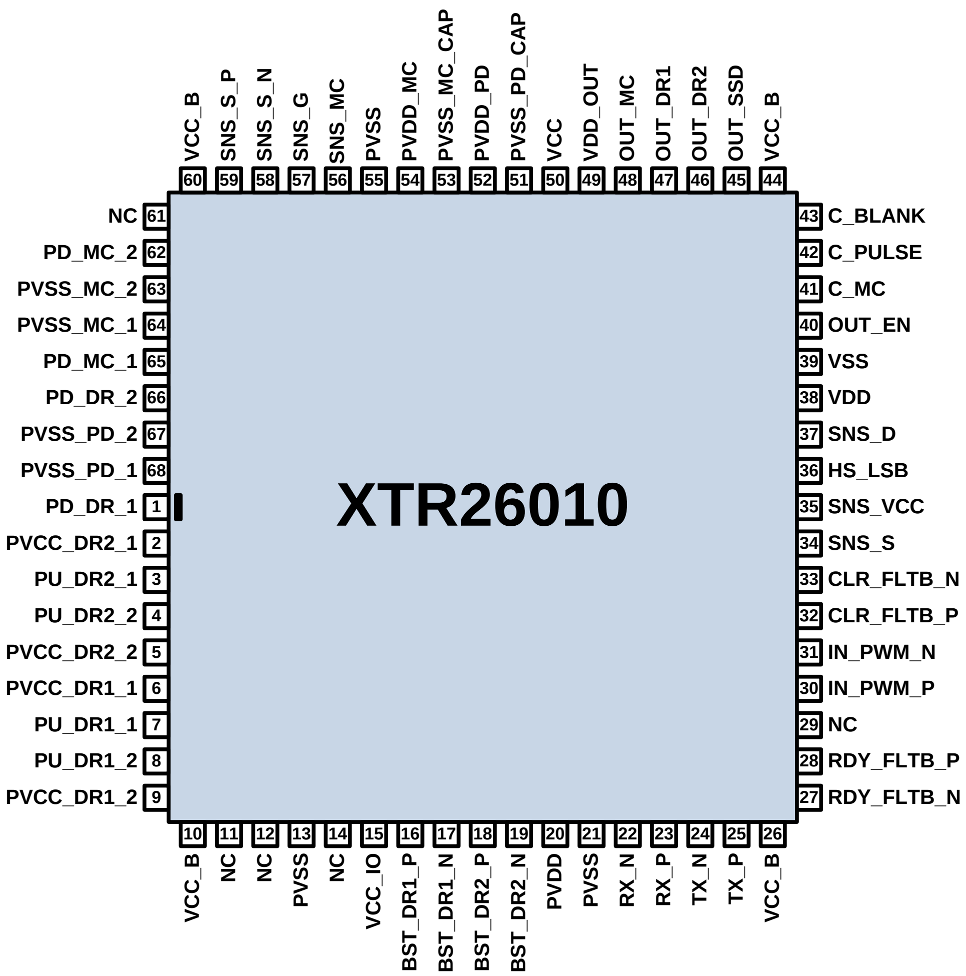


ABSOLUTE MAXIMUM RATINGS

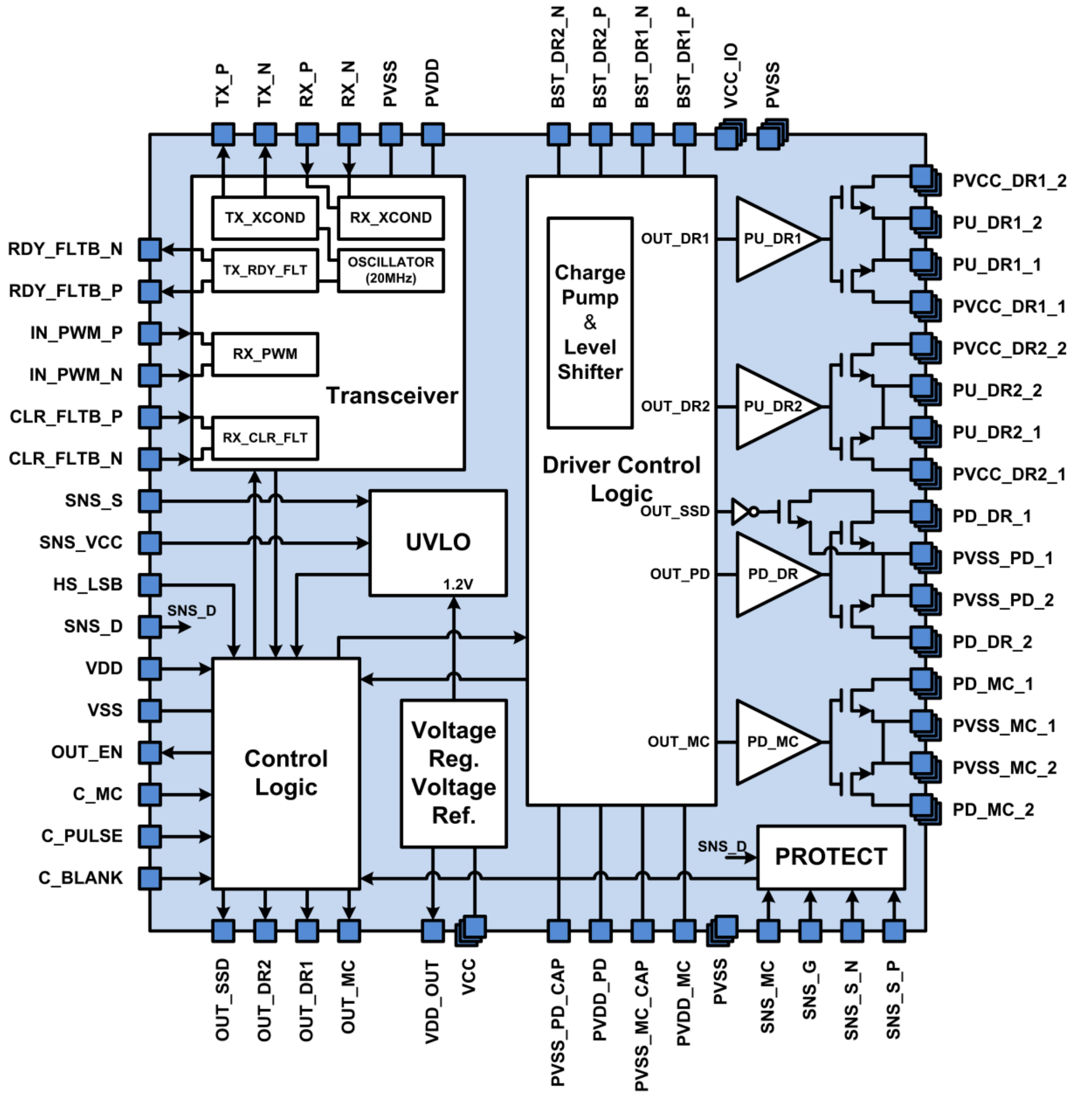
Supply voltage:	VCC_IO-PVSS	-0.5V to 44V
	VCC, VCC_B, and PVCC_DRx_x	PVSS-0.5V to VCC_IO+0.5V
	PVDD-PVSS	-0.5V to 5.5V
	VDD, PVDD_PD, and PVDD_MC	VSS-0.5V to VDD+0.5V
	VSS, PVSS_MC, PVSS_PD	PVSS-0.5V to PVSS+0.5V
Inputs pins:	IN_PWM_P, IN_ PWM_P, CLR_FLTB_N, CLR_FLTB_N, RX_P, RX_N, SNS_VCC, SNS_S, HS_LSB, SNS_D	PVSS-0.5V to PVDD+0.5V
Outputs pins:	PD_MC_x and PD_DR_x	PVSS-0.5V to VCC_IO+0.5V
	PU_DR1_1 and PU_DR1_2	PVSS-0.5V to PVCC_DR1+0.5V
	PU_DR1_1 and PU_DR1_2	PVSS-0.5V to PVCC_DR2+0.5V
	OUT_EN, OUT_DR1, OUT_DR2, OUT_MC, OUTSSDTX_P, TX_N, RDY_FLT_P, RDY_FLT_N, VDD_OUT	PVSS-0.5V to PVDD+0.5V
Storage Temperature Range		-70°C to +230°C
Operating Junction Temperature Range		-70°C to +300°C
ESD Classification		1kV HBM MIL-STD-883

Caution: *Stresses beyond those listed in "ABSOLUTE MAXIMUM RATINGS" may cause permanent damage to the device. These are stress ratings only and functionality of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to "ABSOLUTE MAXIMUM RATINGS" conditions for extended periods may permanently affect device reliability.*

PACKAGING (CCJ68: 68 J-LEAD CERAMIC CHIP CARRIER)



BLOCK DIAGRAM (XTR26010-BD)



Die level block diagram showing all available functionalities and bond-pads.

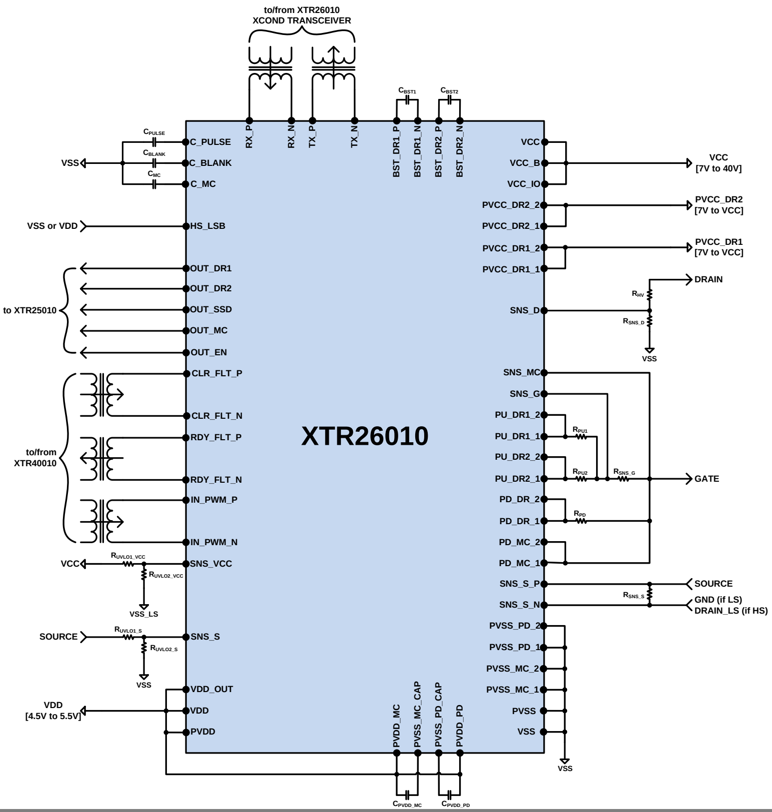
PIN DESCRIPTION (CCJ68)

Pin number	Name	Description
1	**PD_DR_1**	Output of the pull-down driver PD_DR with typical 2A peak drive current. Connect to **PD_DR_2** to have typical 3A peak drive current.
2	**PVCC_DR2_1**	Positive supply voltage of PU_DR2 driver. Connect to local power **VCC** plane.
3	**PU_DR2_1**	Output of the pull-up driver PU_DR2 with typical 1.5A peak drive current. Connect to **PU_DR2_2** to have typical 3A peak drive current.
4	**PU_DR2_2**	Output of the pull-up driver with a typical 1.5A peak drive current. Connect to **PU_DR2_1** to have a typical 3A peak drive current.
5	**PVCC_DR2_2**	Positive supply voltage of PU_DR2 driver. Connect to local power **VCC** plane.
6	**PVCC_DR1_1**	Positive supply voltage of PU_DR1 driver. Connect to local power **VCC** plane.
7	**PU_DR1_1**	Output of the pull-up driver PU_DR1 with a typical 1.5A peak drive current and programmable pulse width. Connect to **PU_DR1_2** to have a typical 3A peak drive current.
8	**PU_DR1_2**	Output of the pull-up driver PU_DR1 with a typical 1.5A peak drive current and programmable pulse width. Connect to **PU_DR2_1** to have a typical 3A peak drive current.
9	**PVCC_DR1_2**	Positive supply voltage of PU_DR1 driver. Connect to local power **VCC** plane.
10	**VCC_B**	Connect to power **VCC** plane.
11	**NC**	No internal connection.
12	**NC**	No internal connection.
13	**PVSS**	Power **VSS**. Connect to **VSS** through a local plane.
14	**NC**	No internal connection.

Pin number	Name	Description
15	**VCC_IO**	Supply voltage of the high-voltage IO ring. Connect to power **VCC** plane.
16	**BST_DR1_P**	Positive terminal of the bootstrap capacitor of the PU_DR1 driver.
17	**BST_DR1_N**	Negative terminal of the bootstrap capacitor of the PU_DR1 driver.
18	**BST_DR2_P**	Positive terminal of the bootstrap capacitor of the PU_DR2 driver.
19	**BST_DR2_N**	Negative terminal of the bootstrap capacitor of the PU_DR2 driver.
20	**PVDD**	5V supply voltage versus **PVSS** supplying the transceiver and the output stage of the drivers. Connect to **VDD_OUT** or an external 5V supply voltage versus **PVSS** through a local power **VDD** plane.
21	**PVSS**	Power **VSS**. Connect to **VSS** through a local plane.
22	**RX_N**	Negative input of the internal receiver of the cross-conduction information between HS and LS.
23	**RX_P**	Positive input of the internal receiver of the cross-conduction information between HS and LS.
24	**TX_N**	Negative output of the internal transmitter of the cross-conduction information between HS and LS.
25	**TX_P**	Positive output of the internal transmitter of the cross-conduction information between HS and LS.
26	**VCC_B**	Connect to power **VCC** plane.
27	**RDY_FLT_N**	Negative output giving the READY/FAULT information to the micro-controller through the isolated transceiver.
28	**RDY_FLT_P**	Positive output giving the READY/FAULT information to the micro-controller through the isolated transceiver.
29	**NC**	No internal connection.
30	**IN_PWM_P**	Positive input receiving the PWM signal from the micro-controller through the isolated transceiver.
31	**IN_PWM_N**	Negative input receiving the PWM signal from the micro-controller through the isolated transceiver.
32	**CLR_FLT_P**	Positive input receiving the CLEAR FAULT information from the micro-controller through the isolated transceiver.
33	**CLR_FLT_N**	Negative input receiving the CLEAR FAULT information from the micro-controller through the isolated transceiver.
34	**SNS_S**	Sense node through external resistor divider for the UVLO on the **SOURCE** terminal of the power transistor versus **VSS**. Voltage on this node is compared to an internal reference of 1.2V versus **VSS**.
35	**SNS_VCC**	Sense node for the UVLO on **VCC** pin versus **VSS**. Voltage on this node is compared to an internal reference of 1.2V versus **VSS**.
36	**HS_LSB**	Digital input for driver operation selection as high-side (HS_LSB=1) or low-side (HS_LSB=0).
37	**SNS_D**	Sense node through external resistor divider of the **DRAIN** terminal of the power switch for desaturation detection. Voltage on this node is compared to an internal reference of 0.5V versus **VSS**.
38	**VDD**	5V supply voltage versus **VSS**, supplying all logic except the output stage of the drivers and the transceiver. . Connect to **VDD_OUT** or an external 5V supply voltage versus **VSS** through a local **VDD** plane.
39	**VSS**	Negative supply voltage of the driver (its value depends on the power transistor to be driven). Connect to the reference ground plane of the circuit.
40	**OUT_EN**	Digital output enable signal for the driver outputs. To be connected to **EN** pin when XTR25010 is used together with XTR26010.
41	**C_MC**	Connect a capacitor between this pin and **VSS** plane to define the Miller Clamp delay
42	**C_PULSE**	Connect a capacitor between this pin and **VSS** to define the pulse width of **OUT_DR1**. If connected to **VDD** the pulse width is equal to the input PWM signal ON time.
43	**C_BLANK**	Connect a capacitor between this pin and **VSS** to define the blanking time.
44	**VCC_B**	Connect to power **VCC** plane.
45	**OUT_SSD**	Digital output control signal of soft-shutdown driver. To be connected to **IN_SSD** pin of XTR25010 when it is used together with XTR26010.
46	**OUT_DR2**	Digital output control signal of pull-up driver PU_DR2. To be connected to **IN_DR2** pin of XTR25010 when it is used together with XTR26010.
47	**OUT_DR1**	Digital output control signal of pull-up driver PU_DR1. To be connected to **IN_DR1** pin of XTR25010 when it is used together with XTR26010.
48	**OUT_MC**	Digital output control signal of Active Miller Clamp pull-down driver PD_MC. To be connected to **IN_MC** pin of XTR25010 when it is used together with XTR26010.
49	**VDD_OUT**	Output of internal voltage regulator generating 5V versus **VSS**. Connect to **VDD/PVDD** to supply the 5V parts of the circuit.
50	**VCC**	Positive supply voltage of the driver (its value depends on the power transistor to be driven).
51	**PVSS_PD_CAP**	Bottom plate of decoupling capacitor of the pull-down (PD_DR) pre-driver. This pin is internally connected to **PVSS_PD_1/PVSS_PD_2**. Do not connect to **VSS** plane.
52	**PVDD_PD**	Top plate of decoupling capacitor of the pull-down (PD_DR) pre-driver. Connect to **PVDD** plane.
53	**PVSS_MC_CAP**	Bottom plate of decoupling capacitor of the Miller clamp (PD_MC) pre-driver. This pin is internally connected to **PVSS_MC_1/PVSS_MC_2**. Do not connect to **VSS** plane.
54	**PVDD_MC**	Top plate of decoupling capacitor of the Miller Clamp (PD_MC) pre-driver. Connect to **PVDD** plane.
55	**PVSS**	Power **VSS**. Connect to **VSS** through a local plane.

Pin number	Name	Description
56	**SNS_MC**	Sense pin of the Miller Clamp. Connect to the **GATE** terminal of the power transistor.
57	**SNS_G**	Sense pin of the power switch gate (gate failure detection). Connect to the **GATE** terminal of the power transistor through a series sense resistor.
58	**SNS_S_N**	Negative sense pin of the **SOURCE** terminal of the power switch source (over-current detection).
59	**SNS_S_P**	Positive sense pin of the **SOURCE** terminal of the power switch source (over-current detection).
60	**VCC_B**	Connect to power **VCC** plane.
61	**NC**	No internal connection.
62	**PD_MC_2**	Output of the Miller Clamp pull-down driver with a typical 2A peak drive current. Connect to **PU_MC_1** to have a typical 3A peak drive current.
63	**PVSS_MC_2**	Power **VSS** of the PD_MC driver. Connect to **PVSS** plane.
64	**PVSS_MC_1**	Power **VSS** of the PD_MC driver. Connect to **PVSS** plane.
65	**PD_MC_1**	Output of the Miller Clamp pull-down driver PD_MC with a typical 2A peak drive current. Connect to **PU_MC_2** to have a typical 3A peak drive current.
66	**PD_DR_2**	Output of the pull-down driver PD_DR with a typical 2A peak drive current. Connect to **PU_DR2_2** to have a typical 3A peak drive current.
67	**PVSS_PD_2**	Power VSS of PD_DR driver. Connect to **PVSS** plane.
68	**PVSS_PD_1**	Power VSS of PD_DR driver. Connect to **PVSS** plane.

RECOMMENDED OPERATING CONDITIONS

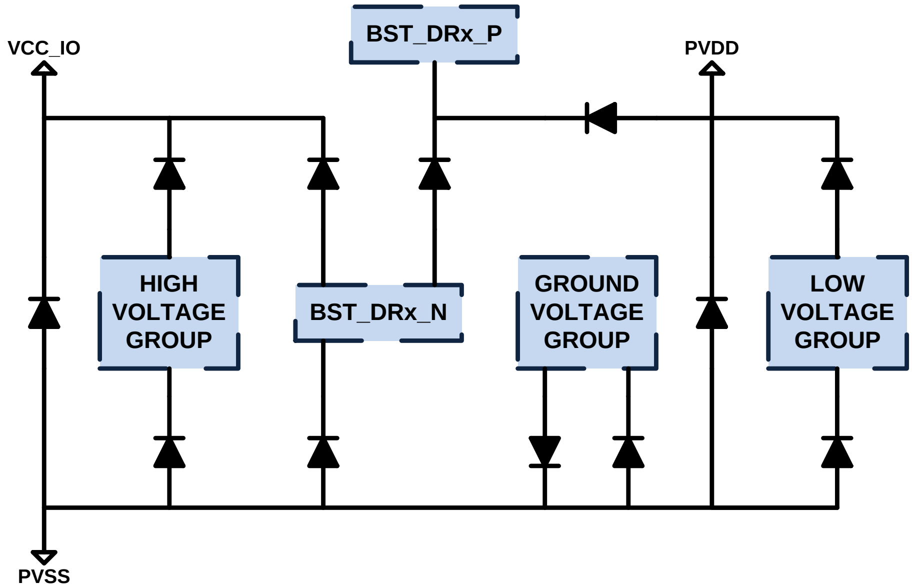


Parameter	Min	Typ	Max	Units
High voltage power supply VCC-VSS	7		40	V
High voltage power supply PVCC_DR1	VSS+7		VCC	V
High voltage power supply PVCC_DR2	VSS+7		VCC	V
High voltage inputs: SNS_G, SNS_MC, SNS_S_N, SNS_S_P	VSS		VCC	
High voltage outputs: PD_DR_1, PD_DR_2, PU_DR2_1, PU_DR2_2, PU_DR1_1, PU_DR1_2, PD_MC_2, PD_MC_1	VSS		VCC	
Low voltage power supply VDD-VSS (external or from internal voltage regulator)	4.5		5.5	V
Low voltage inputs: IN_PWM_N, IN_PWM_P, CLR_FLT_N, CLR_FLT_P, HS_LSB, SNS_D, SNS_S, SNS_VCC, RX_P, RX_N	VSS		VDD	
Low voltage outputs: OUT_DR1, OUT_DR2, OUT_SSD, OUT_MC, OUT_EN, RDY_FLT_P, RDY_FLT_N, TX_P, TX_N	VSS		VDD	
Junction Temperature[1] T_j	-60		230	°C

[1] Operation beyond the specified temperature range is achieved.

ESD CLAMPING SCHEME

Pin Groups	Pins
High voltage power supply	VCC-PVSS
High voltage group	PD_DR_1, PD_DR_2, PU_DR2_1, PU_DR2_2, PU_DR1_1, PU_DR1_2, VCC_B, VCC_IO, BST_DR1_N, BST_DR2_N, VCC, SNS_MC, SNS_S_N, SNS_S_P, PD_MC_2, PD_MC_1
Low voltage power supply	VDD-PVSS
Low voltage group	PVDD, RX_N, RX_P, TX_N, TX_P, RDY_FLT_N, RDY_FLT_P, IN_PWM_N, IN_PWM_P, CLR_FLT_N, CLR_FLT_P, SNS_S, SNS_VCC, HS_LSB, SNS_D, VDD, OUT_EN, C_MC, C_PULSE, C_BLANK, OUT_SSD, OUT_DR2, OUT_DR1, OUT_MC, VDD_OUT, PVDD_PD, PVDD_MC
Bootstrap voltages	BST_DRx_N: BST_DRx_P
Ground voltage group	VSS, PVSS_PD_CAP, PVSS_MC_CAP, PVSS_MC_2, PVSS_MC_1, PVSS_PD_2, PVSS_PD_1



ELECTRICAL SPECIFICATIONS

Unless otherwise stated, specification applies for VCC-VSS=20V and -60°C≤T_j≤230°C.

Parameter	Condition	Min	Typ	Max	Units
Supply Voltage					
VCC-VSS		7		40	V
VDD-VSS	Internally generated from VCC.	4.5		5.5	V
Source of SiC transistor to VSS		0		40	V
Quiescent current consumption	In fault state (no TX/RX active)		5		mA
Internal Linear Voltage Regulator (LDO)					
Total accuracy	7V≤VCC-VSS≤40V, 1mA≤I_{LOAD}≤50mA	-5		+5	%
Load regulation	VCC-VSS=20V, 1mA≤I_{LOAD}≤50mA		-1		%
Line regulation	7V≤VCC-VSS≤40V, I_{LOAD}=25mA		±1		%
Output current	7V≤VCC-VSS≤40V	0		50	mA
Output load capacitance	0.01Ω≤ESR≤0.1Ω	0.33	1	3.3	µF
UVLO (on VCC and SOURCE terminal of SiC versus VSS)					
UVLO threshold accuracy			5		%
UVLO hysteresis			10		%
Internal comparator reference vs. VSS		1.14	1.2	1.26	V
Allowed input current on sense pins.	SNS_VCC and SNS_S			10	mA
Leakage current on sense pins	1.14V≤V_{SNS}≤1.26V			1	µA
Drain Failure Detection (desaturation)					
Protection threshold range vs. SOURCE	VSS=-40V…0V.	1			V
Internal comparator reference vs. VSS		0.45	0.55	0.6	V
Protection threshold accuracy			10		%
Allowed input current on SNS_D pin.				5	mA
SNS_D leakage current	0.45V≤V_{SNS_D}≤0.6V			500	nA
Gate Failure Detection (between SNS_G to SNS_MC)					
Gate current threshold range	R_{SNS_G}=100mΩ.		1.5		A
Gate current threshold accuracy			20		%
Source Failure Detection (over-current protection between SNS_S_P to SNS_S_N)					
Source current threshold range	R_{SNS_S}=10mΩ.		10		A
Source current threshold accuracy			20		%
Driver					
Propagation delay/channel	from IN_PWM_x to driver outputs		200		ns
Rise time	1nF output capacitor per driver channel		15		ns
Fall time	1nF output capacitor per driver channel		15		ns
Minimum ON time t_{ON_min}		1			µs
Minimum OFF time t_{OFF_min}		1			µs
Peak output current of PU_DR1 driver (PU_DR1_1 and PU_DR1_2 shorted)	100nF output capacitor		3		A
Peak output current of PU_DR2 driver (PU_DR2_1 and PU_DR2_2 shorted)	100nF output capacitor		3		A
Continuous output current of DR2_PU (PU_DR2_1 and PU_DR2_2 shorted)	VCC-VSS=7V		0.5		A
Peak output current of PD_DR driver (PD_DR_1 and PD_DR_2 shorted)	100nF output capacitor		3		A
Peak output current of PD_MC driver (PD_MC_1 and PD_MC_2 shorted)	100nF output capacitor		3		A
Soft-shutdown transistor R_{ON}		50	100	150	Ω
Transceiver					
Supply voltage		4.5		5.5	V
Supply current	2 TX/RX, C_{OUT}=50pF, DC=0%...100%	1		20	mA
Carrier frequency			20		MHz
Carrier duty cycle			50		%
Jitter			50		ns
Propagation delay	1 TX + 1 Transformer + 1 RX		120		ns
Maximum data rate			2		Mbps
Common-mode current immunity (see AN-00371-13 for details)				100	mA
TX output resistance (RON)	VDD=5V		15		Ω
RX output buffer V_{OH}	I_{OUT}=8mA	4			V
RX output buffer V_{OL}	I_{OUT}=8mA			1	V

ELECTRICAL SPECIFICATIONS (CONTINUED)

Unless otherwise stated, specification applies for VCC-VSS=20V and -60°C≤T_j≤230°C.

Parameter	Condition	Min	Typ	Max	Units
Control Logic					
Schmitt triggered input					
V_{IH}		4			V
V_{IL}				1	V
Hysteresis			2		V
Blanking time					
Blanking time range	Externally adjusted with a capacitor (100pF…10nF)	0.1		10	µs
Blanking time accuracy	Externally adjusted with a capacitor		20		%
Miller Clamp delay					
Miller Clamp delay range	Externally adjusted with a capacitor (100pF…10nF)	0.1		10	µs
Miller Clamp time accuracy	Externally adjusted with a capacitor		20		%
Pulse width on PU_DR1_1 & PU_DR1_2					
Pulse time range	Externally adjusted with a capacitor (100pF…3.3nF)	0.1		3.3	µs
Pulse time accuracy	Externally adjusted with a capacitor		20		%
Output buffers					
Peak output current (sink and source)	50pF output capacitor	10			mA
V_{OH}	I_{OUT}=8mA	4.1			V
V_{OL}	I_{OUT}=8mA			0.4	V

THEORY OF OPERATION

Introduction

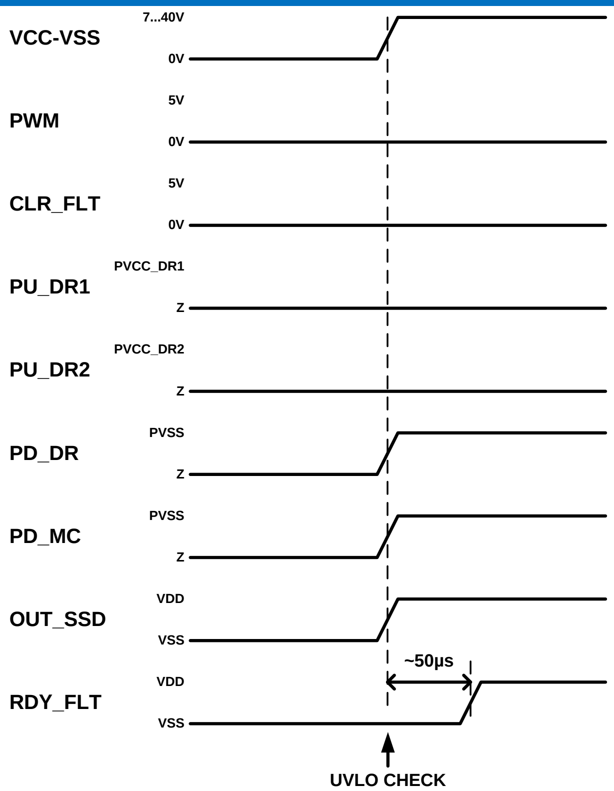
XTR26010 is a high-temperature, high reliability intelligent power transistor driver integrated circuit specifically designed to drive normally-On as well as normally-Off Silicon Carbide (SiC), Gallium Nitride (GaN) and standard silicon power transistors, such as MOSFETs, JFETs, SJTs, BJTs, MESFETs and HEMTs. The XTR26010 features:

- Internal 5V linear regulator.
- Cross-conduction protection between high-side and low-side power drivers.
- 5-channel transceiver (2 TX and 3 RX) for isolated data transmission with the microcontroller and between high side and low side drivers
- Double pull-up gate-drive-channels (PU_DR1 and PU_DR2) capable of sourcing a peak current of 3A with optional pulsed operation of PU_DR1.
- Pull-down gate-drive-channel capable of sinking 3A peak current.
- On-chip programmable delay active Miller clamp (AMC) on PD_MC channel with 3A current capability,
- On-chip soft-shut-down (SSD) capability that slowly shuts down the power transistor in case of fault.
- Independent failure detection on the drain, gate and source terminals of the power transistor.
- Safe start-up through UVLO (Under Voltage Lockout) function.

Operation Phases

Startup phase

The startup phase is initialized by the turn on of the power supplies of the circuit VCC and VSS. The UVLO is checked and if the power supply values are higher than the fixed thresholds and the output gate is close to VSS, an internal counter with a delay of 50µs is started. This delay secures the correct turn-on of the internal voltage reference. During the startup phase the PD_DR and PD_MC drivers outputs are activated for safe normally on start-up, and the input PWM is blanked (If a PWM signal is received, it is not transferred to the driver outputs). At the end of the counter the signal RDY_FLT goes to "1". The circuit enters into the functional phase: if a PWM signal is received, it is transferred to the driver outputs.



Functional phase

The functional phase starts when the RDY_FLT output flags a "1". In this phase, the circuit is ready to receive the PWM signal from the microcontroller.

When the PWM signal turns on, it is transferred after the propagation delay from the IN_PWM input to the PU_DR2 output. For PU_DR1 output, two operation modes are possible:

- Pulsed mode: in this mode a pulse is generated on PU_DR1 output. The pulse width is given by:

$$t_{PULSE}=1k*C_{PULSE}$$

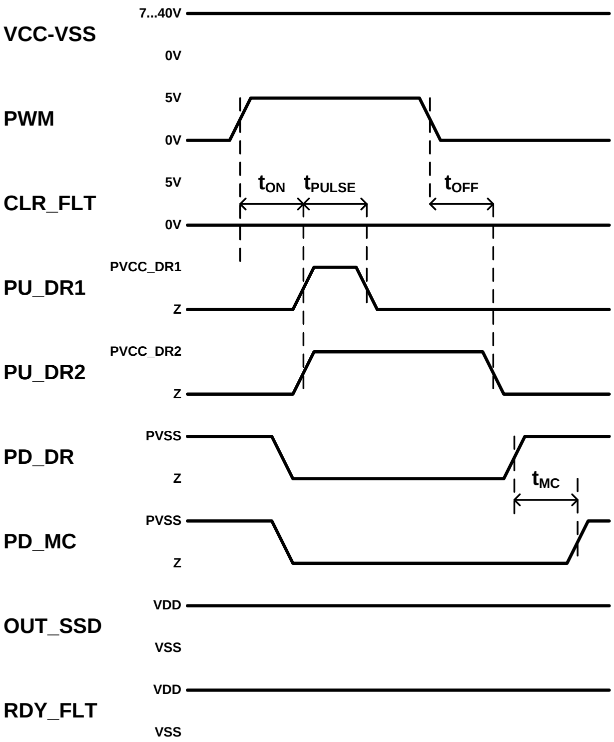
where C_{PULSE} is the external capacitor connected between C_PULSE and VSS pins. This mode is suitable for driving normally-off SiC JFETs and BJTs.

- Normal mode: in this mode the pulse width is equal to the PWM on time. This mode is activated by connecting C_PULSE pin to VDD before turning-on the power supplies.

When the PWM signal turns-off, the PD_DR driver is turned-on after the propagation delay t_{OFF}, while the PD_MC driver is turned-on after $t_{OFF}+t_{MC}$, where t_{MC} is the Active Miller Clamp delay given by:

$$t_{MC}=1k^{*} C_{MC}$$

where C_{MC} is the external capacitor connected between C_MC and VSS pins.



Fault phase

The fault phase is initialized if at least one of the following signals flags an error:

- UVLO on VCC supply versus VSS.
- UVLO on SOURCE node versus VSS.
- Desaturation detection on the DRAIN terminal of the power transistor.
- Over-current detection on the GATE terminal of the power transistor.
- Over-current detection on the SOURCE terminal of the power transistor.

The UVLO error is checked permanently during the functional phase of the circuit, while the other failures are checked when the PWM signal is turned-on and outside the blanking time t_{BLANK} given by:

$$t_{BLANK}=1k^{*}C_{BLANK}$$

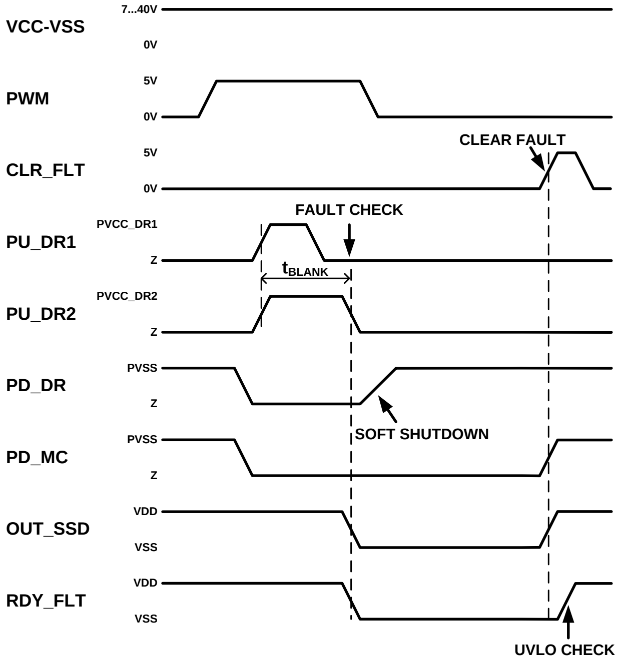
where C_{BLANK} is the external capacitor connected between C_BLANK and VSS pins.

Immediately after fault detection, RDY_FLT goes to “0”, and this information is sent to the microcontroller through the TX_RDY_FLT transmitter. Then, the PU_DR1, PU_DR2, and PD_DR drivers are turned-off and the Soft Shut-Down driver is turned-on. This slowly turns-off the power transistor to avoid high dV/dt and high turn-off current.

To get out from this state, two alternatives are possible:

- A permanent 1 on CLR_FLT pin. In this case, after a time-out of 100µs, the startup counter is reset initializing a new startup phase.
- A rising edge on CLR_FLT pin. This also results in a new startup phase that starts immediately with no time-out.

It should be noted that the CLR_FLT pin can be used as a reset pin for the circuit. Indeed, even when no fault is detected, a rising edge on CLR_FLT initializes a new startup phase.



Functional Features

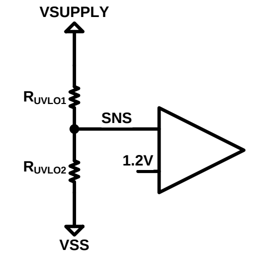
Cross conduction protection

The cross conduction protection has been implemented to prevent short-circuiting the high voltage power supply through the High Side (HS) and Low Side (LS) power transistors of a half bridge. This is achieved through a bidirectional isolated data communication between the XTR26010 set as a HS driver and the XTR26010 set as a LS driver of the half bridge. The XTR26010 LS is the master and the XTR26010 HS is the slave. When the PWM_LS signal turns-on, the TX_XCOND_LS sends a “0” to the RX_XCOND_HS forcing it to turn-off its PU_DR1/PU_DR2 and to turns-on the PD_DR and then the PD_MC. After checking that the gate of the HS power transistor is nearly discharged using the SNS_MC_HS sense pin, the TX_XCOND_HS sends a “1” to RX_XCOND_LS telling that the HS is off and that the LS can safely turn-on. Then, the PU_DR1/PU_DR2 LS are turned-on. When the PWM_LS signal turns-off, the LS turn-off its PU_DR1/PU_DR2 and turns-on its PD_DR and then its PD_MC. After checking that the gate of the LS power transistor is nearly discharged using the SNS_MC_LS sense pin, the TX_XCOND_LS sends a “1” to the RX_XCOND_HS telling that the HS can turn-on if his PWM_HS signal is turned-on.

The cross conduction protection can be disabled if the user wishes to manage it externally. To do this both the HS and LS drivers must be set as slave (HS_LSB pin connected to VDD) and the RX_XCOND must receive a “1” (RX_P connected to VDD and RX_N connected to VSS).

Under Voltage Lockout (UVLO) operation

The UVLO block checks the value of the external power supplies (VCC-VSS, SOURCE-VSS), and the internally or externally generated VDD supply (5V versus VSS). A fraction of VDD value is compared to an internal reference of 1.2V versus VSS and an UVLO_VDD flag is set to “1” when the VDD reaches 90% of its expected value. For the external power supplies, the UVLO block compares an externally fixed threshold through a resistor divider to an internal reference of 1.2V versus VSS:



To simplify the equation for the computation of the UVLO threshold voltage V_{TH_UVLO}, we consider VSS=0V. The V_{TH_UVLO} is obtained in terms of R_{UVLO1} and R_{UVLO2} as follows:

$$V_{TH\_UVLO}=\frac{R_{UVLO1}+R_{UVLO2}}{R_{UVLO2}}\cdot 1.2V$$

The current that can be tolerated (100µA for example, it must be high enough compared to leakage current) in the resistor divider can give the value of R_{UVLO2} using:

$$R_{UVLO2}=\frac{1.2V}{100\mu A}=12k\Omega$$

Then, for V_{TH_UVLO}=15V, the R_{UVLO1} is obtained:

$$R_{UVLO1}=\left(\frac{V_{TH\_UVLO}}{1.2}-1\right)\cdot R_{UVLO2}=138k\Omega$$

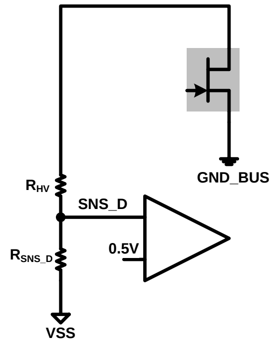
The SNS_VCC/SNS_S pins are internally clamped to 2.8V with a maximum current sink of 10mA.

Protect operation

The protect block is responsible for the detection of a bad operation on the three terminals of the power transistor.

Drain failure detection (desaturation)

When the power transistor is turned-on, the voltage on its drain must be very close to the voltage on its source. If this is not the case, a drain failure is detected using the circuits sketched below:



To simplify the equation for the computation of the desaturation threshold voltage V_{TH_DESAT}, we consider VSS=0V. The desaturation detection threshold V_{TH_DESAT} is then given by

$$V_{TH\_DESAT}=\frac{R_{HV}+R_{SNS\_D}}{R_{SNS\_D}}\cdot 0.5V$$

The current that can be tolerated (1mA for example, it must be high enough compared to leakage current) in the resistor divider can give the value of R_{HV} which sees the high voltage (1200V):

$$R_{HV}=\frac{1200V}{1mA}=1.2M\Omega$$

Then, for V_{TH_DESAT}=15V, the R_{SNS_D} is obtained:

$$R_{SNS\_D}=\left(\frac{0.5}{V_{TH\_DESAT}-0.5}\right)\cdot R_{HV}=41.4k\Omega$$

The SNS_D pin is internally clamped to 1.4V versus VSS pin with a maximum current sink of 5mA. The parasitic capacitors on this pin must be minimized as it is proportional to the current that can be tolerated in the resistor divider. This current must be high enough to quickly charge the parasitic capacitor. This charging time defines the desaturation detection delay after the blanking time. During the blanking time, the SNS_D pin is forced to VSS to insure no fault detection during the blanking time.

Gate over-current detection

When the power transistor is turned-on, the gate current is measured using the differential voltage between SNS_G and SNS_MC and compared to a threshold fixed by the sense resistor R_{SNS_G}. In the case of damage on the gate, the current should be higher than the fixed threshold indicating gate failure for the circuit. The gate over-current threshold is given by:

$$I_{TH\_G}=\frac{150mV}{R_{SNS\_G}}$$

It should be noted that gate over-current protection is not active only when the PWM signal is ON and if the VCC is lower than 0V. In this case, the UVLO protection is active and allows to protect the circuit in case of short-circuit between gate and source.

Source over-current detection

When the power transistor is turned-on, the source current is measured using the differential voltage between SNS_S_P and SNS_S_MC and compared to a threshold fixed by the sense resistor R_{SNS_S}. In the case of damage on the source, the current should be higher than the fixed threshold indicating source failure for the circuit. The source over-current threshold is given by:

$$I_{TH\_S}=\frac{100mV}{R_{SNS\_S}}$$

For correct operation of the source over-current detection, a minimum voltage of 5V is need between GND_BUS and VSS. If for a given application this is not possible to fulfill, the over-current detection can be disabled by shorting both SNS_S_P and SNS_S_N to VDD.

Bootstrap capacitors

The bootstrap capacitor value can be selected taking into account two conditions:

- It should be high enough to supply the PU_DRx buffer and to charge the gate capacitor of the PU transistors to maintain it on for a given on time. A rule of thumb here is to take at least 100 times the gate capacitor which is in the order of 300pF. This gives as a first guess 30nF for the C_{BST} (see figure below).
- The bootstrap capacitor C_{BST} is charged for the first time during the startup time given by the rise time of the power supply and the 50µs delay fixed by the startup counter. The charging path is, as described in the figure bellow with the red arrows, going from the 5V versus VSS power supply PVDD via the integrated bootstrap diode, then the external R_{PU}, and finally the PD_MC driver. During operation, C_{BST} is charged through the resistor R_{PU} during the t_{OFF}-t_{MC} where t_{OFF} is the off time of the PWM signal and t_{MC} is the Miller Clamp time given by the external capacitor C_{MC}. Hence, C_{BST} must fulfill the following condition:

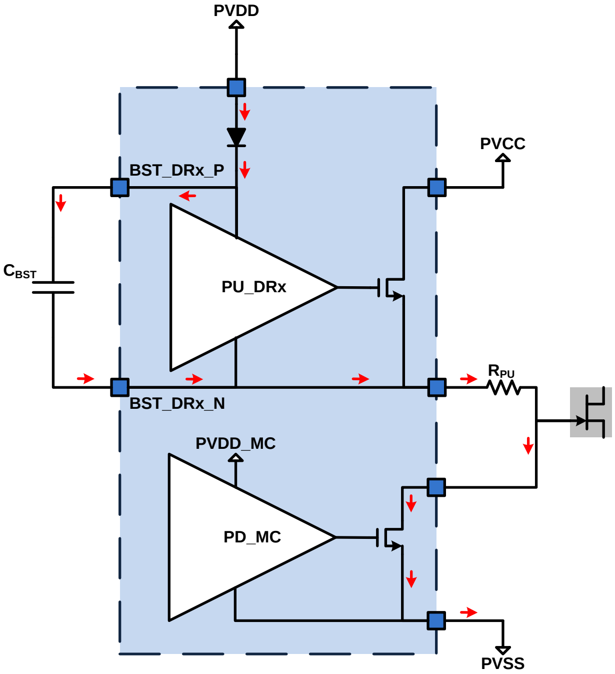
  $$C_{BST} > (Iq+C_{eq}*VCC*fr)*t_{ON}/V_{BST\_ripple}/$$

  where Iq=250µA is the quiescent current delivered from BST_DRx_P to the pull-up driver, C_{eq}≈500pF is the equivalent capacitor that must be charged by BST_DRx_P up to the voltage VCC, fr is the PWM frequency, V_{BST_ripple} is the peak to peak voltage between BST_DRx_P and BST_DRx_N during the ON time t_{ON}. For VCC=40V, fr=100kHz, V_{BST_ripple}=400mV, and t_{ON}=9µs (t_{OFF}=1µs), C_{BST} must be higher than 50.6nF (100nF is recommended with a lower limit of 10nF).

The integrated charge pump has been designed to be able to maintain the on state permanently (PWM DTC 100%). It is not able to charge the bootstrap capacitor when the PWM signal is switching. In this case the R_PU must satisfy the following condition:

$$R_{PU} < fr*t_{OFF}*(VDD-V_{TD}-V_{BST\_mean})/(Iq+C_{eq}*VCC*fr)$$

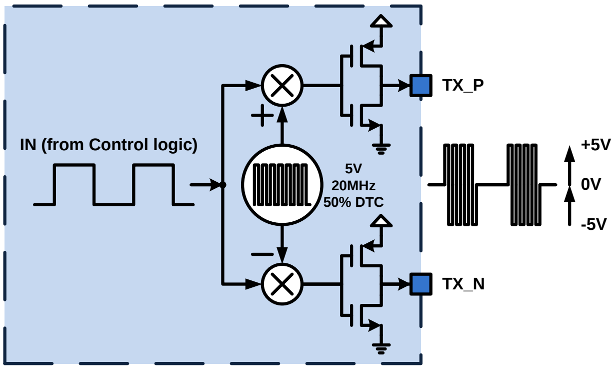
where VDD is the 5V supply generated by the internal voltage regulator, V_{TD}=0.7V is the threshold voltage of the bootstrap diode, and V_{BST_mean} is the average value of the voltage between BST_DRx_P and BST_DRx_N. For fr=100kHz, t_{OFF}=1µs, VDD=5V, V_{TD}=0.7V, V_{BST_mean}=3.8V, Iq=250µA, C_{eq}=500pF, VCC=40V, R_{PU} must be lower than 22.22Ω



Transceiver
The XTR26010 implements a 5-channel isolated data transceiver with 2 transmitters (TX_XCOND and TX_RDY_FLT) and 3 receivers (RX_XCOND, RX_PWM, and RX_CLR_FLT). The galvanic isolation is achieved by an external magnetic transformer for each channel signal.
In the following sections, only one transmitter and one receiver will be described, and thus, the pin index 1,2 will be omitted for simplicity.

TX operation
The transmitter is composed of the following functions (as shown in the figure below):

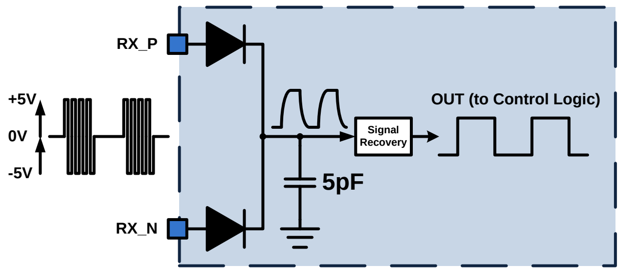
- Oscillator: This block generates a clock with typical oscillation frequency of 20MHz.
- Modulator: This block implements a classical On-Off Keying (OOK) modulation using the clock generated by the oscillator and the digital input signal coming from the control logic block. If a digital "1" is sent to the input of the transmitter, it will be transferred as a differential ±5V versus **VSS** at the output pins **TX_P/TX_N**. On the other hand, a digital "0" is transferred as a 0V versus **VSS** at the output pins **TX_P/TX_N** of the transmitter.
- The output buffer: It consists of several inverters with a typical R_{ON} of 10Ω for the last stage (NMOS or PMOS). This buffer is driven by two complementary signals generated by the modulator. These signals have a duty cycle very close to 50% to guarantee no DC current in the primary inductance of the pulse transformer. This DC current can induce a magnetic field that could saturate the magnetic core and compromise the data transfer.



Transmitter truth table

IN (from Control Logic)	TX_P	TX_N
0	0	0
1	CK	/CK

RX operation
The receiver implements a classical full-wave rectification to demodulate the signal received on the pulse transformer secondary winding (as shown in the figure below). The signal recovery block aims to ensure immunity versus possible high dv/dt, which induces common mode current from one side of the pulse transformer to the other side. This common mode current can induce errors in the data transmission from the transmitter side to the receiver side. When a dv/dt event happens, it is detected by this block. During the dv/dt event the output data is kept at its value just before the dv/dt event. After the dv/dt event, the input data is transferred to the output.



Receiver truth table

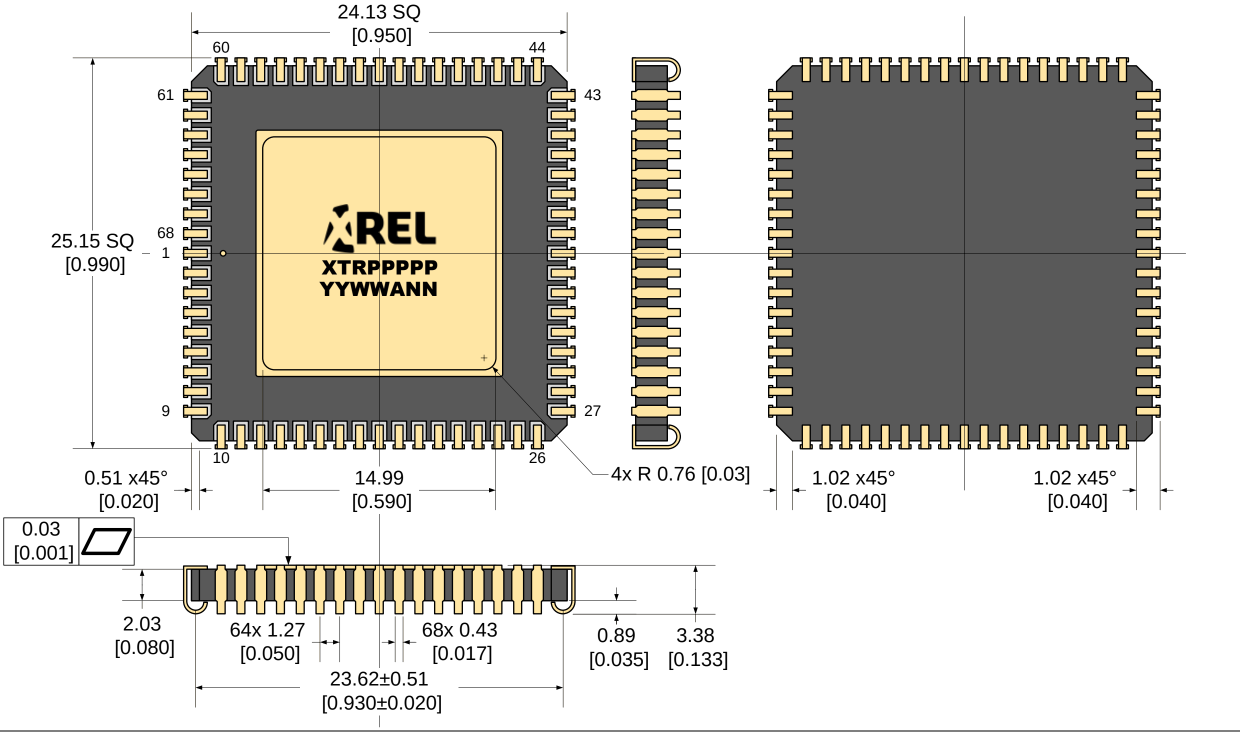
RX_P	RX_N	OUT (to Contol Logic)
0	0	0
CK	/CK	1
0	1	1
1	0	1
1	1	**forbidden**

Plulse transformer
The pulse transformer specifications and design guidelines are given in the application note "Pulse Transformer Design Guidelines" (AN-00371-13).

PACKAGE OUTLINES

Dimensions shown in mm [inches].

J-Formed Leaded Chip Carrier LJCC68



Part Marking Convention	
Part Reference: XTRPPPPPP	
XTR	X-REL Semiconductor, high-temperature, high-reliability product (XTRM Series).
PPPPP	Part number (0-9, A-Z).
Unique Lot Assembly Code: YYWWANN	
YY	Two last digits of assembly year (e.g. 11 = 2011).
WW	Assembly week (01 to 52).
A	Assembly location code.
NN	Assembly lot code (01 to 99).

IMPORTANT NOTICE & DISCLAIMER

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