Marconi
Electronic Devices

MA28137

Radiation Hard Programmable DMA Controller

FEATURES

- Radiation hard to 1 MRad (Si)
- High SEU immunity, latch-up free
- CMOS Silicon-on-Sapphire Technology
- All inputs & outputs fully TTL & CMOS compatible
- MIL-STD-1750A MAS281 compatible
- Four independent DMA channels
- Independent autoinitialization of all channels
- Enable/Disable control of individual DMA requests
- Memory-to-memory transfers
- Memory block initialization

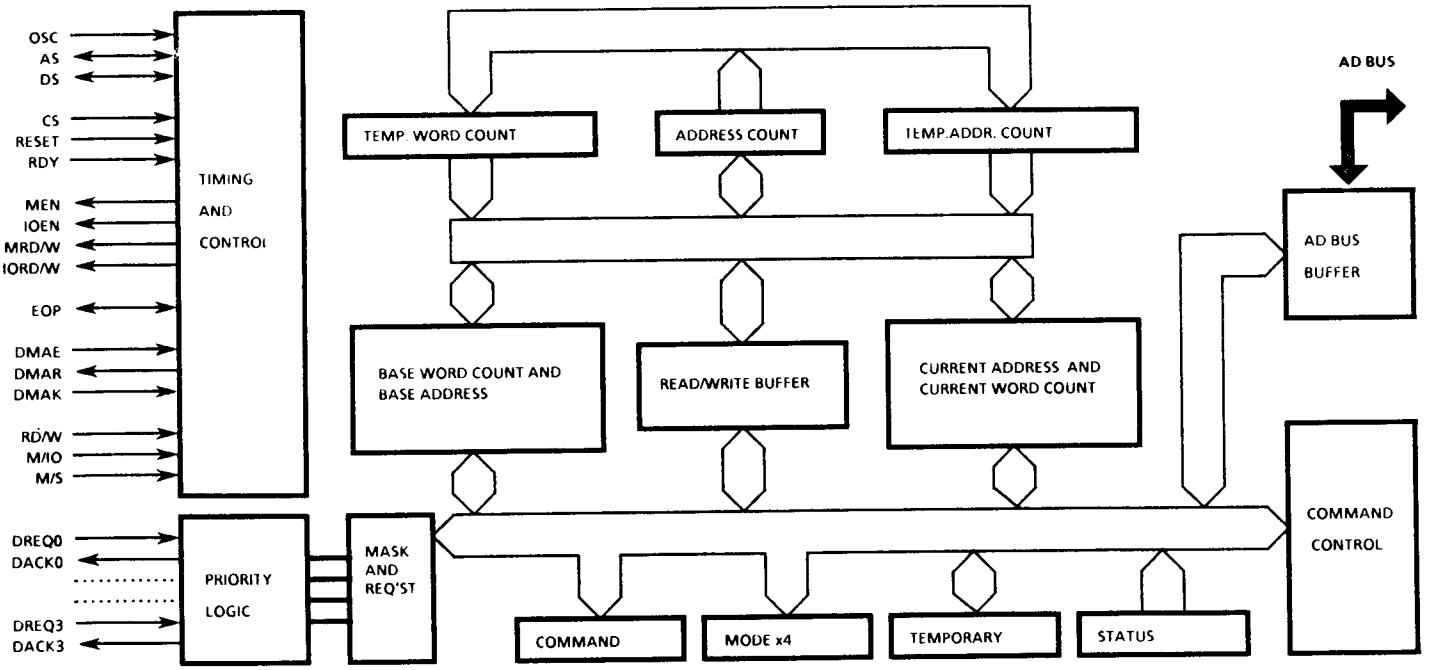
GENERAL DESCRIPTION

The MA28137 Direct Memory Access (DMA) controller is a peripheral interface circuit designed for MAS281-based microprocessor systems. It enhances system performance by allowing external devices to directly transfer information to and from the system memory. Memory-to-memory transfer capability is also provided. The MA28137 offers a wide variety of programmable control features to enhance system optimization and to allow dynamic reconfiguration under program control.

The four independent channels may be expanded by cascading additional controller chips. Each channel has a full 64K address and word count capability and can be individually programmed to autoinitialize to its original condition following an End of Process (EOP).Three basic transfer modes are offered.

The device will support a Memory Management Unit (MMU) for extended addressing to 1M words.

BLOCK DIAGRAM



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MA28137

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PIN DESCRIPTION

SIG.	FUNCTION	DESCRIPTION
V_{DD}	Power	+ 5 volt supply
V_{SS}	Ground	Ground
OSC	Clock Input	Controls the internal operations of the MA28137 and its rate of data transfer. The input may be driven at up to 20MHz.
RDY	Ready	Ready is an input used to extend the memory read and write pulses from the MA28137 to accommodate slow memories or I/O peripheral devices.
DMAE	DMA Enable	The active high DMA enable signal from the Central Processing Unit (CPU) indicates that DMA requests from the controller will be acknowledged.
DMAK	DMA Acknowledge	The active low DMA Acknowledge from the CPU indicates that it has relinquished control of the system busses.
DMAR	DMA Request	This is the DMA requests to the CPU and is used to request control of the system bus. If the corresponding mask bit is clear, the presence of any valid DMA request causes DMA to issue the DMAR to the processor. After DMAR goes active at least one clock cycle must occur before DMAK goes active
AD00-AD15	Address/data bus	System address and data transfer
DS	Data Strobe	When DMAK is high, the DS signal is generated by the system processor. When the DMAK line is low, the DMA controller produces this signal. In both cases the rising edge of DS indicates that valid data is present on the AD bus.
AS	Address Strobe	This signal functions in a similar way to DS, except that its falling edge indicates the presence of a valid address on the AD bus.
CS	Chip Select	Chip select is an active low input used to select the MA28137 as an I.O device during the idle cycle. This allows CPU communication on the data bus.
RESET	Reset	Reset is an active high input which clears the command status. request and temporary registers. and sets the mask register. Following a reset the device is in the idle cycle.

SIG.	FUNCTION	DESCRIPTION
DREQ 0-3	DMA Request	The DMA request lines are individual asynchronous channel request inputs used by peripheral circuits to obtain DMA service. In fixed priority, DREQ0 has the highest priority and DREQ3 has the lowest priority. A request is generated by activating the DREQ line of channel. DACK will acknowledge the recognition of DREQ signal. Polarity of DREQ must be maintained until the corresponding DACK goes active.
DACK 0-3	DMA Acknowledge	DMA Acknowledge is used to notify the individual peripherals when one has been granted a DMA cycle. The sense of these lines is programmable. Reset initializes them to be active low.
EOP	End of Process	End of process is an active low bidirectional signal. Information concerning the completion of DMA services is available at the bidirectional EOP pin. The MA28137 allows an external EOP signal to terminate an active DMA service. This is accomplished by pulling the EOP signal low. The MA28137 also generates a pulse when the terminal count (TC) for an channel is reached. This generates an EOP signal which is output through the EOP line. The reception of EOP, either internal of external, will cause the MA28137 to terminate the service, reset the request, and, if Autoinitialize is enabled, to write the base registers of that channel. The mask bit and TC bit in the status word will be set for the currently active channel by EOP unless the channel is programmed for autoinitialize. In that case, the mask bit remains clear. During memory-to-memory transfers, EOP will be output when the TC for channel 1 occurs. EOP should be tied high with a pull-up resistor if it is not used to prevent erroneous end of process inputs.
RD/W	Read/Write	Indicates direction of data flow to and from the microprocessor. A logic '1' signifies a read by the processor.
M/IO	Memory or I/O	This is an input from the MAS281 and indicates the type of instruction currently being executed by the processor.

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SIG.	FUNCTION	DESCRIPTION
MEN	Memory Enable	When low, this signal indicates that the system memory is to be accessed.
IOEN	Input/Output Enable	When low, this signal indicates that the system I/O is to be accessed.
MRD/W	Memory Read/Write	This line defines the direction of data transfer to and from the system memory. A logic 1 implies a read from memory, logic 0 a write to memory.
IORD/W	Input/Output Read/Write	This line defines the direction of data transfer to and from the system I/O. A logic 1 implies a read from I/O, logic 0 a write to I/O.
M/S	Master/Slave mode	When this line is set to a logical 1 and no DMAK has been issued the controller is in master mode and will generate the system control signals MEN, IOEN, MRD/W and IORD/W from the incoming signals M/IO and RD/W. A logical 0 places these outputs in a high impedance state, allowing another controller to assert these lines. See the section on cascade mode for further information.
AS0-AS3	Address status	Used by an MMU during expanded memory access to define the page register set used during DMA transfers.
PS0-PS3	Process status	Used by an MMU during expanded memory access to provide page access protection during DMA transfers.
IN/OP	Instruction/ Operation	Used with an MMU to select the correct page register set.

NAME	SIZE	NUMBER
Base Address Registers	16 bits	4
Base Word Count Registers	16 bits	4
Current address registers	16 bits	4
Current word count registers	16 bits	4
Temporary address register	16 bits	1
Temporary word count register	16 bits	1
Status register	8 bits	1
MMU status register	9 bits	4
Command register	8 bits	1
Temporary register	8 bits	1
Mode registers	6 bits	4
Mask register	4 bits	1
Request register	4 bits	1

FUNCTIONAL DESCRIPTION

The MA28137 block diagram shown on page 1, includes the major logic blocks and internal registers. The data interconnection paths are also shown. Not shown are the various control signals between the blocks.

The MA28137 contains a number of registers which are accessible to the CPU and which define the way in which DMA transfers are to take place. A detailed description of the registers and their functions can be found under register description.

The MA28137 contains three basic blocks of control logic. The timing control block generates internal timing and external control signals for the MA28137. The program command control block decodes the various commands given to the MA28137 by the microprocessor prior to servicing the DMA request. It also decodes the mode control word used to select the type of DMA during the servicing. The priority encoder block resolves priority contention betwen DMA channels requesting service simultaneously.

DMA Operation

The MA28137 is designed to operate in two major cycles. These are called idle and active cycle. Each device cycle is made up of a number of states. The MA28137 can assume seven separate states, each composed of one full clock period.

State 1 (S1) is the inactive state. It is entered when the MA28137 has no valid DMA requests pending. While in State S1, the DMA requests controller is inactive but may be in the program condition, being programmed by the processor.

State S0 is the first state of DMA service. The MA28137 has requested a hold but the processor has not yet returned an acknowledge. The MA28137 may still be programmed until it receives DMAK from the CPU. An acknowledge from the CPU will signal that DMA transfers may begin.

S1, S2,S3 and S4 are the working states of the DMA service. If more time is needed to complete a transfer that is available with normal timing, wait states can be inserted between S2 or S3 and S4 by the use of the ready line on the MA28137.

Note that the data is transferred directly from the I/O device to memory (or vice versa). Memory to memory transfers require a read-from and a write-to memory to complete each transfer. The data is not read into or driven out of the MA28137 in I/O to-memory or memory-to-I/O DMA transfers.The states, which resemble the normal working states use two digit numbers for identification.

Eight states are required for a single transfer. The first four states (S11, S12, S13, S,14) are used for the read-from-memory half and the last four states (S21, S22,S23,S24) for the write-to-memory half of the transfer.

Idle Cycle

When no channel is requesting service the MA28137 will enter the idle cycle and perform "S1" states. In this cycle the MA28137 will sample the DREQ lines every clock cycle to determine if any channel is requesting a DMA service. The device will also sample CS, looking for an attempt by the microprocessor to write or read the internal registers of the MA28137.

When CS is low and DMAK is high, the MA28137 enters the program condition. The CPU can now establish, change or inspect the internal definition of the device by reading from or writing to the internal registers. The four low-order address/data lines, AD15-AD12, select which register is to be accessed. The RD/W and DS lines are used to select and time reads or writes.

There are two special software commands which can be executed by the MA28137 in the program condition. These commands are decoded as sets of address with CS and RD/W. The commands, which include master clear, do not make use of the data bus.

Active Cycle

When the MA28137 is in the idle cycle and a non-masked channel requests a DMA service, the device will output a DMAR to the microprocessor and enter the active cycle. It is in this cycle that the DMA service will take place, in one of four modes.

Single Transfer Mode - In single transfer mode the device is programmed to make one transfer only. The word count will be decremented and the address decremented or incremented following each transfer. When the word count "rolls over" from zero the $FFFF_H$, a Terminal Count (TC) will cause an autoinitialize if the channel has been programmed to do so.DREQ must be held active until DACK becomes active in order to be recognised.

If DREQ is held active throughout the single transfer, DMAR will go inactive and release the bus to the system. It will again go active and, upon receipt of a new DMAK another single transfer will be performed.

Block Transfer Mode - In block transfer mode the device is activated by DREQ to continue making transfers during the service until a TC, caused by the word count going to $FFFF_H$, or an external end of process is encountered. DREQ need only be held active until DACK becomes active. Again an autoinitialization will occur at the end of the service if the channel has been programmed for it.

Demand Transfer Mode - In demand transfer mode the device is programmed to continue making transfers until a TC or external EOP is encountered or until DREQ goes inactive. Thus transfers may continue until the I/O device has exhausted its data capacity.

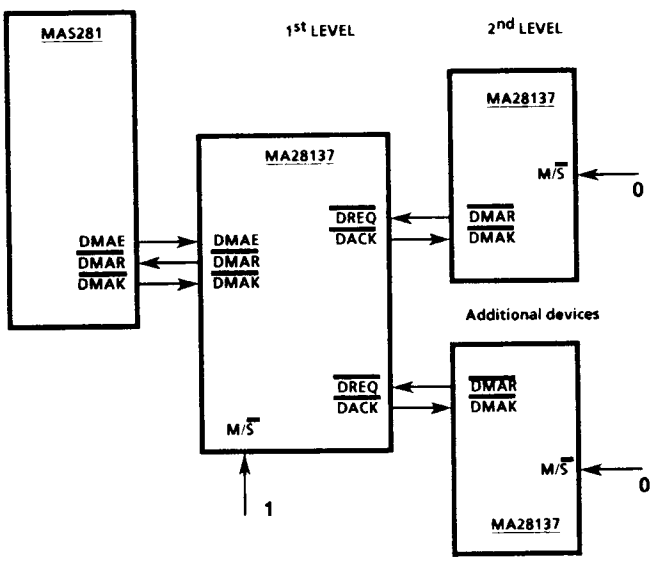
After the I/O device has had a chance to catch up, the DMA service is re-established by means of a DREQ. During the time between services when the microprocessor is allowed to operate, the intermediate values of address and word count are stored in the MA28137. Current address and current word count registers. Only an EOP can cause an autoinitialize at the end of the service: EOP is generated either by TC or by an external signal.

Cascade Mode - This mode is used to cascade more than one MA28137 together for simple system expansion. The DMAR and DMAK signals from the additional controller are connected to the DREQ and DACK signals of a channel on the initial MA28137. This allows the DMA requests of the additional device to propagate through the priority network circuitry of the processing device. The priority chain is preserved and the new device must wait for its turn to acknowledge requests.

In a system with only one DMA controller, the controller generates the system control signals MEN, IOEN, MRD/W and IORD/W from the incoming signals M/IO and RD/W during periods when DMAK is high (i.e. no transfers occurring). This allows the same control signals to be used during both DMA and non-DMA modes.In a multi-level DMA system during non-DMA periods only one controller must generate the four system control lines, to prevent contention. The master/slave (M/S) pin enables (master) or disables (slave) the generation of these control lines during non-DMA mode and allows one level 1 controller to be designated a master (with all other controllers as slaves).

The cascade channel of the initial MA28137 is used only for prioritizing the additional device, it does not produce any address or control signals of its own. These could conflict with the outputs of the active channel in the added device. The MA28137 will respond to DREQ and DACK but all other output except DMAR will be disabled.

The diagram below shows two additional devices cascaded into an initial device using two of its channels. This forms a two level DMA system. More MA28137s could be added at the second level by using the remaining channels of the first level. Additional devices can also be added by cascading into the channels of the second level devices, forming a third level.



Transfer Types - Each of the three active transfer modes can perform three different types of transfer. These are read, write and verify.

Write transfers move data from an I/O device to memory by making MRD/W low,IOR/W high and toggling DS. Similarly read transfers move data from memory to an I/O device by making MRD/W high, IORD/W low and toggling DS.

Verify transfers are pseudo transfers. The MA28137 operates as in read or write transfers generating addresses and responding to EOP, etc. However, the memory and I/O control lines all remain inactive. Verify mode is not permitted during memory to memory operation.

Memory-to-Memory - To perform block moves of data from one area of memory to another with a minimum of program effort and time, the MA28137 includes a memory-to-memory transfer feature. Programming a bit in the command register selects channels 0 and 1 to operate as memory-to-memory transfer channels. The transfer is initiated by setting the software DREQ for channel 0. The MA28137 requests a DMA service in the normal manner. After DMAK is true, the device, using

eight-state transfers in block transfer mode, reads data from the memory. The channel 0 current address register is the source for the address used and is decremented or incremented in the normal manner. The data byte read from the memory is stored in the MA28137 internal temporary register. Channel 1 then writes the data from the temporary register to memory using the address in its current address register and incrementing or decrementing it in the normal manner. The channel 1 current word count is decremented. When the word count of channel 1 becomes equal to $FFFF_H$, a TC is generated causing an EOP output terminating the service.

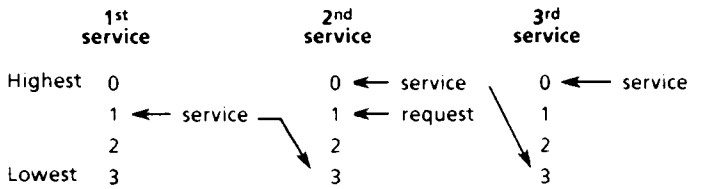
Channel 0 may be programmed to retain the same address for all transfers. This allows a single word to be written to a block of memory.The MA28137 will respond to external EOP signals during memory-to-memory transfers. Data comparators in block search schemes may use this input to terminate the service when a match is found. Memory-to-memory operations can be detected as an active AS with no DACK outputs.

Autoinitialize - By programming a bit in the mode register a channel may be set up as an autoinitialize channel. During autoinitialize, the original values of the current address and current word count registers are automatically restored from the base address and base word count registers of that channel following EOP. The base registers are loaded simultaneously with the current registers by the microprocessor and remain unchanged throughout the DMA service. The mask bit is not set when the channel is in autoinitialize. Following autoinitialize the channel is ready to perform another DMA service, without CPU intervention, as soon as a valid DREQ is detected.

Priority - The MA28137 has two types of priority encoding available as software selectable options. The first is fixed priority which fixes the channels in priority order based upon the descending value of their number. The channel

with the lowest priority is 3 followed by 2, 1 and the highest priority channel 0. After the recognition of any one channel for service, the other channels are prevented from interfering with that service until it is completed.

The second scheme is rotating priority. The last channel to get service becomes the lowest priority channel with the others rotating accordingly. With rotating priority in a single chip DMA system any device requesting service is guaranteed to be recognised after no more than three higher priority services have occurred. This prevents any one channel from monopolizing the system.



REGISTER DESCRIPTION

Current Address Register - Each channel has a 16-bit current address register. This register holds the value of the address used during DMA transfers. The address is automatically incremented or decremented after each transfer and the intermediate values of the address are stored in the current address register during the transfer. This register is restored to its original value by an autoinitialize. Autoinitialize takes place only after an EOP.

Current Word Register - Each channel has a 16-bit current word count register. This register determines the number of transfers to be performed. The actual number of transfers will be one more than the number programmed in the current word count register (i.e. programming a count of 100 will result in 101 transfers).

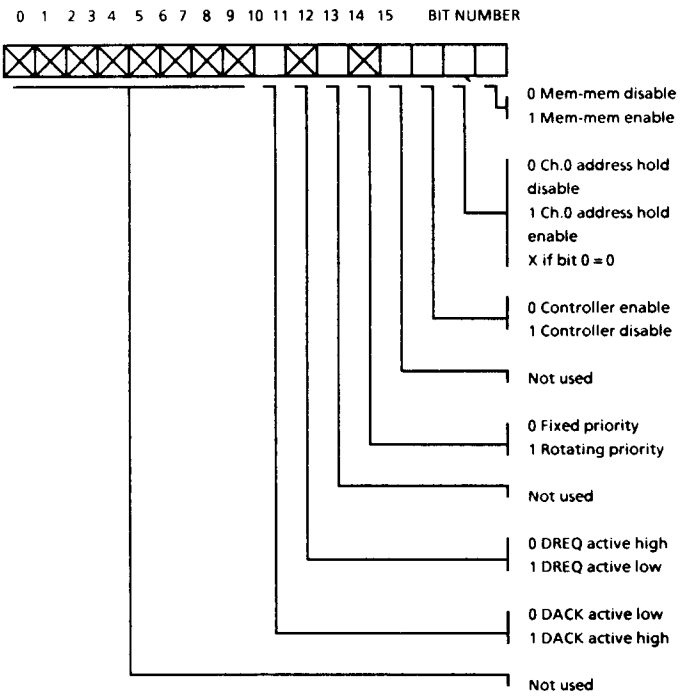
The word count is decremented after each transfer. The intermediate value of the word count is stored in the register during the transfer. When the value in the register goes from zero to $FFFF_H$, a TC will be generated. Following the end of a DMA service it may also be reinitialized by an autoinitialization back to its original value,however, this may only occur when an EOP occurs. If it is not autoinitialized this register will have a count of $FFFF_H$ after TC.

Base Address and Base Word Count Registers - Each channel has a pair of base address and base word count registers. These 16-bit registers store the original value of their associated current registers. During autoinitialize

these values are used to restore the current registers to their original values. The base registers are written simultaneously with their corresponding current register. These registers cannot be read by the microprocessor.

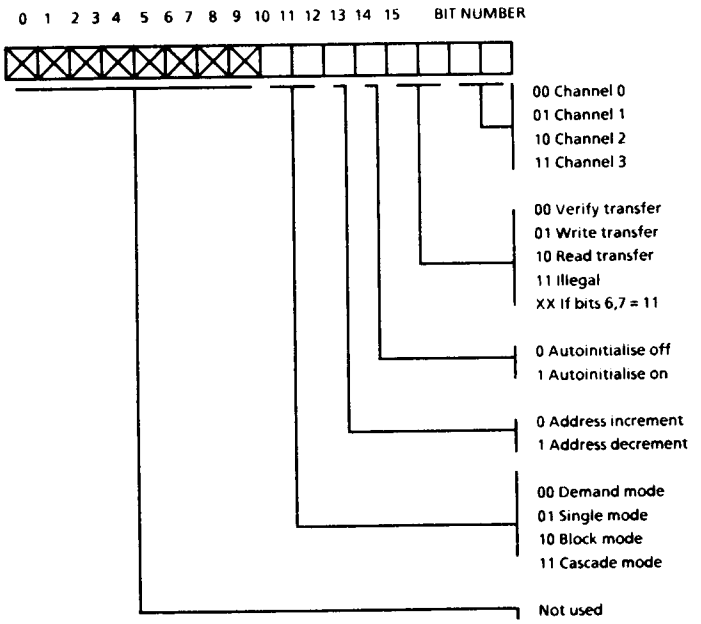
Command Register - This 8-bit register controls the operation of the MA28137. It is programmed by the microprocessor in the program condition and is cleared by reset or a master clear instruction. The following table lists the function of the command bits.

Command register



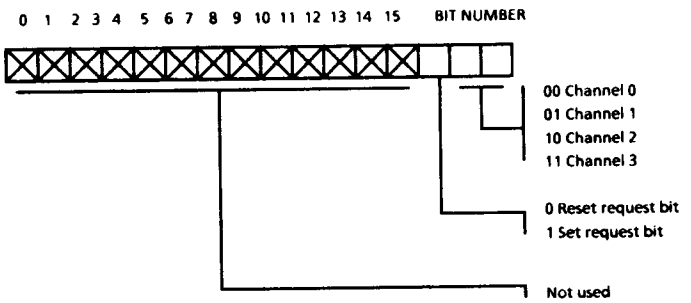
Mode Register - Each channel has a 6-bit mode register associated with it. When the register is being written to by the microprocessor in the program condition, bits 0 and 1 determine which channel mode register is to be written.

Mode register



Request Register - The MA28137 can respond to requests for DMA service which are initiated by software as well as by a DREQ. Each channel has a request bit associated with it in the 4-bit request register. These are non-maskable and subject to prioritization by the priority encoder network, Each register bit is set or reset separately under software control or is cleared upon generation of a TC or external EOP. The entire register is cleared by a reset. To set or reset a bit, the software loads the proper form of the data word. In order to make a software request, the channel must be in block mode.

Request register

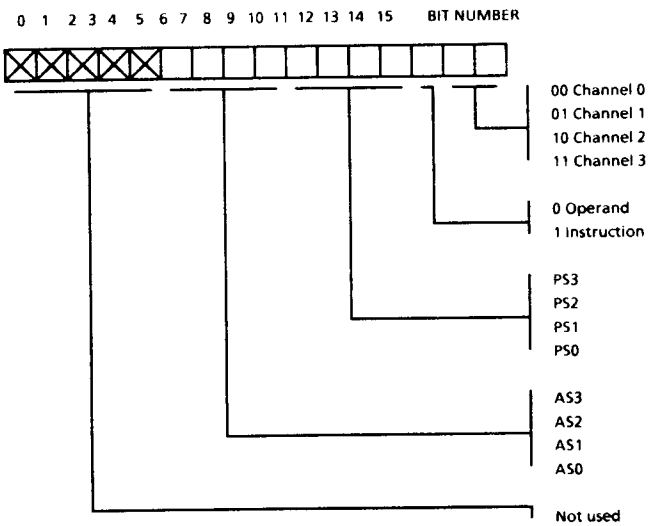


MMU Status Register - Each channel has associated with it a 9-bit register which holds process and address status information for user by an MMU. During DMA transfer, the contents of this register are placed on the lines AS0-3.

PS0-3 to allow the correct memory page to be selected and accessed. In addition, the signal IN/OP is produced to select the instruction or operand page register set. The entire register is cleared by a reset.

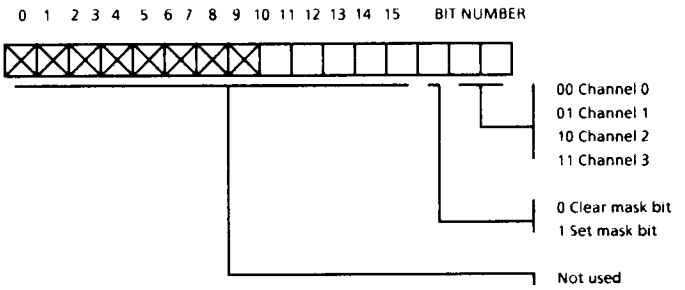
During memory to I/O or I/O to memory transfers, the AS and PS fields associated with the selected channel are placed on the appropriate output lines. During memory-memory transfer the AS and PS fields alternate between those programmed into channels 0 and 1 to allow transfers between different address states.

MMU status register

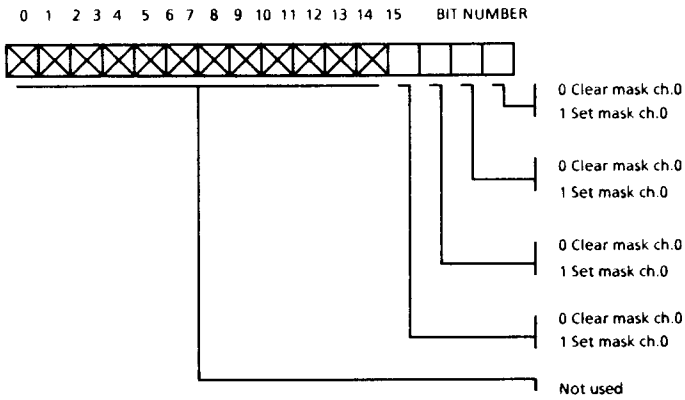


Mask Register - Each channel has a mask bit which can be set to disable the incoming DREQ. Each mask bit is set when its associated channel produces an EOP if the channel is not programmed for autoinitialize. Each bit of the 4 -bit mask register may also be set or cleared separately under software control. The entire register is also set by a reset. This disables all DMA requests until a clear mask register instruction allows them to occur. The instruction to separately set or clear the mask bits is similar in form to that used with the request register.
All four bits of the mask register may also be written with a single command.

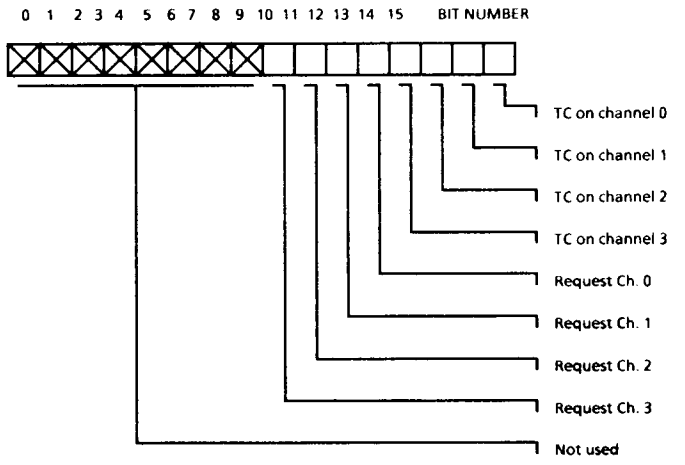
Mask register



Mask register 4-bit write



Status register



Status Register - The status register is available to be read out of the MA28137 by the microprocessor. It contains information about the status of the device at this point.

This information includes which channels have reached a terminal count and which channels have pending DMA

requests. Bits 0-3 are set every time a TC is reached by that channel or an external EOP is applied. These bits are cleared upon reset and on each status read. Bits 4-7 are set whenever their corresponding channel is requesting service.

Temporary Register - The temporary register is used to hold data during memory-to-memory transfers. Following the completion of a transfer, the last word moved can be read by the microprocessor in the program condition. The temporary register always contains the bit pattern on the data bus.

last byte transferred in the previous memory-to-memory operation, unless cleared by a reset.

Software Commands - These are two additional special software commands which can be executed in the program condition. They do not depend on any specific The two software commands are as follows:

Master Clear: This software instruction has the same effect as the hardware reset. The command status, request and temporary registers are cleared and the mask register is set. The MA28137 will enter the idle cycle.

Clear mask: This command clears the mask bits of all four channels, enabling them to accept DMA requests.

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Register	Operation	Signals				
		RD/W	A12	A13	A14	A15
Command	Write	0	1	0	0	0
Mode	Write	0	1	0	1	1
Request	Write	0	1	0	0	1
Mask	Set/reset	0	1	0	1	0
Mask	Write	0	1	1	1	1
Temporary	Read	1	1	1	0	1
Status	Read	1	1	0	0	0
MMU stat.	Write	0	1	1	0	0

Signals					Operation
A12	A13	A14	A15	RD/W	
1	0	0	0	1	Read status register
1	0	0	0	0	Write command register
1	0	0	1	1	Illegal
1	0	0	1	0	Write request register
1	0	1	0	1	Ilegal
1	0	1	0	0	Write single mask register bit
1	0	1	1	1	Illegal
1	0	1	1	0	Write mode register
1	1	0	0	1	Ilegal
1	1	0	0	0	Write MMU status
1	1	0	1	1	Read temporary register
1	1	0	1	0	Master clear
1	1	1	0	1	Ilegal
1	1	1	0	0	Clear mask register
1	1	1	1	1	Ilegal
1	1	1	1	0	Write all mask register bits

PROGRAMMING

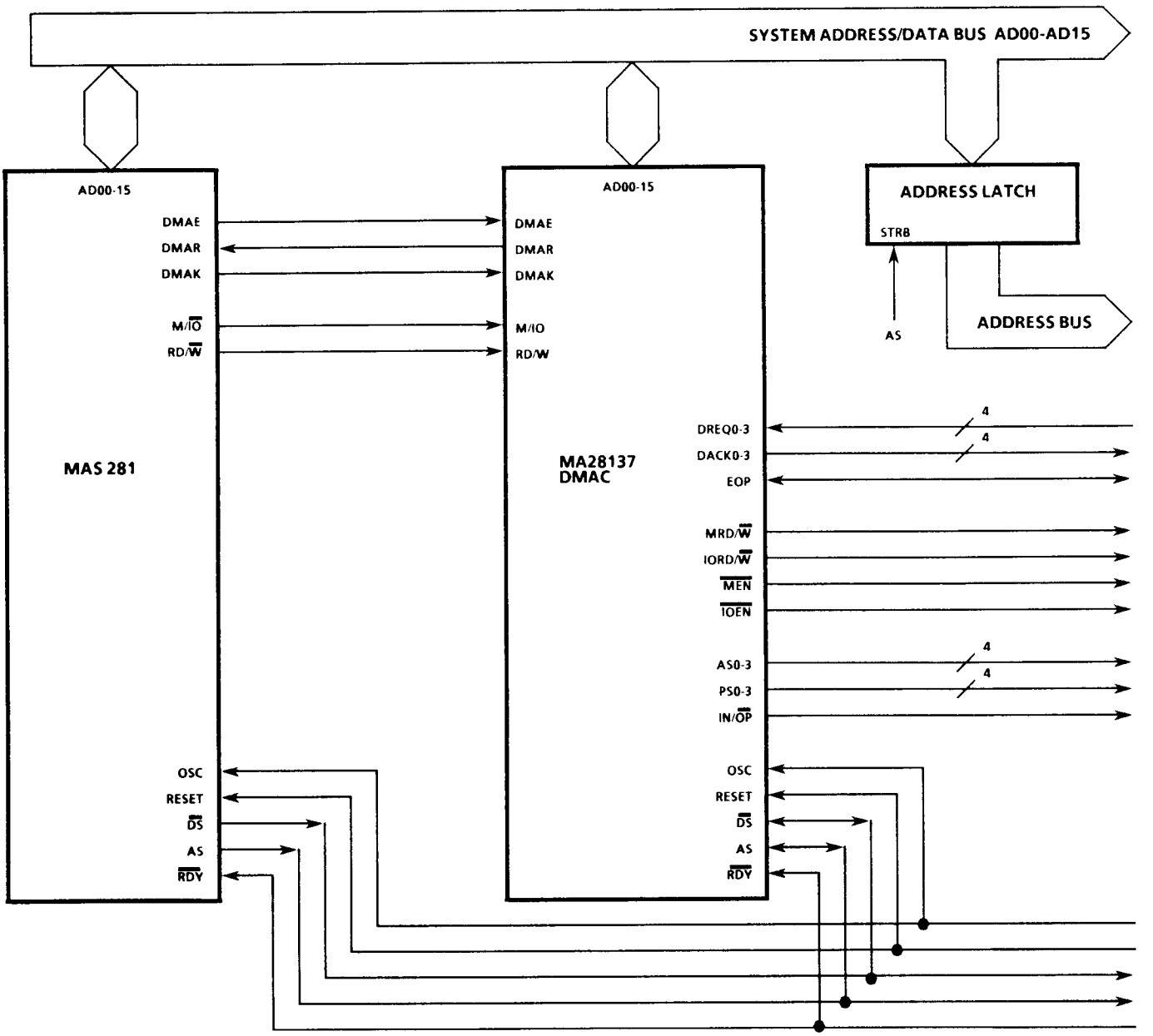
The MA28137 will accept programming from the host processor any time that DMAK is inactive; this is true even if DMAR is active. The responsibility of the host is to assure that programming and DMAK are mutually exclusive. Note that a problem can occur if a DMA request occurs on an unmasked channel while the MA28137 is being programmed. For instance, the CPU may be starting to reprogam the two byte address register of channel 1 when channel 1 receives a DMA request. If the MA28137 is enabled (bit 2 in the command register is 0) and channel 1 is unmasked, a DMA service will occur after only one byte of the address register has been reprogrammed. This can be avoided by disabling the controller (setting bit 2 in the command register) or masking the channel before programming any other registers. Once this is complete, the controller can be enabled/un-masked.

After power-up it is suggested that all internal locations especially the mode registers, be loaded with some valid value. This should be done even if some channels are unused.

Radiation hard Programmable DMA Controller

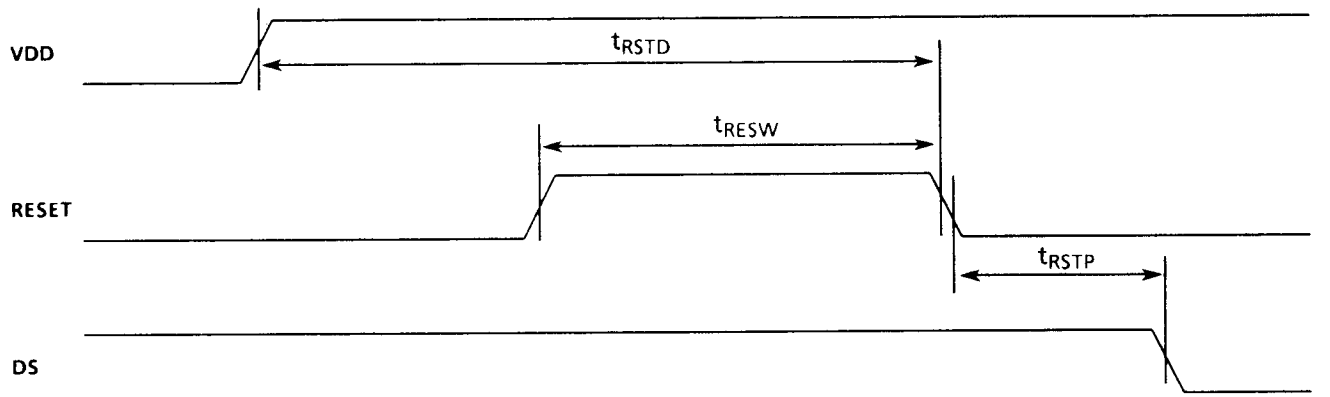
APPLICATIONS INFORMATION

The diagram below shows a suitable method for configuring a DMA system with the MA28137 controller and an MAS281 microprocessor system. The multimode DMA controller issues a DMAR to the processor whenever there is at least one valid DMA request from a peripheral device. When the processor replies with a DMAK signal, the MA28137 takes control of the address bus, the data bus and the control bus.

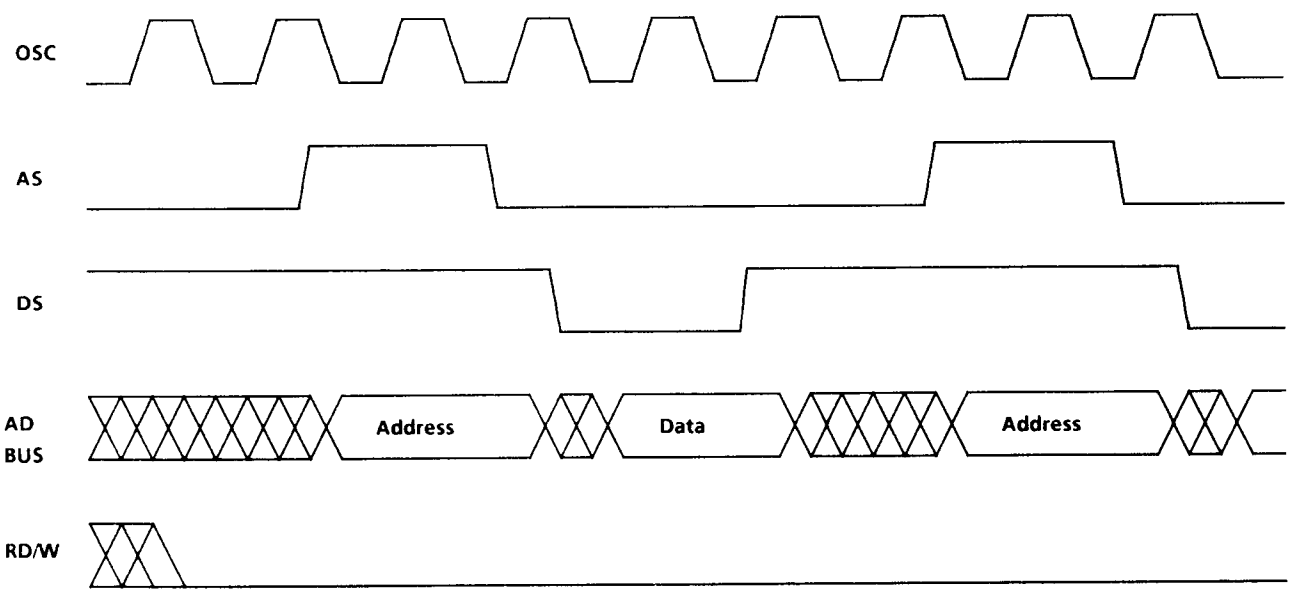


MA28137 System interfacing

TIMING DIAGRAMS

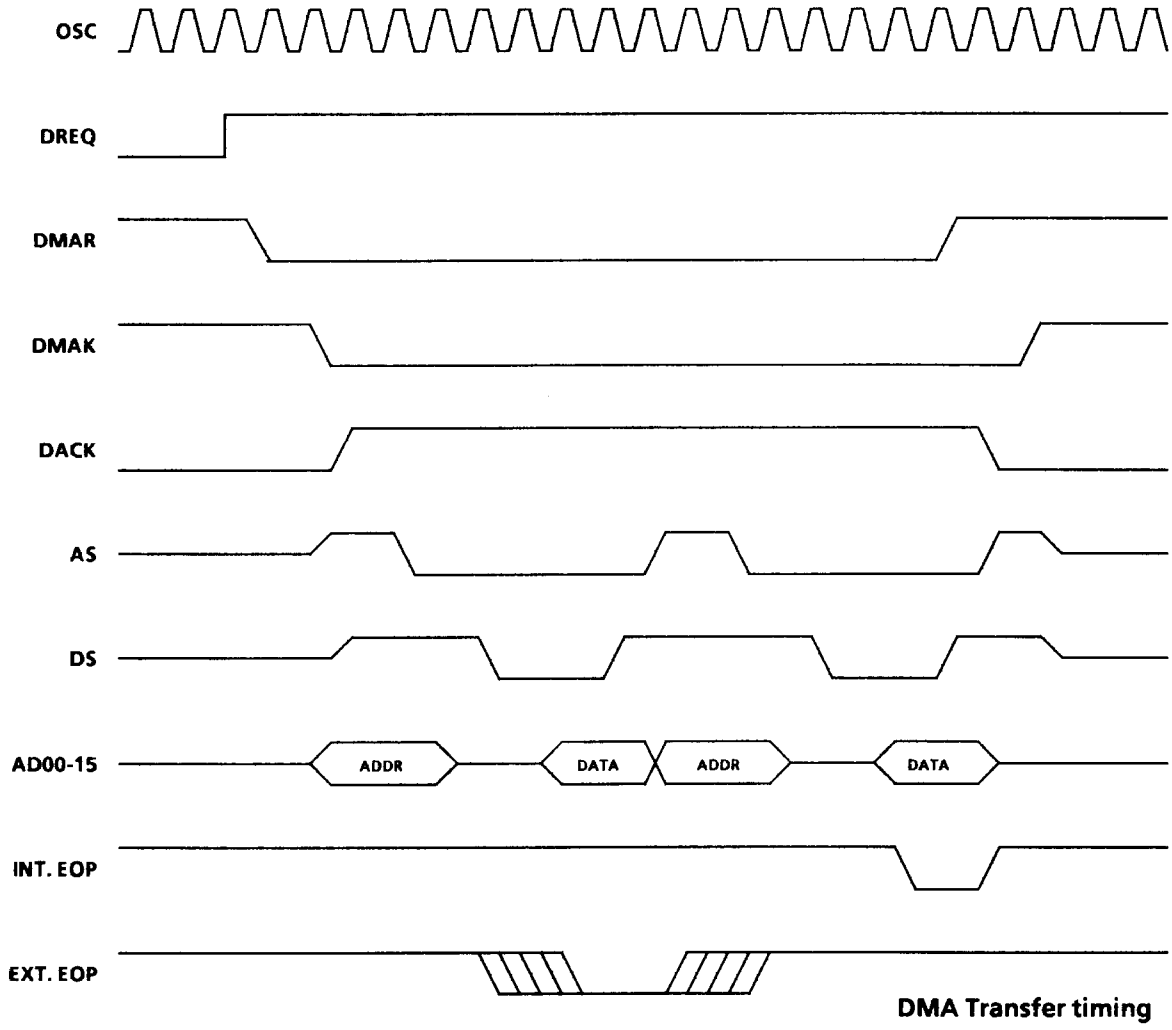


Reset Timing

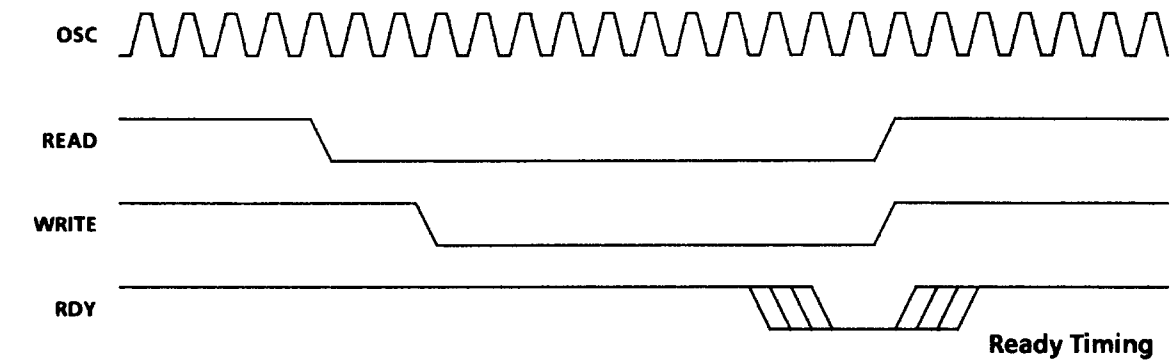


Slave mode write

TIMING DIAGRAMS (continued)



DMA Transfer timing



Ready Timing

ABSOLUTE MAXIMUM RATINGS

PARAMETER	MIN	MAX	UNITS
SUPPLY VOLTAGE	-0.5	10	V
INPUT VOLTAGE	-0.3	V_{DD} + 0.3	V
CURRENT THROUGH ANY PIN	-20	20	mA
OPERATING TEMP.	-55	125	°C
STORAGE TEMP.	-65	150	°C

Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions, or at any other condition above those indicated in the operations section of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING DC ELECTRICAL CHARACTERISTICS

V_{DD} = 5V ± 10%. Over full operating temperature range.

SYMBOL	PARAMETER	TOTAL DOSE RADIATION NOT EXCEEDING $3x10^5$ RAD (Si)			TOTAL DOSE ≤ 1 MRAD (Si)		UNITS	CONDITION
		MIN	TYP	MAX	MIN	MAX		
V_{DD}	SUPPLY VOLTAGE	4.5	5.0	5.5	4.5	5.5	V	
V_{IH1}	Input High Voltage	2.0			2.0		V	
V_{IL1}	Input Low Voltage			0.8		0.3	V	
V_{OH1}	Output High Voltage	2.4			2.4		V	I_{OH} = -0.8mA
V_{OL1}	Output low Voltage			0.4		0.4	V	I_{OL} = 2.0mA
I_{ILI}	Input Leakage Current			10		10	uA	$V_{IN} = V_{SS}$ or V_{DD}
I_{LO}	Output Leakage Current			20		20	uA	$V_{OUT} = V_{SS}$ or V_{DD}
I_{DD}	Power Supply Current		0.1	1.0		4.0	mA	Static

Radiation Hard Programmable DMA Controller

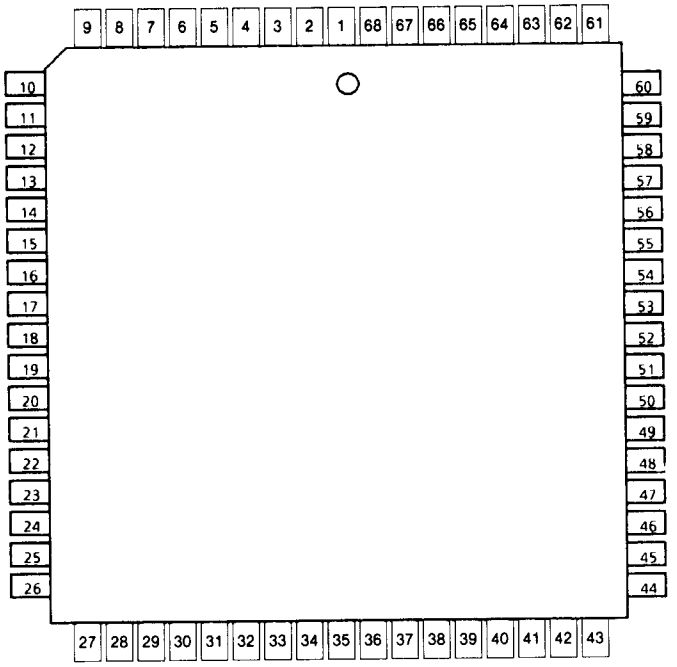
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNITS	CONDITIONS
t_{RSTD}	VDD applied to RESET falling	V_{DD}	RESET			ns	
t_{RESW}	RESET pulse width	RESET	RESET			ns	
t_{RSTP}	RESET to first Program	RESET	CS			ns	
t_{CW}	Chip select to end of write	CS	DS			ns	
t_{ASU}	Address setup to AS falling	A15-12	AS			ns	
t_{AH}	Address hold from AS falling	A15-12	AS			ns	
t_{DSUW}	Data setup to DS rising (processor writing)	AD15-00	DS			ns	
t_{DHW}	Data hold from DS falling (processor writing)	AD15-00	DS			ns	
t_{DSUR}	Data setup to DS rising (processor reading)	AD15-00	DS			ns	
t_{DSUR}	Data hold from DS falling (processor reading)	AD15-00	DS			ns	
t_{DSL}	Write pulse width	DS	DS			ns	
t_{DOZ}	DS rising to data output high impedance	DS	AD15-00			ns	

Radiation Hard Programmable DMA Controller

PIN ASSIGNMENTS

68 Lead Ceramic Flatpack

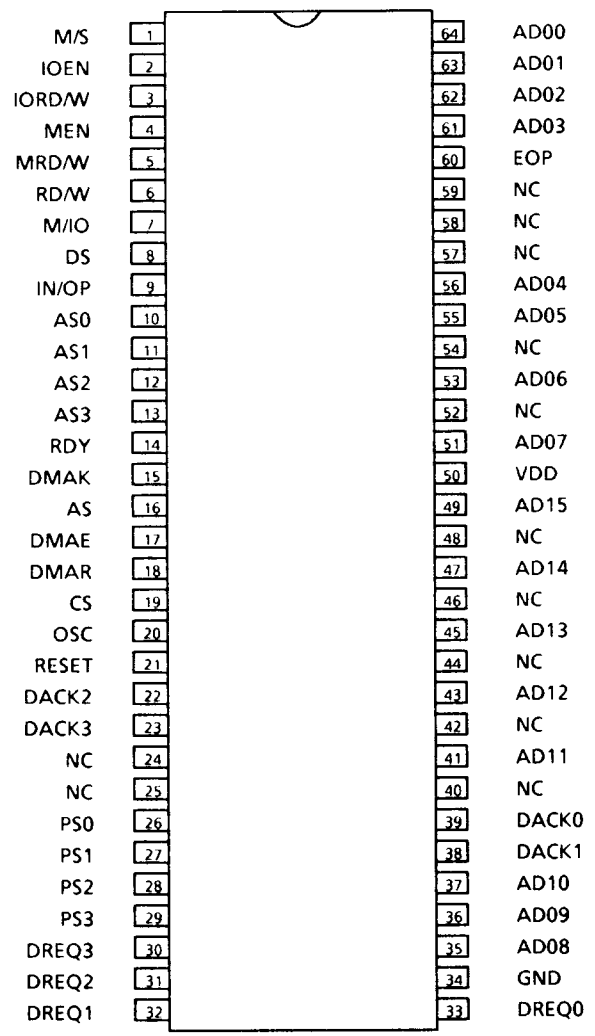


1	M/S	18	DMAR	35	GND	52	AD15
2	IOEN	19	CS	36	AD08	53	VCC
3	IORD/W	20	OSC	37	AD09	54	AD07
4	MEN	21	RESET	38	AD10	55	NC
5	MRD/W	22	DACK2	39	DACK1	56	AD06
6	RD/W	23	DACK3	40	DACK0	57	NC
7	M/IO	24	NC	41	NC	58	AD05
8	DS	25	NC	42	NC	59	AD04
9	IN/OP	26	NC	43	NC	60	NC
10	AS0	27	PS0	44	AD11	61	NC
11	AS1	28	PS1	45	NC	62	NC
12	AS2	29	PS2	46	AD12	63	NC
13	AS3	30	PS3	47	NC	64	EOP
14	RDY	31	DREQ3	48	AD13	65	AD03
15	DMAK	32	DREQ2	49	NC	66	AD02
16	AS	33	DREQ1	50	AD14	67	AD01
17	DMAE	34	DREQ0	51	NC	68	AD00

Radiation Hard Programmable DMA Controller

PIN ASSIGNMENTS (continued)

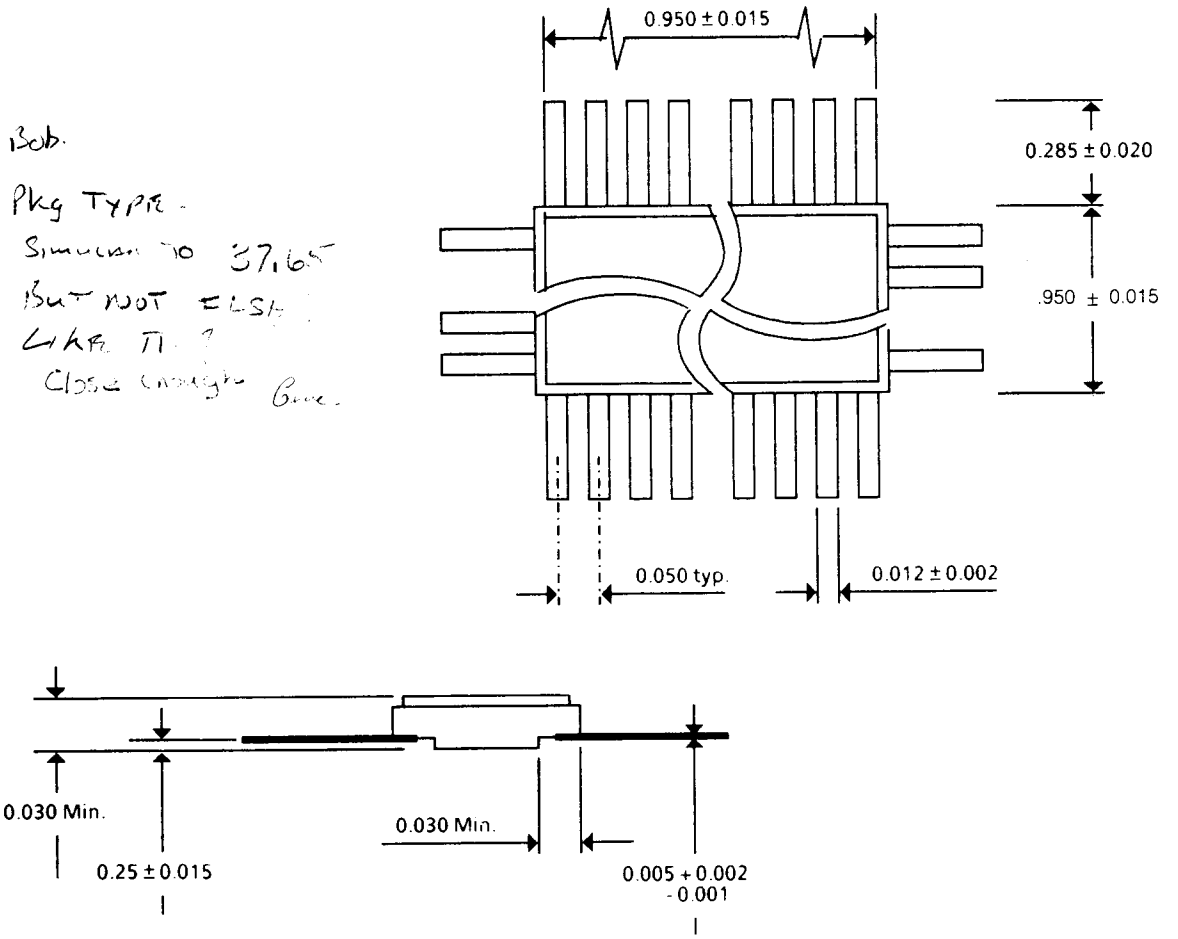
64 Lead DIL



Radiation Hard Programmable DMA Controller

PACKAGE OUTLINES

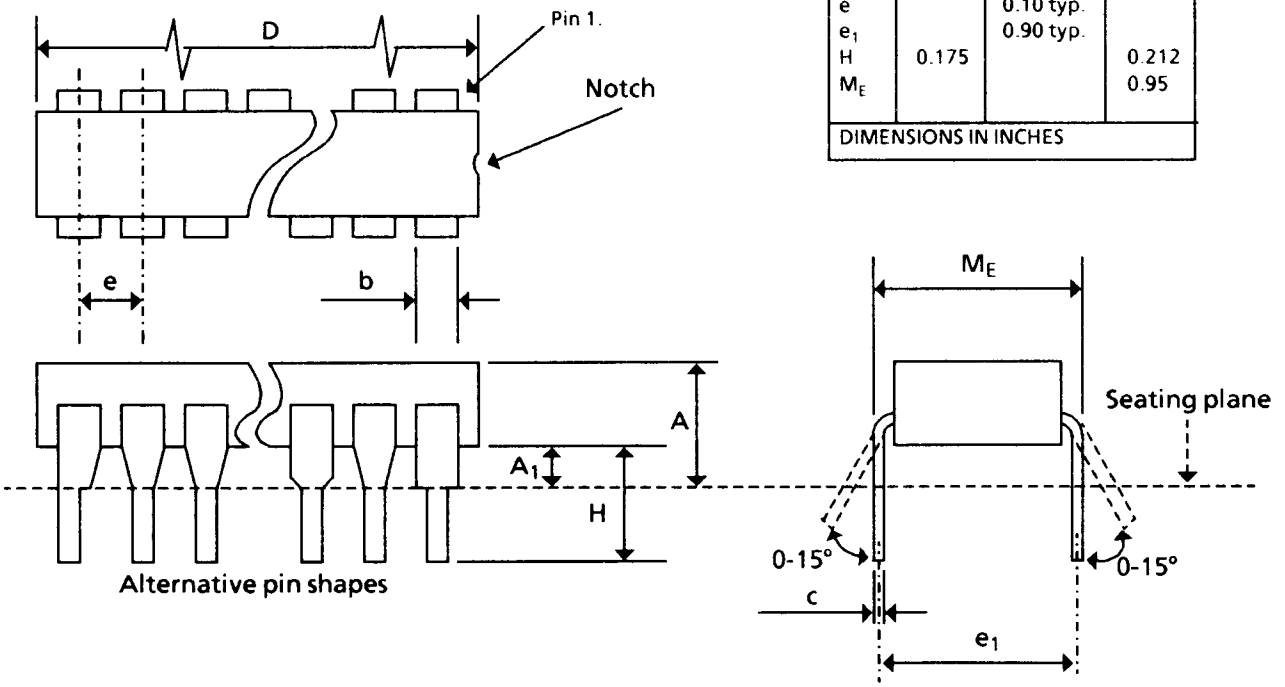
68 Lead Ceramic Flatpack



Radiation Hard Programmable DMA Controller

PACKAGE OUTLINES (cont.)

64 Lead Ceramic DIL



Ref.	Min.	Nom.	Max.
A	0.105		0.145
A_1	0.025		0.045
b	0.047		0.053
c		0.01	
D	3.189		1.111
e		0.10 typ.	
e_1		0.90 typ.	
H	0.175		0.212
M_E			0.95
DIMENSIONS IN INCHES			

Radiation Hard Programmable DMA Controller

TOTAL DOSE RADIATION TESTING

For product procured to guaranteed total dose radiation levels, each wafer lot will be approved when all sample devices from each lot pass the total dose radiation test.

The sample devices will be subjected to the total dose radiation level (Cobalt-60 Source), defined by the ordering code, and must continue to meet the electrical parameters specified in the data sheet. Electrical tests, pre and post irradiation, will be read and recorded.

Marconi Electronic Devices can provide radiation testing compliant with MIL STD 883C remote sensing method 1019 notice 5.

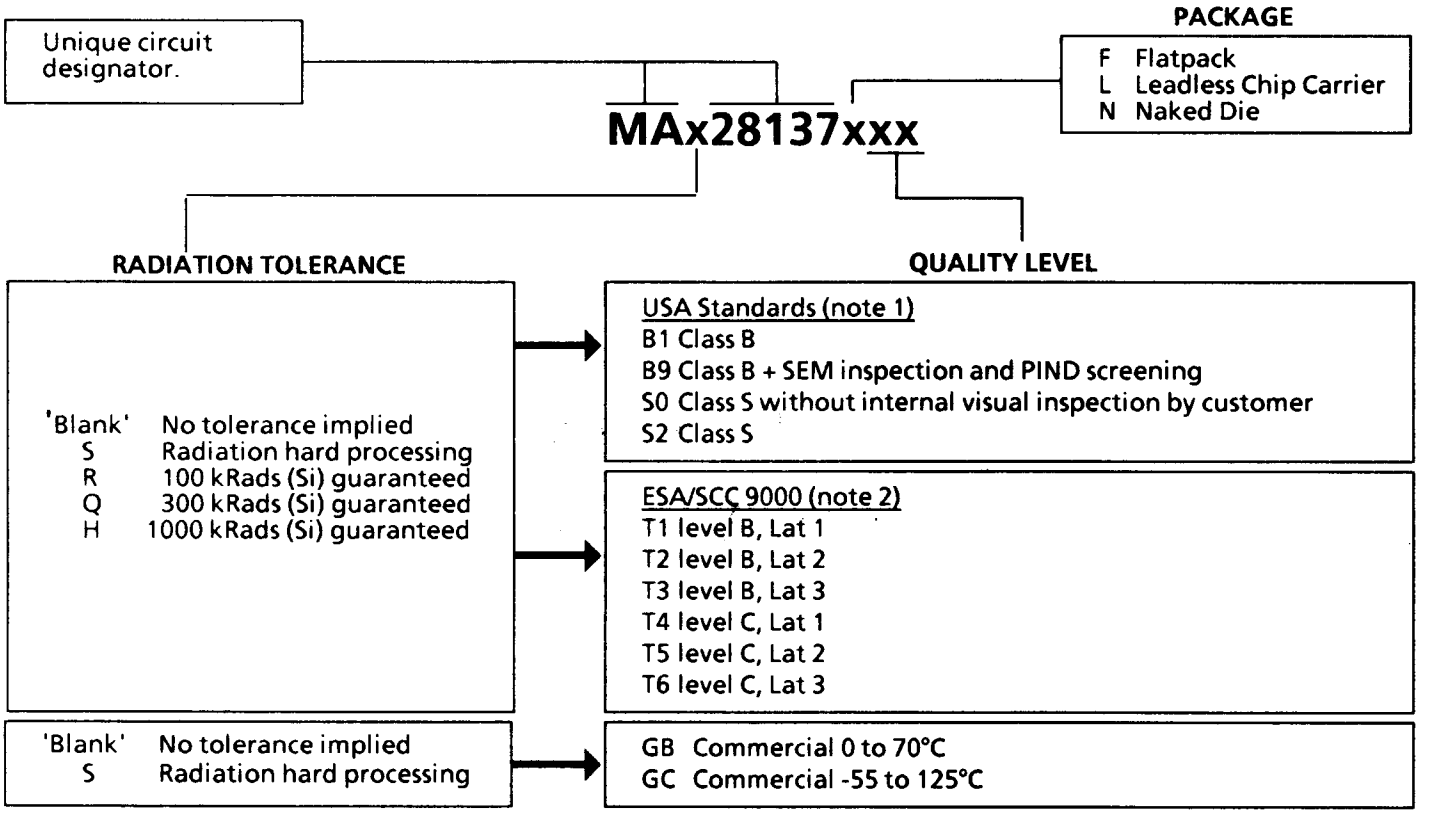
RADIATION PERFORMANCE

Total dose (Function to 300 KRad specification)	$3x10^5$ Rad (Si)
Total dose (Function to 1 MRad specification)	$1x10^6$ Rad (Si)
Transient upset (Stored data loss)	$1x10^{11}$ Rad (Si)/sec
Transient Upset (Survivability)	$>1x10^{12}$ Rad (Si)/sec
Neutron Hardness (Function to specification)	$1x10^{15}$ neutrons/cm^2
Latch-Up	Not Possible

Bob. TOTAL DOSE
3×10^5 - 3 MIL
ISN'T 0.1
2.5 - IS IT?
1×10^6 RADS

Radiation Hard Programmable DMA Controller

ORDERING INFORMATION



1 Marconi Electronic Devices quality levels conform to MIL STD 883C class B/S, screening method 5004 and Quality Conformance Inspection method 5005 . This does not imply DESC certification, however MIL-M-38510 qualified product listing is being sought.

2 Marconi's specifications for European Space manufacturing flows, including their associated screening procedures, conform to ESA/SCC Generic Specification No.9000. A Process Identification Document, describing the manufacture of these devices, has been approved by the European Space Agency.

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