

BLP15H9S100G

Power LDMOS transistor

Rev. 3 — 8 July 2021

AMPLEON

Product data sheet

1. Product profile

1.1 General description

A 100 W LDMOS driver transistor for broadcast and industrial applications. The excellent ruggedness of this device makes it ideal for digital and analog transmitter applications in the frequency range from HF to 2 GHz.

Table 1. Typical performance

Test signal	f (MHz)	V _{DS} (V)	P _L (W)	G _p (dB)	η _D (%)
pulsed RF	1400	50	100	20	62
	1700 to 1850	50	100	16	50
CW	325 to 352	50	90	25	61
	360 to 450	50	100	16	53
DVB-T	169 to 223	50	20	23	30
	470 to 700	50	20	20	30

1.2 Features and benefits

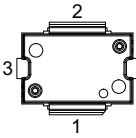
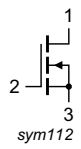
- Designed for broadband operation
- High efficiency
- Integrated dual sided ESD protection
- Excellent ruggedness
- High power gain
- Excellent reliability
- Easy power control
- Excellent stability
- For RoHS compliance see the product details on the Ampleon website

1.3 Applications

- Broadcast transmitter applications
- Industrial, scientific and medical applications
- Applicable at frequencies from HF to 2 GHz

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	drain		
2	gate		
3	source ^[1]		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Package name	Orderable part number	12NC	Packing description	Min. orderable quantity (pieces)
SOT1483-1	BLP15H9S100GZ	9349 603 12515	TR13; 500-fold; 24 mm; dry pack	500
SOT1483-1	BLP15H9S100GXY	9349 603 12538	TR7; 100-fold; 24 mm; dry pack	100

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	106	V
V_{GS}	gate-source voltage		-6	+11	V
T_{stg}	storage temperature		-65	+150	°C
T_j	junction temperature ^[1]		-	225	°C

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the online MTF calculator.

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	$T_{case} = 70\text{ °C}; V_{DS} = 50\text{ V}; P_L = 100\text{ W}$	0.67	K/W

6. Characteristics

Table 6. DC characteristics

$T_j = 25\text{ }^\circ\text{C}$; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0\text{ V}$; $I_D = 0.67\text{ mA}$	106	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$V_{DS} = 10\text{ V}$; $I_D = 67\text{ mA}$	1.5	2.0	2.5	V
V_{GSq}	gate-source quiescent voltage	$V_{DS} = 50\text{ V}$; $I_D = 30\text{ mA}$	1.5	2.0	2.5	V
I_{DSS}	drain leakage current	$V_{GS} = 0\text{ V}$; $V_{DS} = 50\text{ V}$	-	-	1.4	μA
I_{DSX}	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75\text{ V}$; $V_{DS} = 10\text{ V}$	-	11.3	-	A
I_{GSS}	gate leakage current	$V_{GS} = 11\text{ V}$; $V_{DS} = 0\text{ V}$	-	-	140	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75\text{ V}$; $I_D = 2.35\text{ A}$	-	0.30	-	Ω

Table 7. RF characteristics

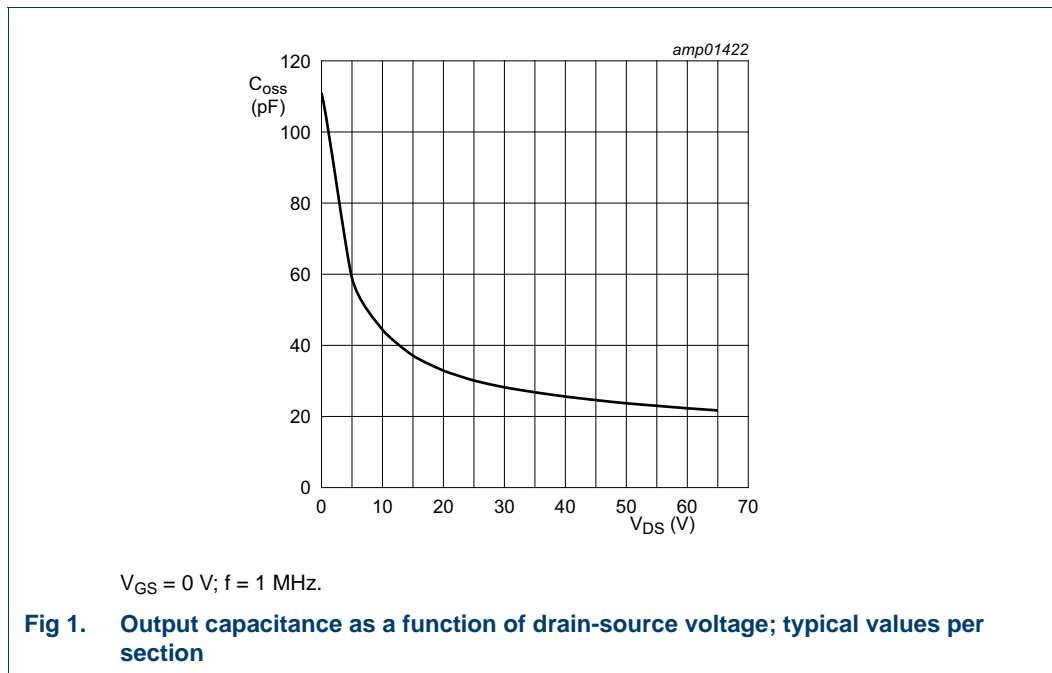
Test signal: pulsed RF; $t_p = 100\text{ }\mu\text{s}$; $\delta = 20\%$; $f = 1400\text{ MHz}$; RF performance at $V_{DS} = 50\text{ V}$; $I_{Dq} = 30\text{ mA}$; $T_{case} = 25\text{ }^\circ\text{C}$; unless otherwise specified; in a class-AB production test circuit with Johnstech socket.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	$P_L = 100\text{ W}$	18	19	-	dB
RL_{in}	input return loss	$P_L = 100\text{ W}$	-	-14	-9	dB
η_D	drain efficiency	$P_L = 100\text{ W}$	53	56	-	%

Table 8. AC characteristics

$T_j = 25\text{ }^\circ\text{C}$; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{iss}	input capacitance	$V_{GS} = 0\text{ V}$; $V_{DS} = 50\text{ V}$; $f = 1\text{ MHz}$	-	75	-	pF
C_{oss}	output capacitance	$V_{GS} = 0\text{ V}$; $V_{DS} = 50\text{ V}$; $f = 1\text{ MHz}$	-	23.4	-	pF
C_{rss}	reverse transfer capacitance	$V_{GS} = 0\text{ V}$; $V_{DS} = 50\text{ V}$; $f = 1\text{ MHz}$	-	0.53	-	pF



7. Test information

7.1 Ruggedness in class-AB operation

The BLP15H9S100G is capable of withstanding a load mismatch corresponding to VSWR = 30 : 1 through all phases under the following conditions: V_{DS} = 55 V; I_{Dq} = 30 mA; P_L = 120 W; f = 1400 MHz; pulsed CW (t_p = 100 μs; δ = 20 %).

7.2 Test circuit

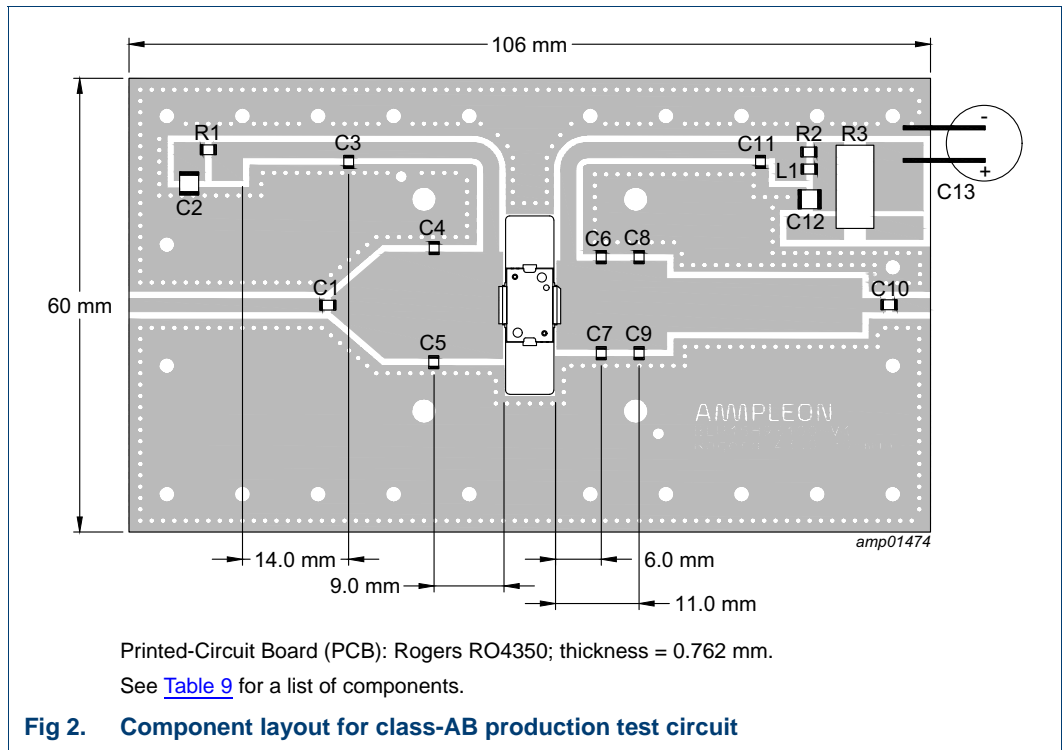


Table 9. List of components

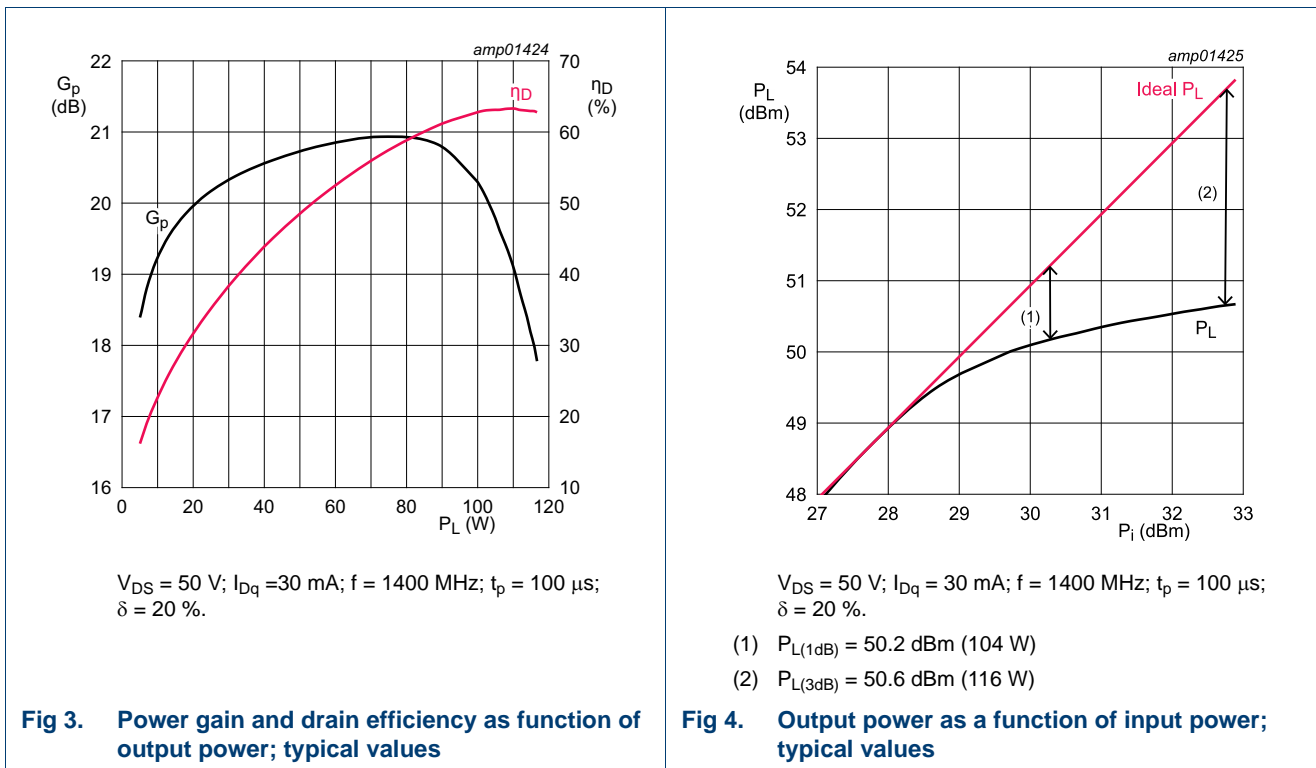
For test circuit see [Figure 2](#).

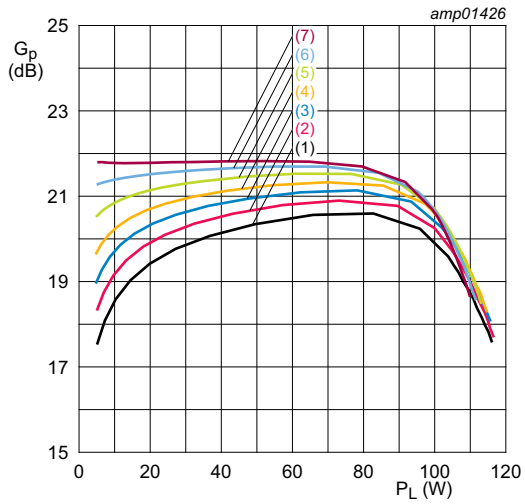
Component	Description	Value	Remarks
C1	multilayer ceramic chip capacitor	2.2 pF	[1]
C2, C12	multilayer ceramic chip capacitor	4.7 μF, 100 V	
C3, C11	multilayer ceramic chip capacitor	30 pF	[1]
C4, C5	multilayer ceramic chip capacitor	2.7 pF	[1]
C6, C7	multilayer ceramic chip capacitor	6.8 pF	[1]
C8, C9	multilayer ceramic chip capacitor	3.3 pF	[1]
C10	multilayer ceramic chip capacitor	20 pF	[1]
C13	electrolytic capacitor	470 μF, 64 V	
R1	chip resistor	4.7 Ω	SMD 1206
R2	chip resistor	10 Ω	SMD 1206
R3	shunt resistor	0.01 Ω	
L1	inductor	9 nH	Coilcraft: 1508-9N0GLB

[1] American Technical Ceramics type 800A or capacitor of same quality.

7.3 Graphical data

7.3.1 Pulsed CW performance measured in production RF test circuit

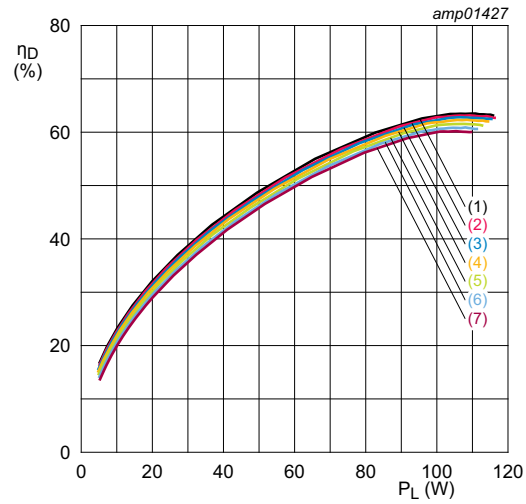




$V_{DS} = 50 \text{ V}$; $f = 1400 \text{ MHz}$; $t_p = 100 \text{ } \mu\text{s}$; $\delta = 20 \text{ \%}$.

- (1) $I_{Dq} = 10 \text{ mA}$
- (2) $I_{Dq} = 30 \text{ mA}$
- (3) $I_{Dq} = 60 \text{ mA}$
- (4) $I_{Dq} = 100 \text{ mA}$
- (5) $I_{Dq} = 200 \text{ mA}$
- (6) $I_{Dq} = 300 \text{ mA}$
- (7) $I_{Dq} = 400 \text{ mA}$

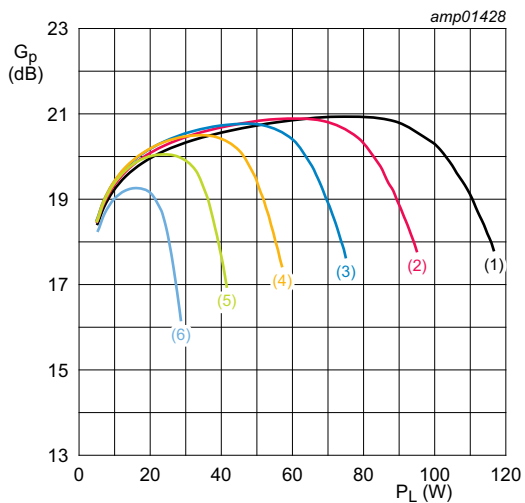
Fig 5. Power gain as a function of output power; typical values



$V_{DS} = 50 \text{ V}$; $f = 1400 \text{ MHz}$; $t_p = 100 \text{ } \mu\text{s}$; $\delta = 20 \text{ \%}$.

- (1) $I_{Dq} = 10 \text{ mA}$
- (2) $I_{Dq} = 30 \text{ mA}$
- (3) $I_{Dq} = 60 \text{ mA}$
- (4) $I_{Dq} = 100 \text{ mA}$
- (5) $I_{Dq} = 200 \text{ mA}$
- (6) $I_{Dq} = 300 \text{ mA}$
- (7) $I_{Dq} = 400 \text{ mA}$

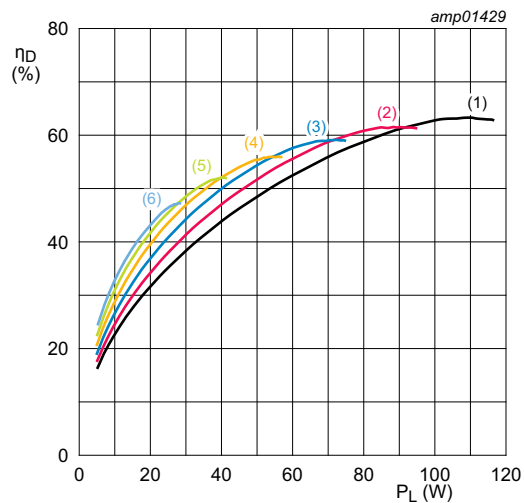
Fig 6. Drain efficiency as a function of output power; typical values



$I_{Dq} = 30 \text{ mA}; f = 1400 \text{ MHz}; t_p = 100 \text{ }\mu\text{s}; \delta = 20 \text{ \%}.$

- (1) $V_{DS} = 50 \text{ V}$
- (2) $V_{DS} = 45 \text{ V}$
- (3) $V_{DS} = 40 \text{ V}$
- (4) $V_{DS} = 35 \text{ V}$
- (5) $V_{DS} = 30 \text{ V}$
- (6) $V_{DS} = 25 \text{ V}$

Fig 7. Power gain as a function of output power; typical values



$I_{Dq} = 30 \text{ mA}; f = 1400 \text{ MHz}; t_p = 100 \text{ }\mu\text{s}; \delta = 20 \text{ \%}.$

- (1) $V_{DS} = 50 \text{ V}$
- (2) $V_{DS} = 45 \text{ V}$
- (3) $V_{DS} = 40 \text{ V}$
- (4) $V_{DS} = 35 \text{ V}$
- (5) $V_{DS} = 30 \text{ V}$
- (6) $V_{DS} = 25 \text{ V}$

Fig 8. Drain efficiency as a function of output power; typical values

8. Package outline

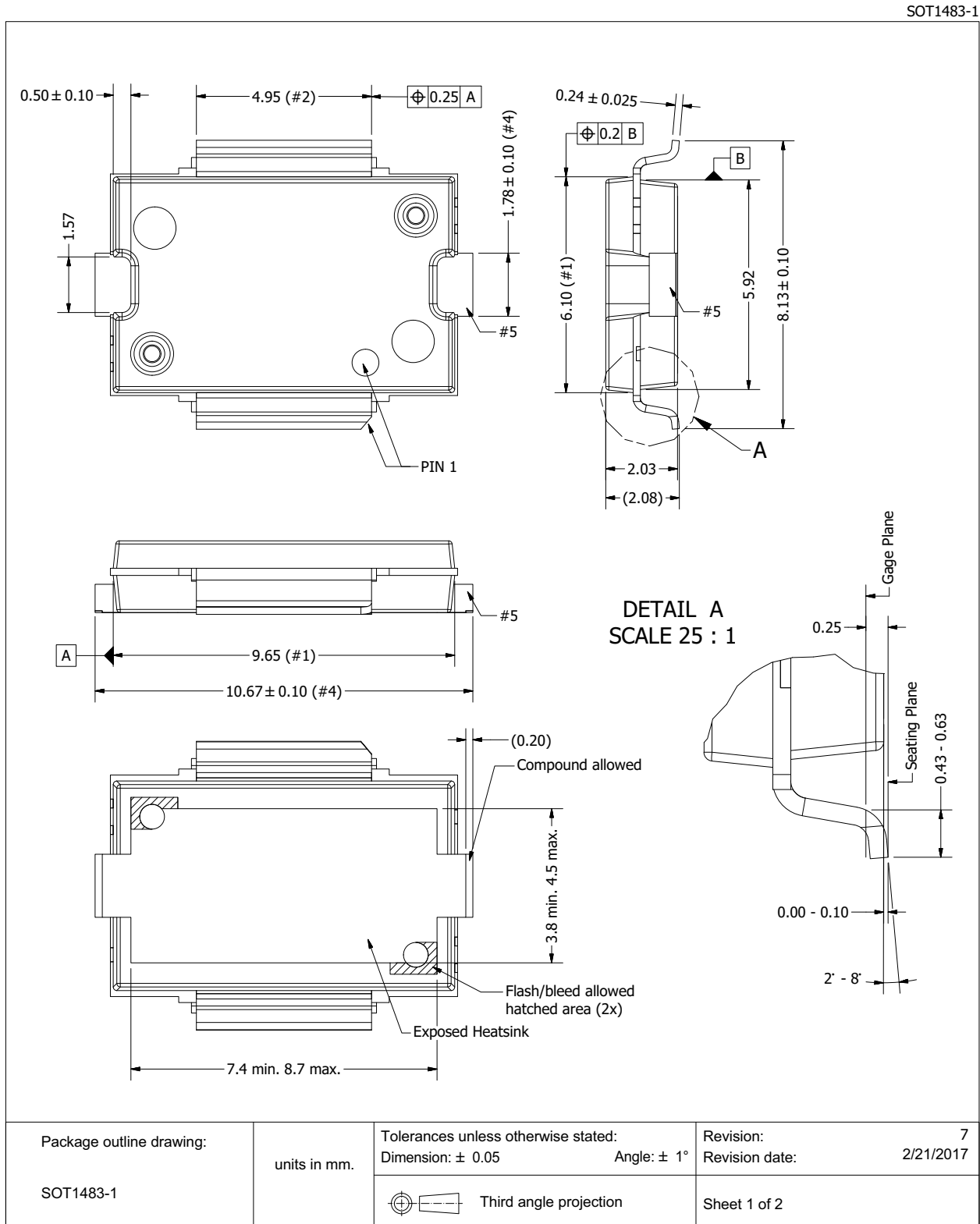
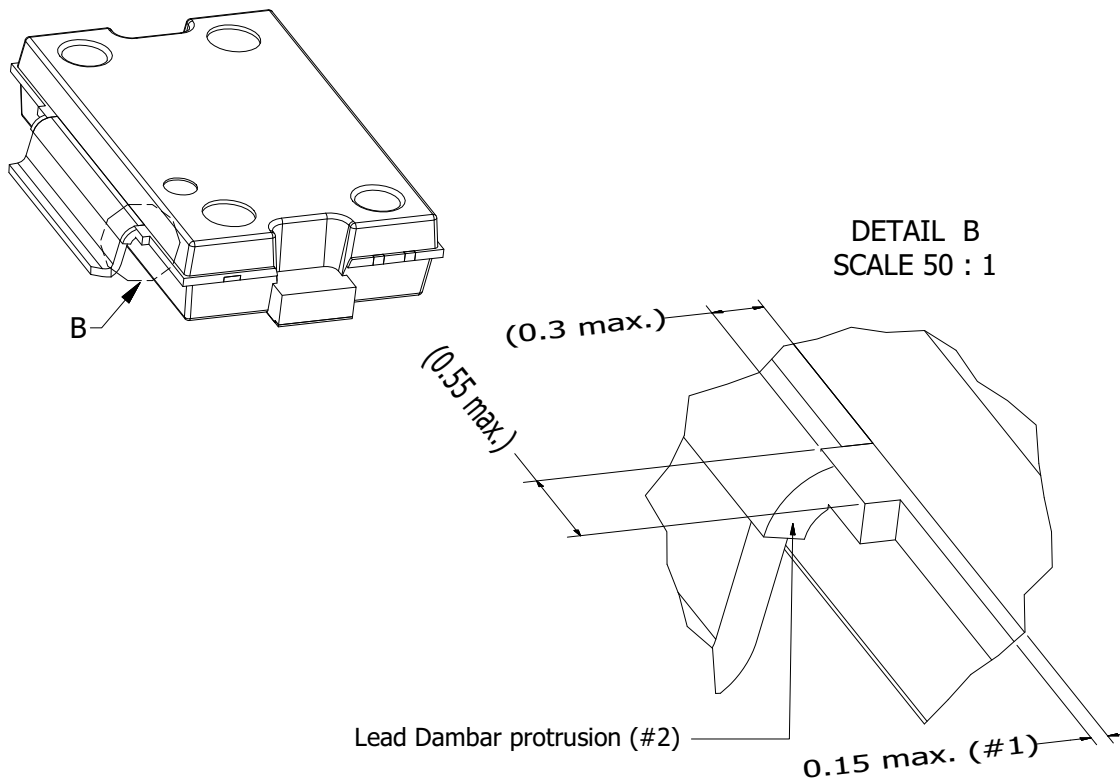


Fig 9. Package outline SOT1483-1 (sheet 1 of 2)

SOT1483-1

Drawing Notes	
Items	Description
(1)	Dimensions are excluding mold protrusion. The mold protrusion is maximum 0.15 mm per side. See also detail B. In the dambar area max. protrusion is 0.55mm max. in length and 0.3 mm max. in width (4x) See also detail B.
(2)	The lead dambar (metal) protrusions are not included. Add 0.14 mm max to the total lead dimension at the dambar location.
(3)	The leads and exposed heatsink are plated with matte Tin (Sn).
(4)	Dimensions (Heatsink ears) 10,67 and 1,78 do not include mould protrusion. Overall Max. dimensions incl. mould protrusions is 10,92 mm. (max.) and 2,03 mm. (max.).
(5)	Surfaces may remain unplated (not solderable surfaces).




Package outline drawing:	units in mm.	Tolerances unless otherwise stated: Dimension: ± 0.05 Angle: $\pm 1^\circ$	Revision: 7 Revision date: 2/21/2017
SOT1483-1		 Third angle projection	Sheet 2 of 2

Fig 10. Package outline SOT1483-1 (sheet 2 of 2)

9. Handling information

CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

Table 10. ESD sensitivity

ESD model	Class
Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002	C2B [1]
Human Body Model (HBM); According to ANSI/ESDA/JEDEC standard JS-001	2 [2]

[1] CDM classification C2B is granted to any part that passes after exposure to an ESD pulse of 750 V.

[2] HBM classification 2 is granted to any part that passes after exposure to an ESD pulse of 2000 V.

10. Abbreviations

Table 11. Abbreviations

Acronym	Description
CW	Continuous Wave
DVB-T	Digital Video Broadcast - Terrestrial
ESD	ElectroStatic Discharge
HF	High Frequency
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
MTF	Median Time to Failure
RoHS	Restriction of Hazardous Substances
SMD	Surface Mounted Device
VSWR	Voltage Standing Wave Ratio

11. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLP15H9S100G v.3	20210708	Product data sheet	-	BLP15H9S100G v.2
Modifications:	<ul style="list-style-type: none"> Table 3 on page 2: added orderable part number BLP15H9S100GXY 			
BLP15H9S100G v.2	20201210	Product data sheet	-	BLP15H9S100G v.1
BLP15H9S100G v.1	20200707	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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13. Contact information

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