DN74LS190 N74LS190

Synchronous BCD Up / Down Counters (with Up / Down Mode Control)

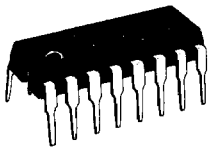
■ Description

DN74LS190 is a synchronous decade up/down counter with up/down control inputs and set inputs.

■ Features

- Up/down switching according to up/down control input
- Asynchronous set input
- Enable input
- Easy cascade connection
- High-speed counting (f_{max} = 25MHz typical)
- Wide operating temperature range (Ta = −20 to +75°C)

P-2

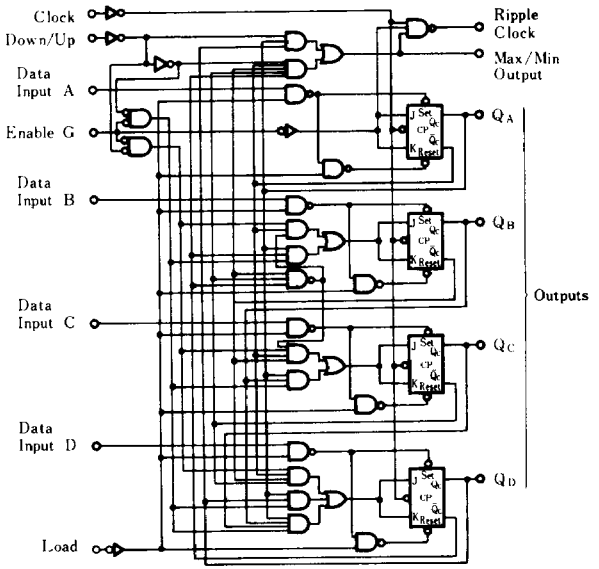


16-pin plastic DIL package

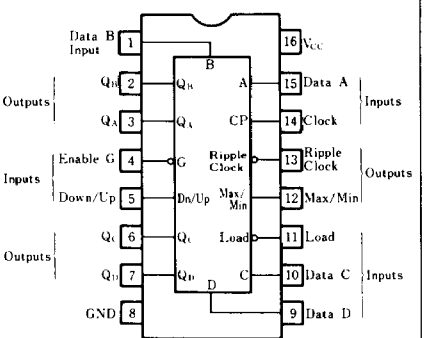
P-5

16-pin Panaflat package (SO-16D)

■ Logic diagram



Pin configuration (top view)



■ Recommended operating conditions

Parameter	Sym	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.00	5.25	V
Output current	I_{OH}			−400	μA
	I_{OL}			8	mA
Operating temperature range	Topr	−20	25	75	℃
Clock frequency	f_{clock}	0		20	MHz
Clock pulse width	$t_{W(CP)}$	30			ns
Load pulse width	$t_{W(Load)}$	35			ns
Set-up time	t_{su}	20			ns
Hold time	t_h	0			ns
Enable time	t_{enable}	40			ns

■ DC characteristics ($Ta = -20 \sim +75℃$)

Parameter		Sym	Test conditions		Min	Typ*	Max	Unit
Input voltage		V_{IH}			2.0			V
		V_{IL}					0.8	V
Output voltage		V_{OH}	$V_{CC}=4.75V$, $I_{OH}=-400\mu A$ $V_{IH}=2V$, $V_{IL}=0.8V$		2.7	3.4		V
		V_{OL}	$V_{CC}=4.75V$ $V_{IH}=2V$ $V_{IL}=0.8V$	$I_{OL}=4mA$		0.25	0.4	V
				$I_{OL}=8mA$		0.35	0.5	V
Input current	Enable	I_{IH}	$V_{CC}=5.25V$ $V_I=2.7V$				60	μA
	Others						20	μA
	Enable	I_{IL}	$V_{CC}=5.25V$ $V_I=0.4V$				−1.2	mA
	Others						−0.4	mA
	Enable	I_I	$V_{CC}=5.25V$ $V_I=7V$				0.3	mA
	Others						0.1	mA
Output short circuit current**		I_{OS}	$V_{CC}=5.25V$ $V_O=0V$		−15		−100	mA
Input clamp voltage		V_{IK}	$V_{CC}=4.75V$ $I_I=-18mA$				−1.5	V
Supply current***		I_{CC}	$V_{CC}=5.25V$			20	35	mA

* When constant at V_{CC} = 5V, Ta = 25°C.
** Only one output at a time short circuited to GND. Also, short circuit time to GND within 1 second.
*** Measured with all outputs open and all inputs grounded.

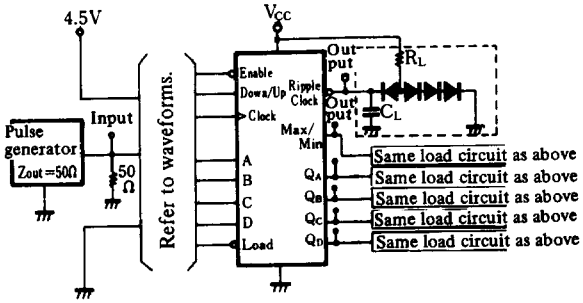
■ Switching characteristics ($V_{CC}=5V$, $Ta=25℃$)

Parameter	Sym	Inputs	Outputs	Test conditions	Min	Typ	Max	Unit
Maximum clock frequency	f_{max}	Clock	Q_A, Q_B Q_C, Q_D	$C_L=15pF$ $R_L=2k\Omega$	20	25		MHz
Propagation delay time	t_{PLH}	Load	Q_A, Q_B Q_C, Q_D			22	30	ns
	t_{PHL}					33	50	ns
	t_{PLH}	A, B C, D	Q_A, Q_B Q_C, Q_D			20	32	ns
	t_{PHL}					27	50	ns
	t_{PLH}	Clock	Ripple Clock			13	20	ns
	t_{PHL}					16	24	ns
	t_{PLH}	Clock	Q_A, Q_B Q_C, Q_D			16	24	ns
	t_{PHL}					24	42	ns
	t_{PLH}	Clock	Max/Min			28	42	ns
	t_{PHL}					37	52	ns
	t_{PLH}	Down/Up	Ripple Clock			30	45	ns
	t_{PHL}					30	45	ns
	t_{PLH}	Down/Up	Max/Min			21	33	ns
	t_{PHL}					22	33	ns
	t_{PLH}	Enable	Ripple Clock			21	33	ns
	t_{PHL}					22	33	ns

※ Switching parameter measurement information

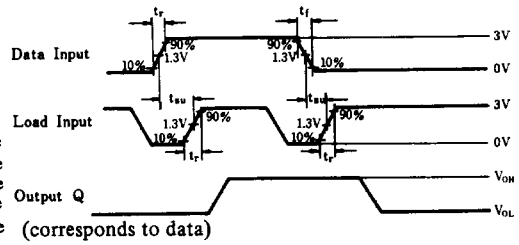
〔1〕 f_{max}, t_{PLH}, t_{PHL} (Clock → Q, $\overline{Q}$)

1. Measurement circuit



1. Number of pulse generators increased as needed.
2. C_L includes probe and tool floating capacitance.
3. Diodes are all MA161.

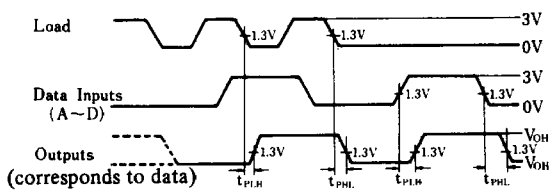
2. Waveforms



Notes

1. Input waveform: $t_r \leqq 15ns$, $t_f \leqq 6ns$, PRR = 1MHz, duty cycle = 50%.

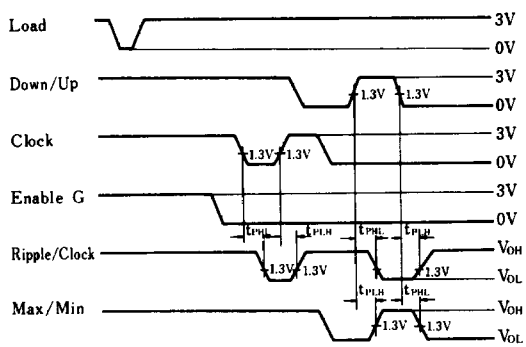
Waveforms 1 Load → Q, Date → Q



Notes

1. All other inputs are 4.5V.

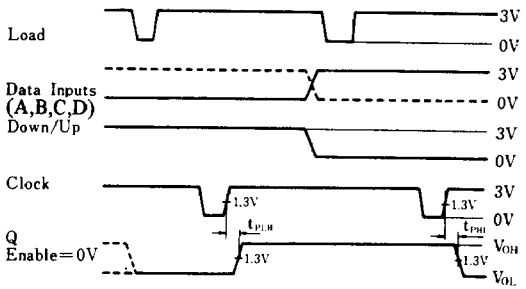
Waveforms-2 G → Ripple CP, CP → Ripple CP, Down/UP → Ripple CP, Down/ Up → Max/Min



Notes

1. All data inputs are 0V.

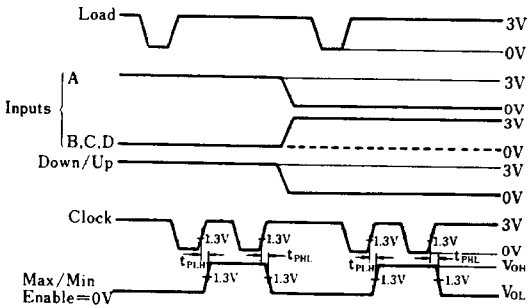
Waveforms-3 Clock → Q



Notes

1. When measuring Q_A, Q_B, and Q_C outputs, refer to the solid line for data inputs A, B, and C, and to the dashed line for input D.
2. When measuring Q_D output, refer to the solid line for data inputs A and D; B and C inputs are 0V.

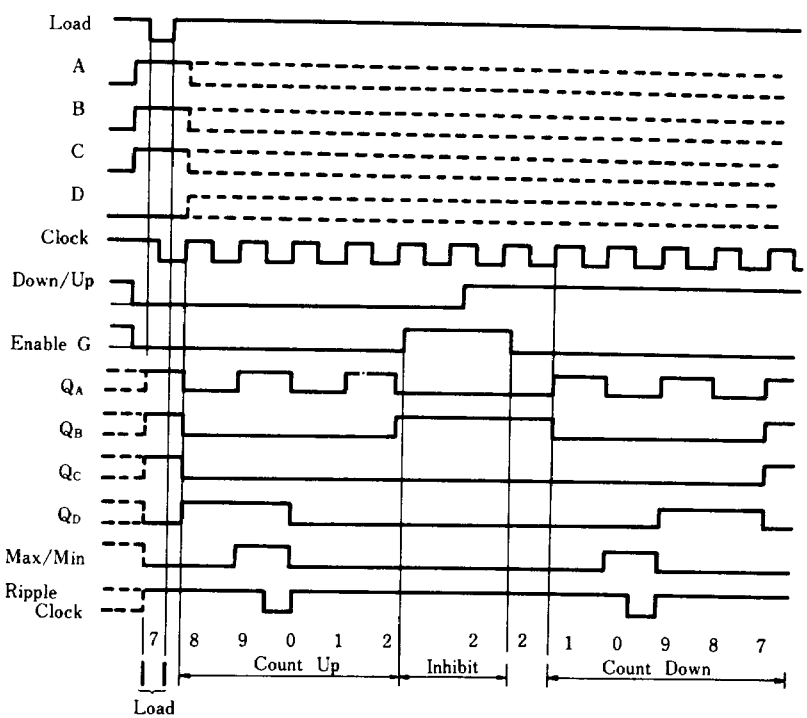
Waveforms-4 Clock → Max/Min



Notes

1. Refer to the dashed line for data inputs B and C, and to the solid line for data input D.

■ Timing chart



Count order

1. Load (set) at 7 (BCD).
2. Count up at 8, 9 (max), 0, 1, 2.
3. Inhibit.
4. Count down at 1, 0 (min), 9, 8, 7.