

GD54/74LS299

8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS

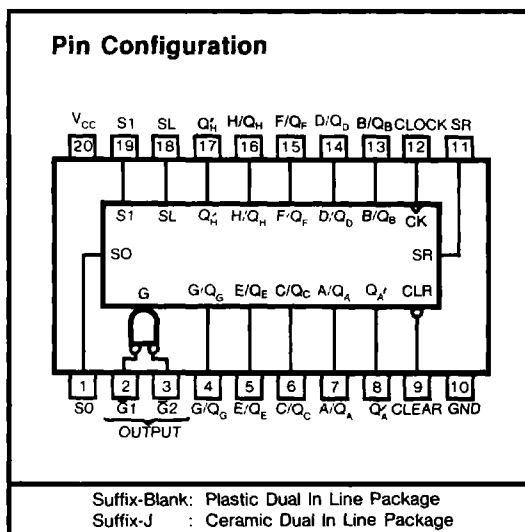
Features

- Multiplexed Inputs/Outputs Provide Improved Bit Density
- Four Modes of Operation:
 - Hold (Store) Shift Left
 - Shift Right Load Data
- Operates with Outputs Enabled or at High Z
- 3-State Outputs Drive Bus Lines Directly
- Can Be Cascaded for N-Bit Word Lengths
- Applications:
 - Stacked or Push-Down Registers.
 - Buffer Storage, and
 - Accumulator Registers

Description

These Schottky TTL eight-bit universal registers feature multiplexed inputs/outputs to achieve full eight bit data handling in a single 20-pin package. Two function-select inputs and two output-control inputs can be used to choose the modes of operation listed in the function table.

Synchronous parallel loading is accomplished by taking both function-select lines, S0 and S1, high. This places the three-state outputs in a high-impedance



state, which permits data that is applied on the input/output lines to be clocked into the register. Reading out of the register can be accomplished while the outputs are enabled in any mode. A direct overriding input is provided to clear the register whether the outputs are enabled or off.

Function Table

MODE	INPUTS					INPUTS/OUTPUTS								OUTPUT				
	CLEAR	FUNCTION SELECT		OUTPUT CONTROL		CLOCK	SERIAL		A/QA	B/QB	C/QC	D/QD	E/QE	F/QF	G/QG	H/QH	QA	QH
		S1	S0	$\overline{G1}^*$	$\overline{G2}^*$		SL	SR										
Clear	L	X	L	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
	L	L	X	X	L	L	X	X	L	L	L	L	L	L	L	L	L	L
Hold	H	L	L	L	L	X	X	X	QA _D	QB _D	QC _D	QD _D	QE _D	QF _D	QG _D	QH _D	QA _D	QH _D
	H	X	X	L	L	L	X	X	QA _O	QB _O	QC _O	QD _O	QE _O	QF _O	QG _O	QH _O	QA _O	QH _O
Shift Right	H	L	H	L	L	†	X	H	H	QA _n	QB _n	QC _n	QD _n	QE _n	QF _n	QG _n	H	QH _n
	H	L	H	L	L	†	X	L	L	QA _r	QB _r	QC _r	QD _r	QE _r	QF _r	QG _r	L	QH _r
Shift Left	H	H	L	L	L	†	H	X	QB _n	QC _n	QD _n	QE _n	QF _n	QG _n	QH _n	H	QA _n	H
	H	H	L	L	L	†	L	X	QB _r	QC _r	QD _r	QE _r	QF _r	QG _r	QH _r	L	QA _r	L
Load	H	H	H	X	X	†	X	X	a	b	c	d	e	f	g	h	a	h

* When one or both output controls are high the eight input/output terminals are disabled to the high-impedance state, however sequential operation or clearing of the register is not affected.

Recommended Operating Conditions

SYMBOL	PARAMETER		54LS299			74LS299			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage,		4.5	5	5.5	4.75	5	5.25	V
I_{OH}	High-level output current,	Q_A thru Q_H	-1			-2.6			mA
		Q_A or Q_H	-0.4			-0.4			
I_{OL}	Low-level output current,	Q_A thru Q_H	12			24			mA
		Q_A or Q_H	4			8			
f_{clock}	Clock frequency,		0	25		0	25		MHz
$t_{w(clock)}$	Width of clock pulse,	Clock high	30			30			ns
		Clock low	10			10			
$t_{w(clear)}$	Width of clear pulse		20			20			ns
t_{su}	Setup time.	Select	35†			35†			ns
		High-level data	20†			20†			
		Low-level data	20†			20†			
		Clear inactive-state	20†			20†			
t_h	Hold time,	Select	10†			10†			ns
		Data	0†			0†			
T_A	Operating free-air temperature.		-55	125		0	70		°C

* Data includes the two serial inputs and the eight input/output data lines.

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER		TEST CONDITIONS		MIN	TYP (Note 1)	MAX	UNIT			
V_{IH}	High-level input voltage				2.0			V			
V_{IL}	Low-level input voltage				54	0.7		V			
					74	0.8					
V_{IK}	Input clamp voltage		$V_{CC} = \text{MIN.}$	$I_I = -18\text{mA}$	-1.5			V			
V_{OH}	High-level output voltage	Q_A thru Q_H	$V_{CC} = \text{MIN.}$	$V_{IH} = 2\text{V}$	54	2.4	3.2	V			
					74	2.4	3.1				
		Q_A or Q_H			$V_{IL} = \text{MAX}$	$I_{OH} = \text{MAX}$	54		2.5	3.4	
							74		2.7	3.4	
V_{OL}	Low-level output voltage	Q_A thru Q_H	$V_{CC} = \text{MIN.}$	$V_{IL} = \text{MAX}$			$I_{OL} = 12\text{mA}$	54, 74	0.25	0.4	V
							$I_{OL} = 24\text{mA}$	74	0.35	0.5	
		Q_A or Q_H			$V_{IH} = \text{MIN.}$	$I_{OL} = 4\text{mA}$	54, 74	0.25	0.4		
						$I_{OL} = 8\text{mA}$	74	0.35	0.5		
I_{OZH}	Off-state output current, high-level voltage applied	Q_A thru Q_H	$V_{CC} = \text{MAX}$	$V_O = 2.7\text{V}$		$V_{IH} = 2\text{V}$	40			μA	
I_{OZL}	Off-state output current low-level voltage applied	Q_A thru Q_H	$V_{CC} = \text{MAX}$	$V_O = 0.4\text{V}$		$V_{IH} = 2\text{V}$	-400			μA	
I_I	Input current at maximum input voltage	S0, S1	$V_{CC} = \text{MAX}$		$V_I = 7\text{V}$	200		μA			
		A thru H			$V_I = 5.5\text{V}$	100					
		Any other			$V_I = 7\text{V}$	100					
I_{IH}	High-level input current	A thru H, S0, S1	$V_{CC} = \text{MAX}$	$V_I = 2.7\text{V}$	40			μA			
		Any other			20						
I_{IL}	Low-level input current	S0, S1	$V_{CC} = \text{MAX}$	$V_I = 0.4\text{V}$	-0.8			mA			
		Any other			-0.4						
I_{OS}	Short-circuit output current	Q_A thru Q_H	$V_{CC} = \text{MAX}$ (Note 2)			-30	-130		mA		
		Q_A or Q_H				-20	-100				
I_{CC}	Supply current		$V_{CC} = \text{MAX}$			33	53		mA		

Note 1. All typical values are at $V_{CC} = 5\text{V}$, $T_A = 25^\circ\text{C}$

Note 2. Not more than one output should be shorted at a time, and the duration should not exceed one second

Switching Characteristics, $V_{CC} = 5V$, $T_A = 25^\circ C$

PARAMETER*	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			See Note3	25	35		MHz
t_{PLH}	Clock	Q_A' or Q_H'	$C_L = 15 \text{ pF}$ $R_L = 2 \text{ k}\Omega$ See Note3		22	33	ns
t_{PHL}					26	39	
t_{PHL}	Clear	Q_A' or Q_H'			27	40	ns
t_{PLH}	Clock	Q_A thru Q_H	$C_L = 45 \text{ pF}$ $R_L = 665 \Omega$ See Note3		17	25	ns
t_{PHL}					26	39	
t_{PHL}	Clear	Q_A thru Q_H			26	40	ns
t_{PZH}	$\bar{G}1, \bar{G}2$	Q_A thru Q_H			13	21	ns
t_{PZL}					19	30	
t_{PHZ}	$\bar{G}1, \bar{G}2$	Q_A thru Q_H	$C_L = 5 \text{ pF}$ $R_L = 665 \Omega$ See Note3		10	15	ns
t_{PLZ}					10	15	

* f_{max} = maximum clock frequency

t_{PLH} = propagation delay time, low to-high-level output

t_{PHL} = propagation delay time, high-to-low-level output

t_{PZH} = output enable time to high level

t_{PZL} = output enable time to low level

t_{PHZ} = output disable time from high level

t_{PLZ} = output disable time from low level

Note 3 For testing f_{max} , all outputs are loaded simultaneously each with C_L and R_L as specified for the propagation times. See load circuits and waveforms on page 3-11