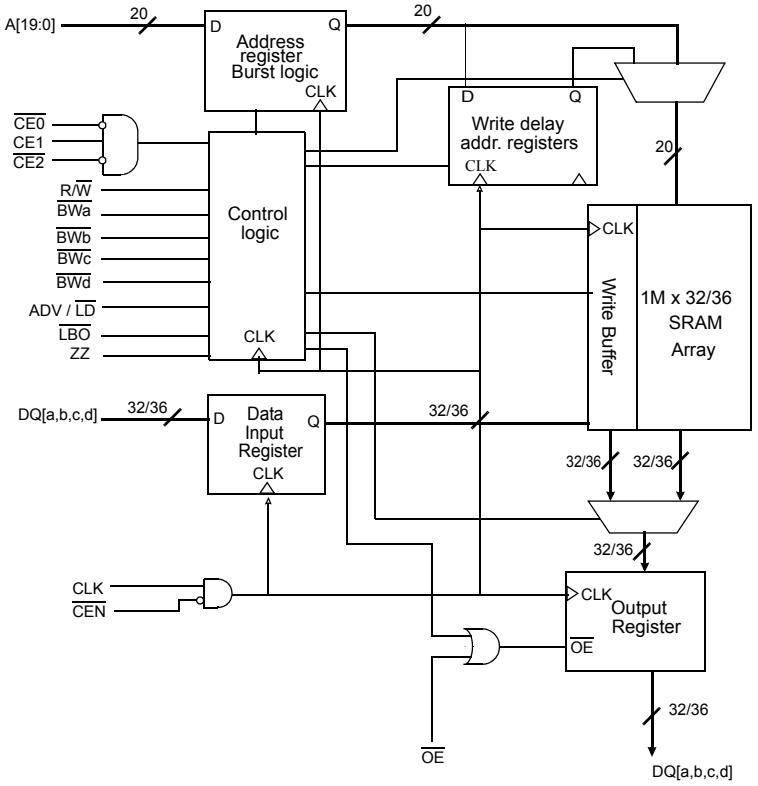
3.3V 1M × 32/36 Pipelined SRAM with NTD™

Features

- Organization: 1,048,576 words × 32 or 36 bits
- NTD™ architecture for efficient bus operation
- Fast clock speeds to 200 MHz
- Fast clock to data access: 3.2/3.5/3.8 ns
- Fast $\overline{OE}$ access time: 3.2/3.5/3.8 ns
- Fully synchronous operation
- Asynchronous output enable control
- Available in 100-pin TQFP and 165-ball BGA packages
- Byte write enables
- Clock enable for operation hold
- Multiple chip enables for easy expansion
- 3.3V core power supply
- 2.5V or 3.3V I/O operation with separate V_{DDQ}
- Self-timed write cycles
- Interleaved or linear burst modes
- Snooze mode for standby operation
- Boundary Scan using IEEE 1149.1 JTAG function is available in 165 Ball BGA Package only.

Logic block diagram



Selection guide

	-200	-166	-133	Units
Minimum cycle time	5	6	7.5	ns
Maximum clock frequency	200	166	133	MHz
Maximum clock access time	3.2	3.5	3.8	ns
Maximum operating current	450	400	350	mA
Maximum standby current	170	150	140	mA
Maximum CMOS standby current (DC)	90	90	90	mA

32 Mb Synchronous SRAM products list[1,2]

Org	Part Number	Mode	Speed
2MX18	AS7C332MPFS18A	PL-SCD	200/166/133 MHz
1MX32	AS7C331MPFS32A	PL-SCD	200/166/133 MHz
1MX36	AS7C331MPFS36A	PL-SCD	200/166/133 MHz
2MX18	AS7C332MPFD18A	PL-DCD	200/166/133 MHz
1MX32	AS7C331MPFD32A	PL-DCD	200/166/133 MHz
1MX36	AS7C331MPFD36A	PL-DCD	200/166/133 MHz
2MX18	AS7C332MFT18A	FT	7.5/8.5/10 ns
1MX32	AS7C331MFT32A	FT	7.5/8.5/10 ns
1MX36	AS7C331MFT36A	FT	7.5/8.5/10 ns
2MX18	AS7C332MNTD18A	NTD-PL	200/166/133 MHz
1MX32	AS7C331MNTD32A	NTD-PL	200/166/133 MHz
1MX36	AS7C331MNTD36A	NTD-PL	200/166/133 MHz
2MX18	AS7C332MNTF18A	NTD-FT	7.5/8.5/10 ns
1MX32	AS7C331MNTF32A	NTD-FT	7.5/8.5/10 ns
1MX36	AS7C331MNTF36A	NTD-FT	7.5/8.5/10 ns

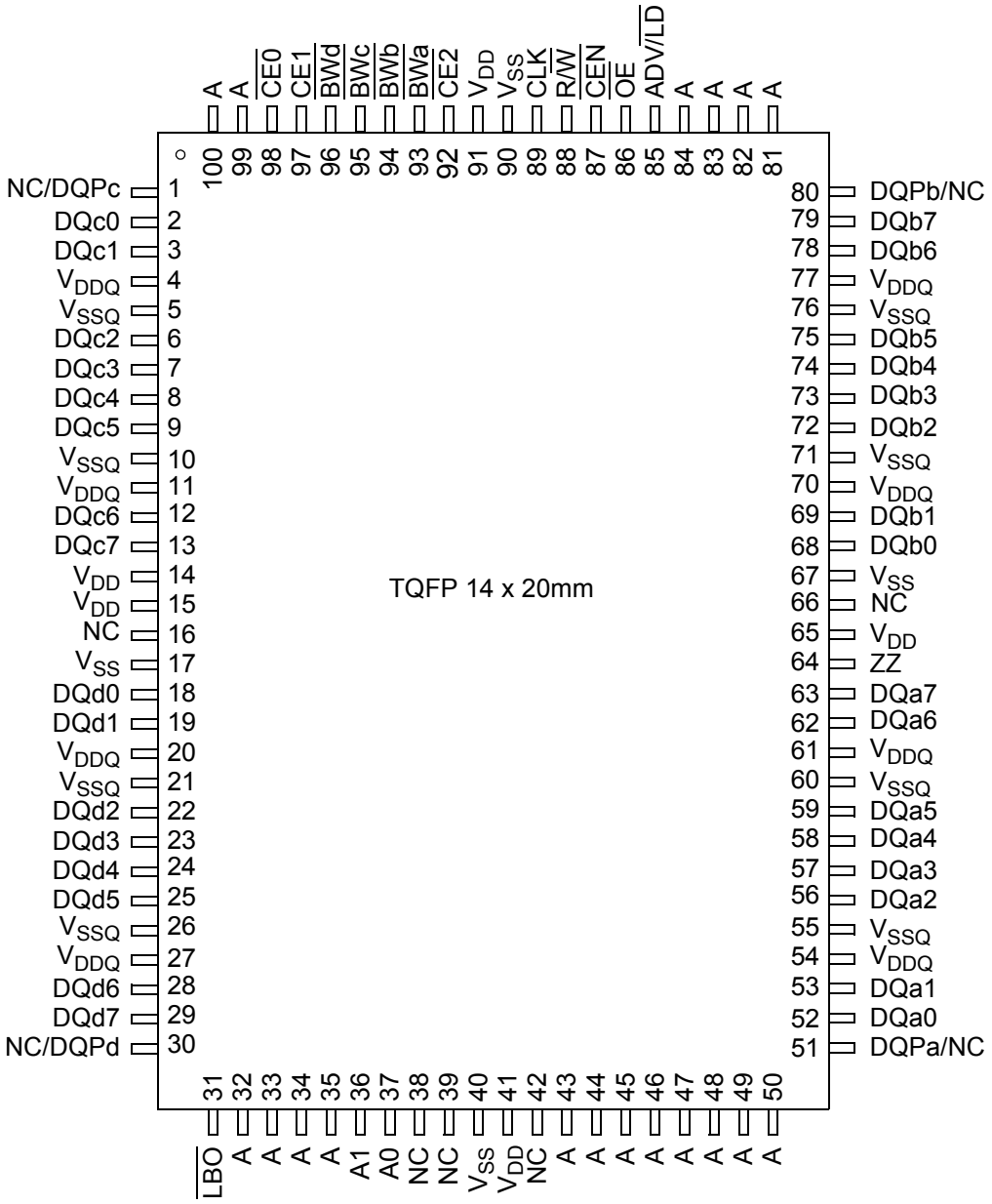
1 Core Power Supply: VDD = 3.3V $\pm$ 0.165V
2 I/O Supply Voltage: VDDQ = 3.3V $\pm$ 0.165V for 3.3V I/O
VDDQ = 2.5V $\pm$ 0.125V for 2.5V I/O

PL-SCD : Pipelined Burst Synchronous SRAM - Single Cycle Deselect
PL-DCD : Pipelined Burst Synchronous SRAM - Double Cycle Deselect
FT : Flow-through Burst Synchronous SRAM
NTD[1]-PL : Pipelined Burst Synchronous SRAM with NTD™
NTD-FT : Flow-through Burst Synchronous SRAM with NTD™

1. NTD: No Turnaround Delay. NTD™ is a trademark of Alliance Semiconductor Corporation. All trademarks mentioned in this document are the property of their respective owners.

Pin and ball assignment

100-pin TQFP - top view



Note: For pins 1, 30, 51, and 80, NC applies to the x32 configuration.
DQPn applies to the x36 configuration.

165-ball BGA - top view for 1M X 36

	1	2	3	4	5	6	7	8	9	10	11
A	NC	A	$\overline{CE0}$	$\overline{BWc}$	$\overline{BWb}$	$\overline{CE2}$	$\overline{CEN}$	ADV/$\overline{LD}$	A	A	NC
B	NC	A	CE1	$\overline{BWd}$	$\overline{BWa}$	CLK	R/$\overline{W}$	$\overline{OE}$	A	A	NC
C	DQPc	NC	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	DQPb
D	DQc	DQc	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQb	DQb
E	DQc	DQc	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQb	DQb
F	DQc	DQc	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQb	DQb
G	DQc	DQc	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQb	DQb
H	V_{DD}	NC	NC	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	NC	NC	ZZ
J	DQd	DQd	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQa	DQa
K	DQd	DQd	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQa	DQa
L	DQd	DQd	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQa	DQa
M	DQd	DQd	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQa	DQa
N	DQPd	NC	V_{DDQ}	V_{SS}	NC	NC	NC	V_{SS}	V_{DDQ}	NC	DQPa
P	NC	NC	A	A	TDI	A1[1]	TDO	A	A	A	NC
R	$\overline{LBO}$	A	A	A	TMS	A0[1]	TCK	A	A	A	A

1 A0 and A1 are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.

Note: Balls C1, N1, C11, N11 are NC for AS7C331MNTD32A

Functional description

The AS7C331MNTD32A/36A family is a high performance CMOS 32 Mbit Synchronous Static Random Access Memory (SRAM) organized as 1,048,576 words × 32 or 36 bits and incorporates a LATE LATE Write.

This variation of the 32Mb synchronous SRAM uses the No Turnaround Delay (NTD™) architecture, featuring an enhanced write operation that improves bandwidth over pipelined burst devices. In a normal pipelined burst device, the write data, command, and address are all applied to the device on the same clock edge. If a read command follows this write command, the system must wait for two 'dead' cycles for valid data to become available. These dead cycles can significantly reduce overall bandwidth for applications requiring random access or read-modify-write operations.

NTD™ devices use the memory bus more efficiently by introducing a write latency which matches the two-cycle pipelined or one-cycle flow-through read latency. Write data is applied two cycles after the write command and address, allowing the read pipeline to clear. With NTD™, write and read operations can be used in any order without producing dead bus cycles.

Assert R/$\overline{W}$ low to perform write cycles. Byte write enable controls write access to specific bytes, or can be tied low for full 32/36 bit writes. Write enable signals, along with the write address, are registered on a rising edge of the clock. Write data is applied to the device two clock cycles later. Unlike some asynchronous SRAMs, output enable $\overline{OE}$ does not need to be toggled for write operations; it can be tied low for normal operations. Outputs go to a high impedance state when the device is de-selected by any of the three chip enable inputs. In pipelined mode, a two cycle deselect latency allows pending read or write operations to be completed.

Use the ADV (burst advance) input to perform burst read, write and deselect operations. When ADV is high, external addresses, chip select, R/$\overline{W}$ pins are ignored, and internal address counters increment in the count sequence specified by the $\overline{LBO}$ control. Any device operations, including burst, can be stalled using the $\overline{CEN}$=1, the clock enable input.

The AS7C331MNTD32A/36A operates with a 3.3V ± 5% power supply for the device core (V_{DD}). DQ circuits use a separate power supply (V_{DDQ}) that operates across 3.3V or 2.5V ranges. These devices are available in a 100-pin TQFP and 165-ball BGA packages.

Capacitance

Parameter	Symbol	Test conditions	Min	Max	Unit
Input capacitance	C_{IN}*	V_{in} = 0V	-	5	pF
I/O capacitance	$C_{I/O}$*	V_{in} = V_{out} = 0V	-	7	pF

*Guaranteed not tested

TQFP and BGA thermal resistance

Description	Conditions		Symbol	Typical	Units
Thermal resistance (junction to ambient)[1]	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51	1–layer	θ_{JA}	40	°C/W
		4–layer	θ_{JA}	22	°C/W
Thermal resistance (junction to top of case)[1]			θ_{JC}	8	°C/W

1 This parameter is sampled

Signal descriptions

Signal	I/O	Properties	Description
CLK	I	CLOCK	Clock. All inputs except $\overline{OE}$, $\overline{LBO}$, and ZZ are synchronous to this clock.
$\overline{CEN}$	I	SYNC	Clock enable. When de-asserted high, the clock input signal is masked.
A, A0, A1	I	SYNC	Address. Sampled when all chip enables are active and ADV/$\overline{LD}$ is asserted.
DQ[a,b,c,d]	I/O	SYNC	Data. Driven as output when the chip is enabled and $\overline{OE}$ is active.
$\overline{CE0}$, CE1, $\overline{CE2}$	I	SYNC	Synchronous chip enables. Sampled at the rising edge of CLK, when ADV/$\overline{LD}$ is asserted. Are ignored when ADV/$\overline{LD}$ is high.
ADV/$\overline{LD}$	I	SYNC	Advance or Load. When sampled high, the internal burst address counter will increment in the order defined by the $\overline{LBO}$ input value. (refer to table on page 2) When low, a new address is loaded.
R/$\overline{W}$	I	SYNC	A high during LOAD initiates a READ operation. A low during LOAD initiates a WRITE operation. Is ignored when ADV/$\overline{LD}$ is high.
$\overline{BW[a,b,c,d]}$	I	SYNC	Byte write enables. Used to control write on individual bytes. Sampled along with WRITE command and BURST WRITE.
$\overline{OE}$	I	ASYNC	Asynchronous output enable. I/O pins are not driven when $\overline{OE}$ is inactive.
$\overline{LBO}$	I	STATIC	Selects Burst mode. When tied to V_{DD} or left floating, device follows interleaved Burst order. When driven Low, device follows linear Burst order. *This signal is internally pulled High.*
TDO	O	SYNC	Serial data-out to the JTAG circuit. Delivers data on the negative edge of TCK. (BGA only)
TDI	I	SYNC	Serial data-in to the JTAG circuit. Sampled on the rising edge of TCK. (BGA only)
TMS	I	SYNC	This pin controls the Test Access Port state machine. Sampled on the rising edge of TCK. (BGA only)
TCK	O	SYNC	Serial data-out to the JTAG circuit. Delivers data on the negative edge of TCK. (BGA only)
ZZ	I	ASYNC	Snooze. Places device in low power mode; data is retained. Connect to GND if unused.
NC	-	-	No connect

Snooze Mode

SNOOZE MODE is a low current, power-down mode in which the device is deselected and current is reduced to ISB2. The duration of SNOOZE MODE is dictated by the length of time the ZZ is in a High state.

The ZZ pin is an asynchronous, active high input that causes the device to enter SNOOZE MODE.

When the ZZ pin becomes a logic High, ISB2 is guaranteed after the time t_{ZZI} is met. After entering SNOOZE MODE, all inputs except ZZ become disabled and all outputs go to High-Z. Any operation pending when entering SNOOZE MODE is not guaranteed to successful complete. Therefore, SNOOZE MODE (READ or WRITE) must not be initiated until valid pending operations are completed. similarly, when exiting SNOOZE MODE during tPUS, only a DESELECT or READ cycle should be given while the SRAM is transitioning out of SNOOZE MODE.

Burst order

Interleaved burst order $\overline{LBO}$ = 1					Linear burst order $\overline{LBO}$ = 0				
	A1 A0	A1 A0	A1 A0	A1 A0		A1 A0	A1 A0	A1 A0	A1 A0
Starting address	0 0	0 1	1 0	1 1	Starting Address	0 0	0 1	1 0	1 1
First increment	0 1	0 0	1 1	1 0	First increment	0 1	1 0	1 1	0 0
Second increment	1 0	1 1	0 0	0 1	Second increment	1 0	1 1	0 0	0 1
Third increment	1 1	1 0	0 1	0 0	Third increment	1 1	0 0	0 1	1 0

Synchronous truth table[5,6,7,8,9,11]

$\overline{CE0}$	CE1	$\overline{CE2}$	ADV/$\overline{LD}$	R/$\overline{W}$	$\overline{BWn}$	$\overline{OE}$	$\overline{CEN}$	Address source	CLK	Operation	DQ	Notes
H	X	X	L	X	X	X	L	NA	L to H	DESELECT Cycle	High-Z	
X	X	H	L	X	X	X	L	NA	L to H	DESELECT Cycle	High-Z	
X	L	X	L	X	X	X	L	NA	L to H	DESELECT Cycle	High-Z	
X	X	X	H	X	X	X	L	NA	L to H	CONTINUE DESELECT Cycle	High-Z	1
L	H	L	L	H	X	L	L	External	L to H	READ Cycle (Begin Burst)	Q	
X	X	X	H	X	X	L	L	Next	L to H	READ Cycle (Continue Burst)	Q	1,10
L	H	L	L	H	X	H	L	External	L to H	NOP/DUMMY READ (Begin Burst)	High-Z	2
X	X	X	H	X	X	H	L	Next	L to H	DUMMY READ (Continue Burst)	High-Z	1,2,10
L	H	L	L	L	L	X	L	External	L to H	WRITE CYCLE (Begin Burst)	D	3
X	X	X	H	X	L	X	L	Next	L to H	WRITE CYCLE (Continue Burst)	D	1,3,10
L	H	L	L	L	H	X	L	External	L to H	NOP/WRITE ABORT (Begin Burst)	High-Z	2,3
X	X	X	H	X	H	X	L	Next	L to H	WRITE ABORT (Continue Burst)	High-Z	1,2,3, 10
X	X	X	X	X	X	X	H	Current	L to H	INHIBIT CLOCK	-	4

Key: X = Don't Care, H = HIGH, L = LOW. $\overline{BW}$n = H means all byte write signals ($\overline{BW}$a, $\overline{BW}$b, $\overline{BW}$c, and $\overline{BW}$d) are HIGH. $\overline{BW}$n = L means one or more byte write signals are LOW.

Notes:

1 CONTINUE BURST cycles, whether READ or WRITE, use the same control inputs. The type of cycle performed (READ or WRITE) is chose in the initial BEGIN BURST cycle. A CONINUE DESELECT cycle can only be entered if a DESELECT CYCLE is executed first.

2 DUMMY READ and WRITE ABORT cycles can be considered NOPs because the device performs no external operation. A WRITE ABORT means a WRITE command is given, but no operation is performed.

3 $\overline{OE}$ may be wired LOW to minimize the number of control signal to the SRAM. The device will automatically turn off the output drivers during a WRITE cycle. $\overline{OE}$ may be used when the bus turn-on and turn-off times do not meet an application's requirements.

4 If an INHIBIT CLOCK command occurs during a READ operation, the DQ bus will remain active (Low-Z). If it occurs during a WRITE cycle, the bus will remain in High-Z. No WRITE operations will be performed during the INHIBIT CLOCK cycle.

5 $\overline{BW}$a enables WRITEs to byte "a" (DQa pins/balls); $\overline{BW}$b enables WRITEs to byte "b" (DQb pins/balls); $\overline{BW}$c enables WRITEs to byte "c" (DQc pins/balls); $\overline{BW}$d enables WRITEs to byte "d" (DQd pins/balls).

6 All inputs except $\overline{OE}$ and ZZ must meet setup and hold times around the rising edge (LOW to HIGH) of CLK.

7 Wait states are inserted by setting $\overline{CEN}$ HIGH.

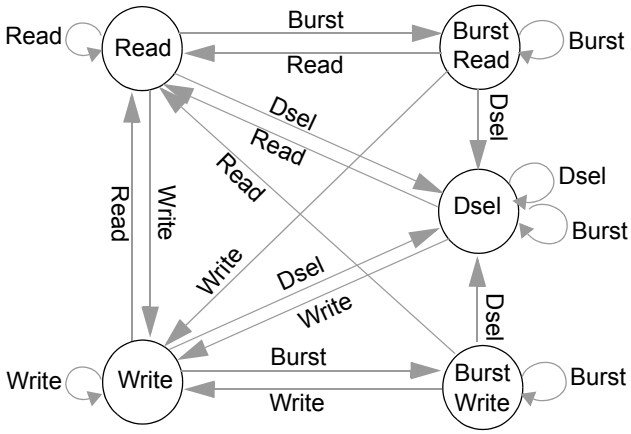
8 This device contains circuitry that will ensure that the outputs will be in High-Z during power-up.

9 The device incorporates a 2-bit burst counter. Address wraps to the initial address every fourth BURST CYCLE.

10 The address counter is incremented for all CONTINUE BURST cycles.

11. ZZ pin is always Low in this truth table.

State diagram for NTD SRAM



Absolute maximum ratings

Parameter	Symbol	Min	Max	Unit
Power supply voltage relative to GND	V_{DD}, V_{DDQ}	–0.5	+4.6	V
Input voltage relative to GND (input pins)	V_{IN}	–0.5	V_{DD} + 0.5	V
Input voltage relative to GND (I/O pins)	V_{IN}	–0.5	V_{DDQ} + 0.5	V
Power dissipation	P_d	–	1.8	W
Short circuit output current	I_{OUT}	–	20	mA
Storage temperature (TQFP)	T_{stg} (TQFP)	–65	+150	°C
Storage temperature (BGA)	T_{stg} (BGA)	–65	+125	°C
Temperature under bias	T_{bias}	–65	+135	°C

Stresses greater than those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect reliability.

Recommended operating conditions at 3.3V I/O

Parameter	Symbol	Min	Nominal	Max	Unit
Supply voltage for inputs	V_{DD}	3.135	3.3	3.465	V
Supply voltage for I/O	V_{DDQ}	3.135	3.3	3.465	V
Ground supply	Vss	0	0	0	V

Recommended operating conditions at 2.5V I/O

Parameter	Symbol	Min	Nominal	Max	Unit
Supply voltage for inputs	V_{DD}	3.135	3.3	3.465	V
Supply voltage for I/O	V_{DDQ}	2.375	2.5	2.625	V
Ground supply	Vss	0	0	0	V

DC electrical characteristics for 3.3V I/O operation

Parameter	Sym	Conditions	Min	Max	Unit
Input leakage current[1]	$\|I_{LI}\|$	V_{DD} = Max, 0V ≤ V_{IN} ≤ V_{DD}	-2	2	µA
Output leakage current	$\|I_{LO}\|$	OE ≥ V_{IH}, V_{DD} = Max, 0V ≤ V_{OUT} ≤ V_{DDQ}	-2	2	µA
Input high (logic 1) voltage	V_{IH}	Address and control pins	2*	V_{DD}+0.3	V
		I/O pins	2*	V_{DDQ}+0.3	
Input low (logic 0) voltage	V_{IL}	Address and control pins	-0.3**	0.8	V
		I/O pins	-0.5**	0.8	
Output high voltage	V_{OH}	I_{OH} = –4 mA, V_{DDQ} = 3.135V	2.4	–	V
Output low voltage	V_{OL}	I_{OL} = 8 mA, V_{DDQ} = 3.465V	–	0.4	V

1 $\overline{LBO}$, and ZZ pins and the 165 BGA JTAG pins (TMS, TDI, and TCK) have an internal pull-up or pull-down, and input leakage = ±10 µA.

DC electrical characteristics for 2.5V I/O operation

Parameter	Sym	Conditions	Min	Max	Unit
Input leakage current	$\|I_{LI}\|$	V_{DD} = Max, 0V ≤ V_{IN} ≤ V_{DD}	-2	2	µA
Output leakage current	$\|I_{LO}\|$	OE ≥ V_{IH}, V_{DD} = Max, 0V ≤ V_{OUT} ≤ V_{DDQ}	-2	2	µA
Input high (logic 1) voltage	V_{IH}	Address and control pins	1.7*	V_{DD}+0.3	V
		I/O pins	1.7*	V_{DDQ}+0.3	V
Input low (logic 0) voltage	V_{IL}	Address and control pins	-0.3**	0.7	V
		I/O pins	-0.3**	0.7	V
Output high voltage	V_{OH}	I_{OH} = –4 mA, V_{DDQ} = 2.375V	1.7	–	V
Output low voltage	V_{OL}	I_{OL} = 8 mA, V_{DDQ} = 2.625V	–	0.7	V

*V_{IH} max < VDD +1.5V for pulse width less than 0.2 X t_{CYC}

**V_{IL} min = -1.5 for pulse width less than 0.2 X t_{CYC}

I_{DD} operating conditions and maximum limits

Parameter	Sym	Test conditions	-200	-166	-133	Unit
Operating power supply current[1]	I_{CC}	$\overline{CE0}$ ≤ V_{IL}, CE1 ≥ V_{IH}, $\overline{CE2}$ ≤ V_{IL}, f = f_{Max}, I_{OUT} = 0 mA, ZZ ≤ V_{IL}	450	400	350	mA
Standby power supply current	I_{SB}	All V_{IN} ≤ 0.2V or ≥ V_{DD} – 0.2V, Deselected, f = f_{Max}, ZZ ≤ V_{IL}	170	150	140	mA
	I_{SB1}	Deselected, f = 0, ZZ ≤ 0.2V, all V_{IN} ≤ 0.2V or ≥ V_{DD} – 0.2V	90	90	90	
	I_{SB2}	Deselected, f = f_{Max}, ZZ ≥ V_{DD} – 0.2V, all V_{IN} ≤ V_{IL} or ≥ V_{IH}	80	80	80	

1 I_{CC} given with no output loading. I_{CC} increases with faster cycle times and greater output loading.

Timing characteristics over operating range

Parameter	Sym	-200		-166		-133		Unit	Notes[1]
		Min	Max	Min	Max	Min	Max		
Clock frequency	F_{MAX}	–	200	–	166	–	133	MHz	
Cycle time	t_{CYC}	5	–	6	–	7.5	–	ns	
Clock access time	t_{CD}	–	3.2	–	3.5	–	3.8	ns	
Output enable low to data valid	t_{OE}	–	3.2	–	3.5	–	3.8	ns	
Clock high to output low Z	t_{LZC}	0	–	0	–	0	–	ns	2,3,4
Data output invalid from clock high	t_{OH}	1.5	–	1.5	–	1.5	–	ns	2
Output enable low to output low Z	t_{LZOE}	0	–	0	–	0	–	ns	2,3,4
Output enable high to output high Z	t_{HZOE}	–	3.0	–	3.4	–	3.8	ns	2,3,4
Clock high to output high Z	t_{HZC}	–	3.0	–	3.4	–	3.8	ns	2,3,4
Output enable high to invalid output	t_{OHOE}	0	–	0	–	0	–	ns	
Clock high pulse width	t_{CH}	2.0	–	2.4	–	2.4	–	ns	5
Clock low pulse width	t_{CL}	2.0	–	2.4	–	2.4	–	ns	5
Address and Control setup to clock high	t_{AS}	1.4	–	1.5	–	1.5	–	ns	6
Data setup to clock high	t_{DS}	1.4	–	1.5	–	1.5	–	ns	6
Write setup to clock high	t_{WS}	1.4	–	1.5	–	1.5	–	ns	6, 7
Chip select setup to clock high	t_{CSS}	1.4	–	1.5	–	1.5	–	ns	6, 8
Address hold from clock high	t_{AH}	0.4	–	0.5	–	0.5	–	ns	6
Data hold from clock high	t_{DH}	0.4	–	0.5	–	0.5	–	ns	6
Write hold from clock high	t_{WH}	0.4	–	0.5	–	0.5	–	ns	6, 7
Chip select hold from clock high	t_{CSH}	0.4	–	0.5	–	0.5	–	ns	6, 8
Clock enable setup to clock high	t_{CENS}	1.4	–	1.5	–	1.5	–	ns	6
Clock enable hold from clock high	t_{CENH}	0.4	–	0.5	–	0.5	–	ns	6
ADV setup to clock high	t_{ADVS}	1.4	–	1.5	–	1.5	–	ns	6
ADV hold from clock high	t_{ADVH}	0.4	–	0.5	–	0.5	–	ns	6
ZZ High to Power down	t_{PDS}	2	–	2	–	2	–	cycle	
ZZ Low to Power up	t_{PUS}	2	–	2	–	2	–	cycle	

1 See “Notes” on page 23

Snooze Mode Electrical Characteristics

Description	Conditions	Symbol	Min	Max	Units
Current during Snooze Mode	$ZZ \geq V_{IH}$	I_{SB2}		80	mA
ZZ active to input ignored		t_{PDS}	2		cycle
ZZ inactive to input sampled		t_{PUS}	2		cycle
ZZ active to SNOOZE current		t_{ZZI}		2	cycle
ZZ inactive to exit SNOOZE current		t_{RZZI}	0		

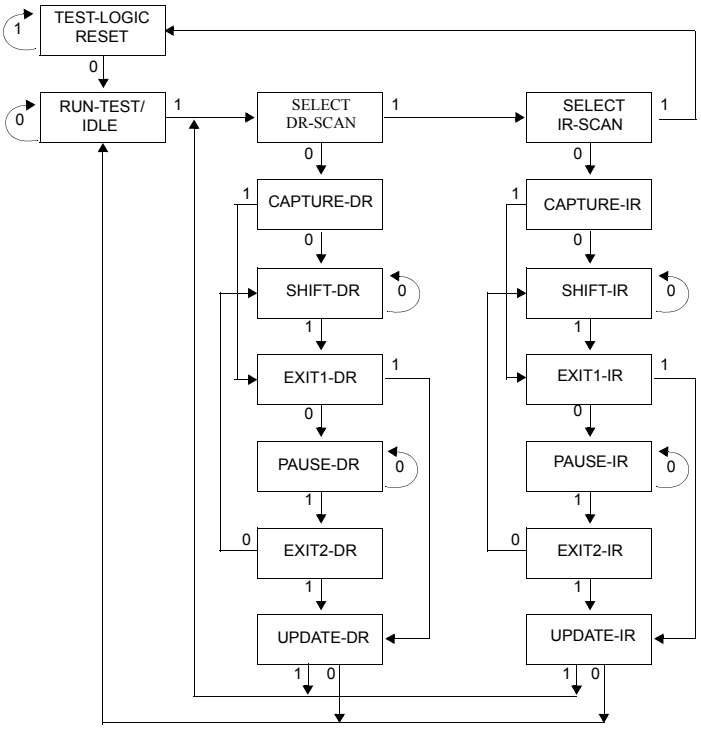
IEEE 1149.1 serial boundary scan (JTAG)

The SRAM incorporates a serial boundary scan test access port (TAP). The port operates in accordance with IEEE Standard 1149.1-1990. The SRAM contains a TAP controller, instruction register, boundary scan register, bypass register, and ID register.

Disabling the JTAG feature

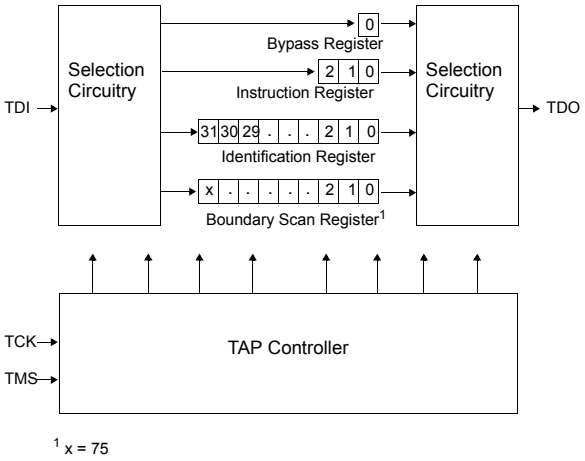
If the JTAG function is not being implemented, TCK should be grounded to avoid mid-level input. At power-up, the device will come up in a reset state which will not interfere with the operation of the device.

TAP controller state diagram



Note: The 0 or 1 next to each state represents the value of TMS at the rising edge of TCK.

TAP controller block diagram



1 x = 75

Test access port (TAP)

Test clock (TCK)

The test clock is used only with the TAP controller. All inputs are captured on the rising edge of TCK. All outputs are driven from the falling edge of TCK.

Test mode select (TMS)

The TAP controller receives commands from TMS input. It is sampled on the rising edge of TCK. You can leave this pin/ball unconnected if the TAP is not used. The pin/ball is pulled up internally, resulting in a logic high level.

Test data-in (TDI)

The TDI pin/ball serially inputs information into the registers and can be connected to the input of any of the registers. The register between TDI and TDO is chosen by the instruction that is loaded into the TAP instruction register. For information on

loading the instruction register, see the TAP Controller State Diagram. TDI is internally pulled up and can be unconnected if the TAP is unused in an application. TDI is connected to the most significant bit (MSB) of any register.

Test data-out (TDO)

The TDO output pin/ball serially clocks data-out from the registers. The output is active depending upon the current state of the TAP state machine. The output changes on the falling edge of TCK. TDO is connected to the least significant bit (LSB) of any register. (See the TAP Controller State Diagram.)

Performing a TAP RESET

You can perform a RESET by forcing TMS high (V_{DD}) for five rising edges of TCK. This RESET does not affect the operation of the SRAM and can be performed while the SRAM is operating.

At power-up, the TAP is reset internally to ensure that TDO comes up in a high-Z state.

TAP registers

Registers are connected between the TDI and TDO pins/balls. They allow data to be scanned into and out of the SRAM test circuitry. Only one register can be selected at a time through the instruction register. Data is serially loaded into the TDI pin/ball on the rising edge of TCK. Data is output on the TDO pin/ball on the falling edge of TCK.

Instruction register

You can serially load three-bit instructions into the instruction register. The register is loaded when it is placed between the TDI and TDO pins/balls as shown in the TAP Controller Block Diagram. The instruction register is loaded with the IDCODE instruction at power up and also if the controller is placed in a reset state, as described in the previous section.

When the TAP controller is in the Capture-IR state, the two least significant bits are loaded with a binary “01” pattern to allow for fault isolation of the board-level series test data path.

Bypass register

To save time when serially shifting data through registers, it is sometimes advantageous to skip certain chips. The bypass register is a single-bit register that can be placed between the TDI and TDO pins/balls. This allows data to be shifted through the SRAM with minimal delay. The bypass register is set low (Vss) when the BYPASS instruction is executed.

Boundary scan register

The boundary scan register is connected to all the input and bidirectional pins/balls on the SRAM. The chip has a 76-bit-long register.

The boundary scan register is loaded with the contents of the RAM I/O ring when the TAP controller is in the Capture-DR state and is then placed between the TDI and TDO pins/balls when the controller is moved to the Shift-DR state. The EXTEST, SAMPLE/PRELOAD, and SAMPLE Z instructions can be used to capture the contents of the I/O ring.

The boundary scan order table shows the order in which the bits are connected. Each bit corresponds to one of the bumps on the SRAM package. The most significant bit (MSB) of the register is connected to TDI, and the least significant bit (LSB) is connected to TDO.

Identification (ID) register

The ID register has a vendor code and other information described in the Identification Register Definitions table. The ID register is loaded with a vendor-specific, 32-bit code during the Capture-DR state when the IDCODE command is loaded in the instruction register. The IDCODE is hardwired into the SRAM and can be shifted out when the TAP controller is in the Shift-DR state.

TAP instruction set

Eight different instructions are possible with the 3-bit instruction register. All combinations are listed in the Instruction Codes table. One of these instructions is reserved and should not be used.

Instructions are loaded into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and TDO. During this state, instructions are shifted through the instruction register through the TDI and TDO pins/balls. To execute the instruction once it is shifted in, the TAP controller needs to be moved into the Update-IR state.

EXTEST

EXTEST is a mandatory 1149.1 instruction which is to be executed whenever the instruction register is loaded with all 0s. EXTEST is not implemented in this SRAM TAP controller, and therefore this device is not compliant to 1149.1.

The TAP controller does recognize an all-0 instruction. When an EXTEST instruction is loaded into the instruction register, the SRAM responds as if a SAMPLE/PRELOAD instruction has been loaded. There is one difference between the two instructions, unlike the SAMPLE/PRELOAD instruction, EXTEST places the SRAM outputs in a High-Z state.

IDCODE

The IDCODE instruction is loaded into the instruction register upon power-up or whenever the TAP controller is given a test logic reset state. The IDCODE instruction causes a vendor-specific, 32-bit code to be loaded into the identification register. It also places the identification register between the TDI and TDO pins/balls and allows the IDCODE to be shifted out of the device when the TAP controller enters the Shift-DR state.

SAMPLE Z

The SAMPLE Z instruction causes the boundary scan register to be connected between the TDI and TDO pins/balls when the TAP controller is in a Shift-DR state. It also places all SRAM outputs into a high-Z state.

SAMPLE/PRELOAD

SAMPLE/PRELOAD is a Standard 1149.1 mandatory public instruction. When the SAMPLE/PRELOAD instruction is loaded in the Instruction Register, moving the TAP controller into the Capture-DR state loads the data in the RAM's input and I/O buffers into the Boundary Scan Register. Boundary Scan Register locations are not associated with an input or I/O pin, and are loaded with the default state identified in the Boundary Scan Chain table at the end of this section of the datasheet.Because the RAM clock is independent from the TAP clock (TCK) it is possible for the TAP to attempt to capture the I/O ring contents while the input buffers are in transition (i.e. in a metastable state). Although allowing the TAP to sample metastable inputs will not harm the device, repeatable results cannot be accepted. RAM input signals must be stabilized for long enough to meet the TAP's input data capture set-up plus hold time (tCS plus tCH). The RAM's clock inputs need not be paused for any other TAP operation except capturing the I/O ring contents into the boundary Scan Register. Moving the controller to Shift-DR state then places the boundary scan register between the TDI and TDO pins.

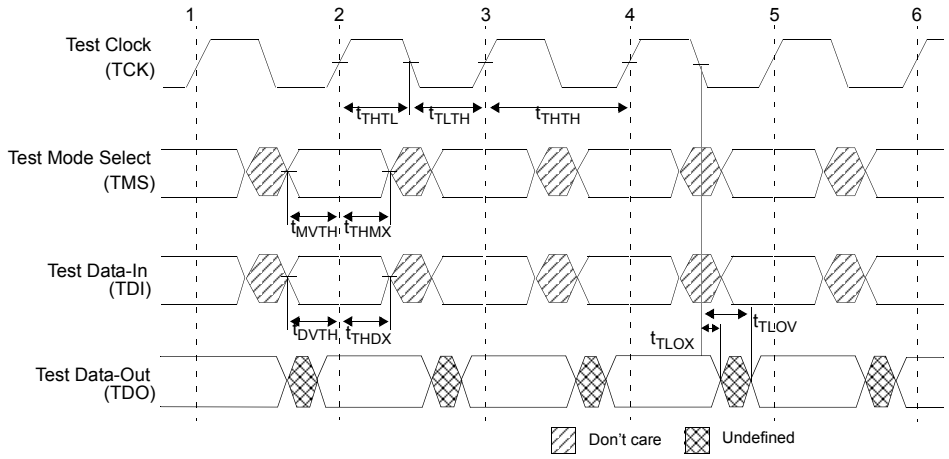
BYPASS

The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board. When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a Shift-DR state, the bypass register is placed between TDI and TDO.

RESERVED

Do not use a reserved instruction. These instructions are not implemented but are reserved for future use.

TAP timing diagram



TAP AC electrical characteristics

For notes 1 and 2, +10°C ≤ T_J ≤ +110°C and +2.4V ≤ V_{DD} ≤ +2.6V.

Description	Symbol	Min	Max	Units
Clock				
Clock cycle time	^{t}THTH	50		ns
Clock frequency	^{F}TF		20	MHz
Clock high time	^{t}THTL	20		ns
Clock low time	^{t}TLTH	20		ns
Output Times				
TCK low to TDO unknown	^{t}TLOX	0		ns
TCK low to TDO valid	^{t}TLOV		10	ns
TDI valid to TCK high	^{t}DVTH	5		ns
TCK high to TDI invalid	^{t}THDX	5		ns
Setup Times				
TMS setup	^{t}MVTH	5		ns
Capture setup	^{t}CS[1]	5		ns
Hold Times				
TMS hold	^{t}THMX	5		ns
Capture hold	^{t}CH[1]	5		ns

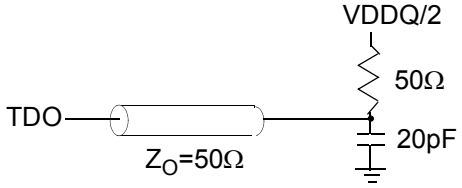
1 ^{t}CS and ^{t}CH refer to the setup and hold time requirements of latching data from the boundary scan register.

2 Test conditions are specified using the load in the figure TAP AC output load equivalent.

TAP AC test conditions

Input pulse levels. . . . . Vss to V_{DD}
Input rise and fall times. . . . . 1 ns
Input timing reference levels. . . . . $V_{DDQ}/2$
Output reference levels . . . . . $V_{DDQ}/2$
Test load termination supply voltage. . . . $V_{DDQ}/2$

TAP AC output load equivalent



3.3V V_{DD}, TAP DC electrical characteristics and operating conditions

($+10^oC \le T_J \le +110^oC$ and $+3.135V \le V_{DD} \le +3.465V$ unless otherwise noted)

Description	Conditions	Symbol	Min	Max	Units	Notes
Input high (logic 1) voltage		V_{IH}	2.0	V_{DD} + 0.3	V	1, 2
Input low (logic 0) voltage		V_{IL}	-0.3	0.8	V	1, 2
Input leakage current	$0V \le V_{IN} \le V_{DD}$	IL_I	-5.0	5.0	µA	
Output leakage current	Outputs disabled, $0V \le V_{IN} \le V_{DDQ}$(DQx)	IL_O	-5.0	5.0	µA	
Output low voltage	I_{OLC} = 100µA	V_{OL1}		0.7	V	1
Output low voltage	I_{OLT} = 2mA	V_{OL2}		0.8	V	1
Output high voltage	I_{OHS} = -100µA	V_{OH1}	2.9		V	1
Output high voltage	I_{OHT} = -2mA	V_{OH2}	2.0		V	1

2.5V V_{DD}, TAP DC electrical characteristics and operating conditions

($+10^oC \le T_J \le +110^oC$ and $+2.4V \le V_{DD} \le +2.6V$ unless otherwise noted)

Description	Conditions	Symbol	Min	Max	Units	Notes
Input high (logic 1) voltage		V_{IH}	1.7	V_{DD} + 0.3	V	1, 2
Input low (logic 0) voltage		V_{IL}	-0.3	0.7	V	1, 2
Input leakage current	$0V \le V_{IN} \le V_{DD}$	IL_I	-5.0	5.0	µA	
Output leakage current	Outputs disabled, $0V \le V_{IN} \le V_{DDQ}$(DQx)	IL_O	-5.0	5.0	µA	
Output low voltage	I_{OLC} = 100µA	V_{OL1}		0.2	V	1
Output low voltage	I_{OLT} = 2mA	V_{OL2}		0.7	V	1
Output high voltage	I_{OHS} = -100µA	V_{OH1}	2.1		V	1
Output high voltage	I_{OHT} = -2mA	V_{OH2}	1.7		V	1

1. All voltage referenced to V_{SS}(GND).
2. Overshoot: $V_{IH}(AC) \le V_{DD} + 1.5V$ for $t \le {}^tKHKH/2$

   Undershoot:$V_{IL}(AC) \ge -0.5$ for $t \le {}^tKHKH/2$

   Power-up: $V_{IH} \le +2.6V$ and $V_{DD} \le 2.4V$ and $V_{DDQ} \le 1.4V$ for $t \le 200ms$

   During normal operation, V_{DDQ} must not exceed V_{DD}. Control input signals (such as $\overline{LD}$, R/$\overline{W}$, etc.) may not have pulsed widths less than t_{KHKL}(Min) or operate at frequencies exceeding f_{KF}(Max).

Identification register definitions

Instruction field	1M x 36	Description
Revision number (31:28)	xxxx	Reserved for version number.
Device depth (27:24)	1010	Defines the depth of 1M words.
Device width (23:21)	011	Defines the width of x32 or x36 bits.
Device ID (20:12)	000001111	Defines product code.
Allinace JEDEC ID code (11:1)	000001010010	Allows unique identification of SRAM vendor.
ID register presence indicator (0)	1	Indicates the presence of an ID register.

Scan register sizes

Register name	Bit size
Instruction	3
Bypass	1
ID	32
Boundary scan	x36:76

Instruction codes

Instruction	Code	Description
EXTEST	000	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all SRAM outputs to High-Z state. This instruction is not 1149.1-compliant.
IDCODE	001	Loads the ID register with the vendor ID code and places the register between TDI and TDO. This operation does not affect SRAM operations.
SAMPLE Z	010	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all SRAM output drivers to a high-Z state.
RESERVED	101	Do not use. This instruction is reserved for future use.
SAMPLE/ PRELOAD	100	Captures I/O ring contents. Places the boundary scan register between TDI and TDO.
BYPASS	111, 011, 110	Places the bypass register between TDI and TDO. This operation does not affect SRAM operations.

165-ball BGA boundary scan order (x36)

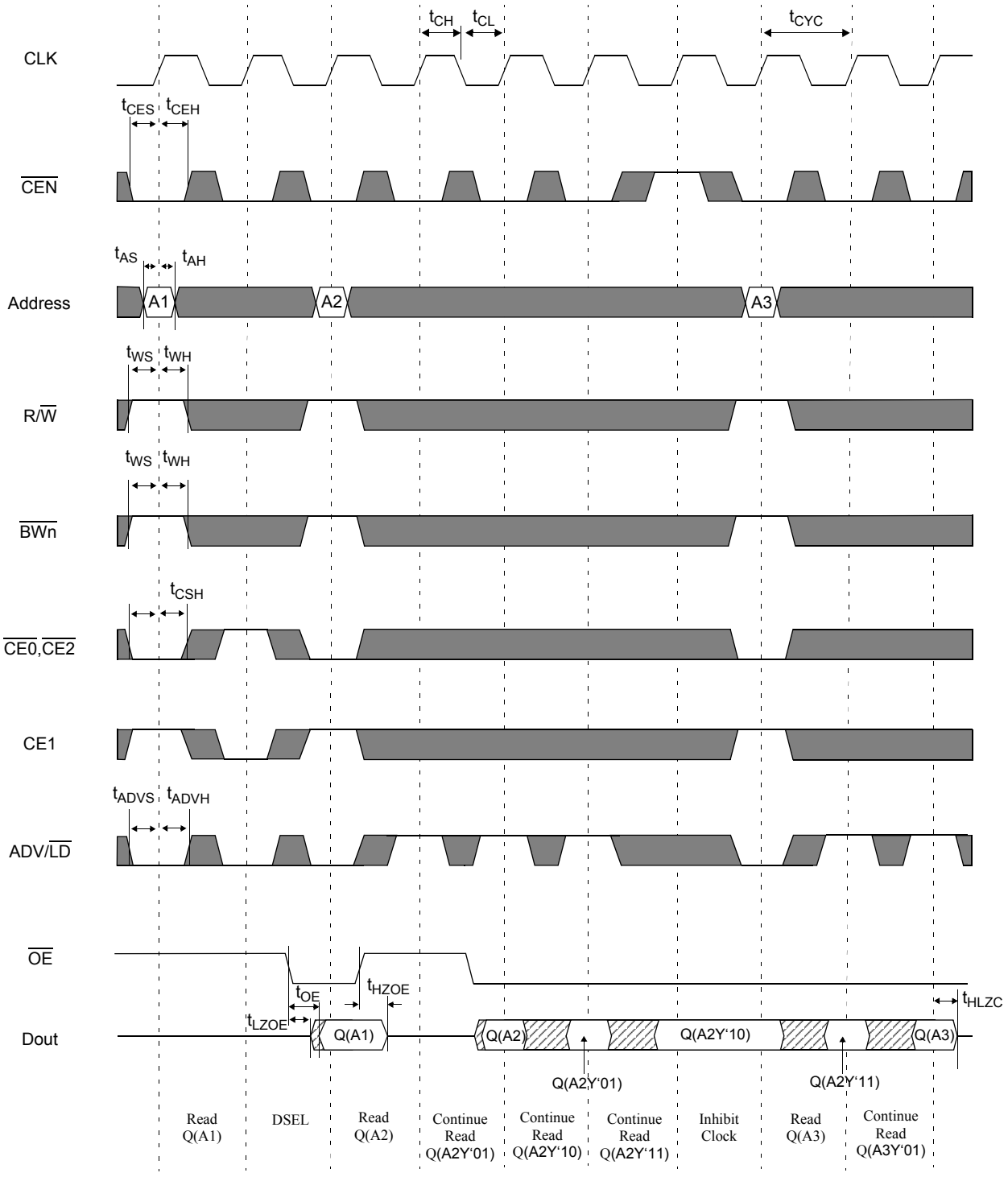
Bit #s	Signal Name	Ball ID
1	NC	6N
2	A	8P
3	A	8R
4	A	9R
5	A	9P
6	A	10P
7	A	10R
8	A	11R
9	NC	11P
10	ZZ	11H
11	DQPa	11N
12	DQa	11M
13	DQa	11L
14	DQa	11K
15	DQa	11J
16	DQa	10M
17	DQa	10L
18	DQa	10K
19	DQa	10J
20	DQb	11G
21	DQb	11F
22	DQb	11E
23	DQb	11D
24	DQb	10G
25	DQb	10F
26	DQb	10E
27	DQb	10D
28	DQPb	11C
29	NC	11A
30	NC	11B
31	A	10A
32	A	10B
33	A	9A
34	A	9B
35	ADV/$\overline{LD}$	8A
36	$\overline{OE}$	8B
37	$\overline{CEN}$	7A
38	R/$\overline{W}$	7B

Bit #s	Signal Name	Ball ID
39	CLK	6B
40	$\overline{CE2}$	6A
41	$\overline{BWa}$	5B
42	$\overline{BWb}$	5A
43	$\overline{BWc}$	4A
44	$\overline{BWd}$	4B
45	CE1	3B
46	$\overline{CE0}$	3A
47	A	2A
48	A	2B
49	NC	1B
50	NC	1A
51	DQPc	1C
52	DQc	1D
53	DQc	1E
54	DQc	1F
55	DQc	1G
56	DQc	2D
57	DQc	2E
58	DQc	2F
59	DQc	2G
60	DQd	1J
61	DQd	1K
62	DQd	1L
63	DQd	1M
64	DQd	2J
65	DQd	2K
66	DQd	2L
67	DQd	2M
68	DQPd	1N
69	A	2R
70	$\overline{LBO}$	1R
71	A	3P
72	A	3R
73	A	4R
74	A	4P
75	A1	6P
76	A0	6R

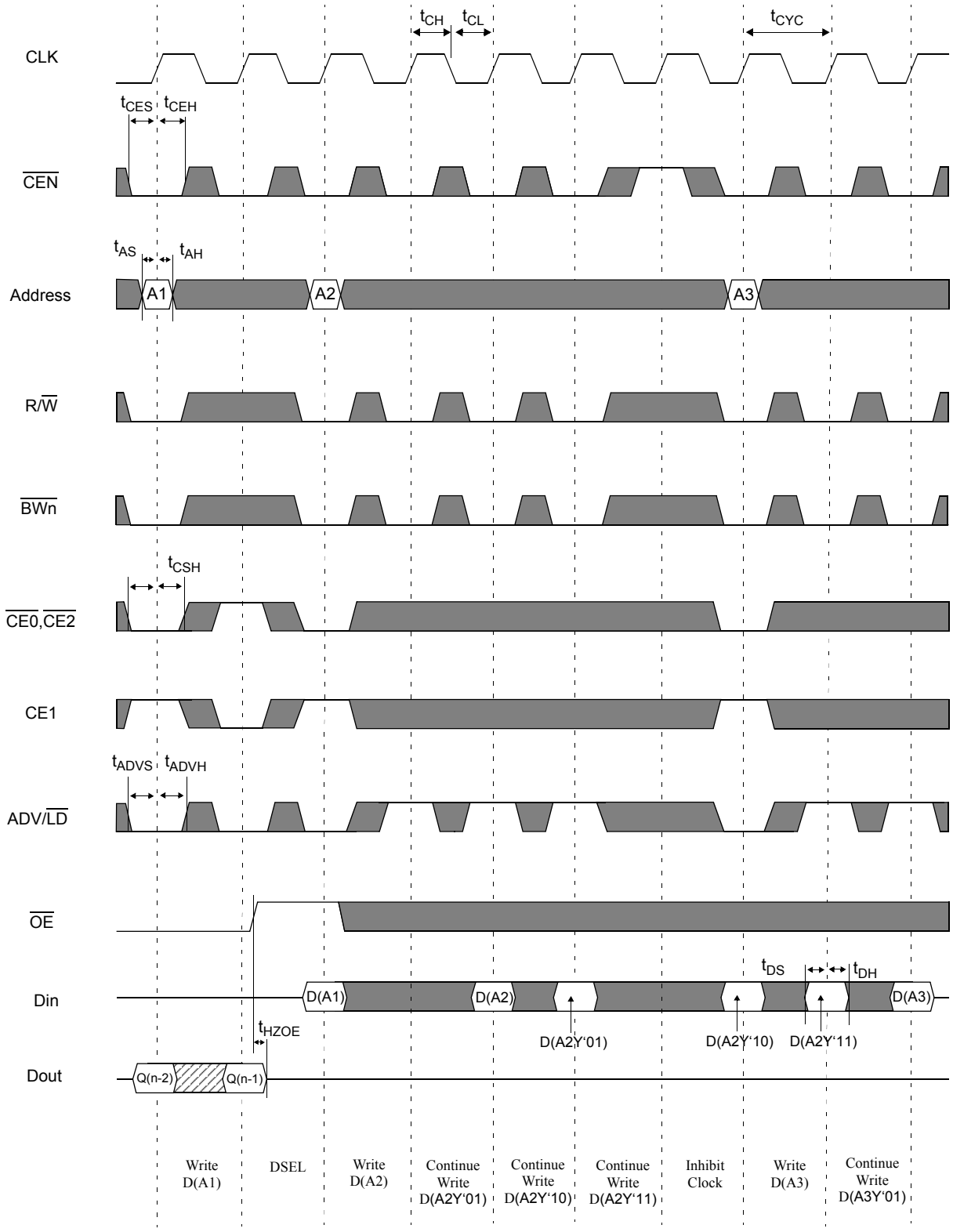
Key to switching waveforms

Rising input Falling input don't care Undefined

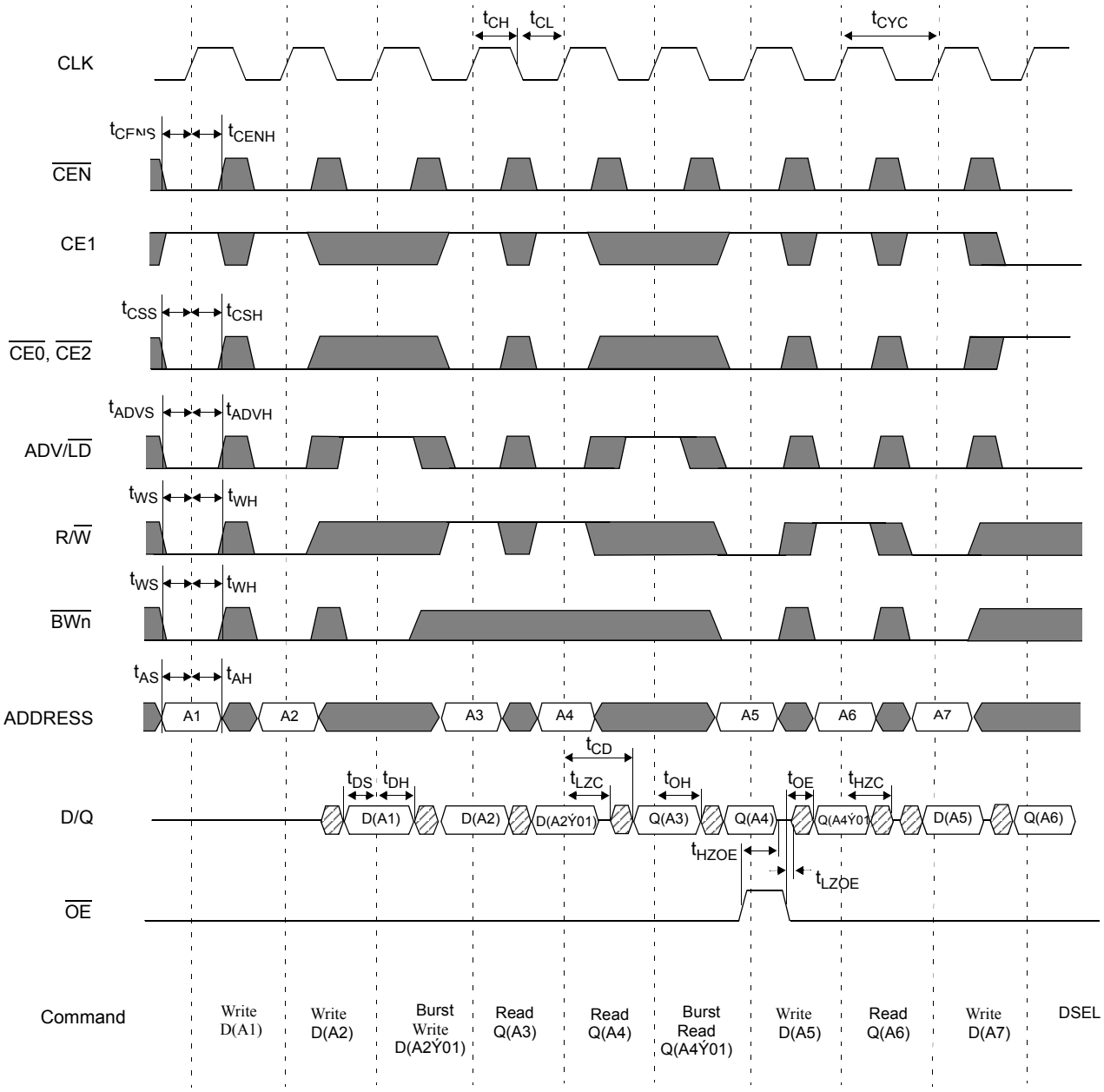
Timing waveform of read cycle



Timing waveform of write cycle

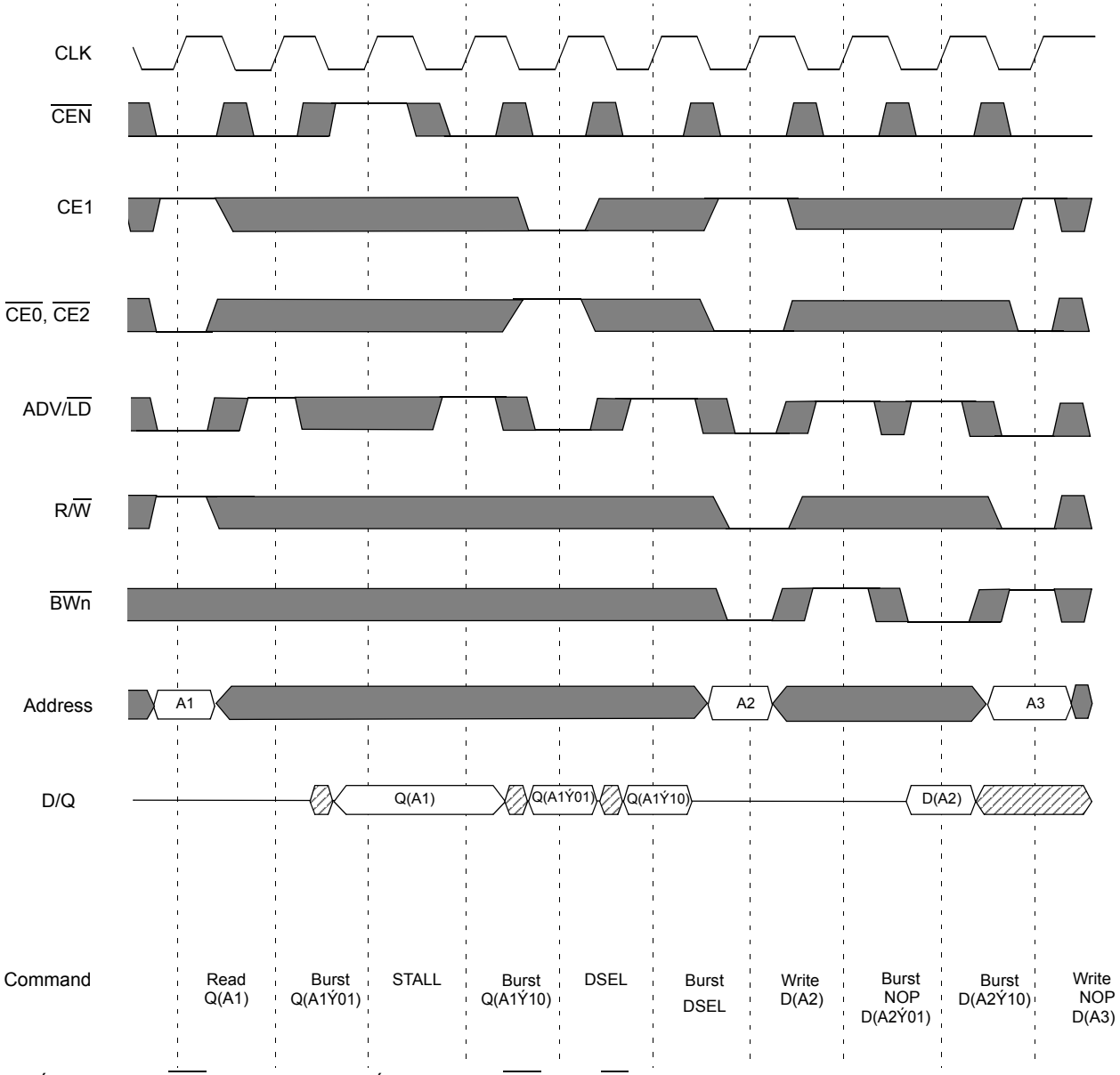


Timing waveform of read/write cycle



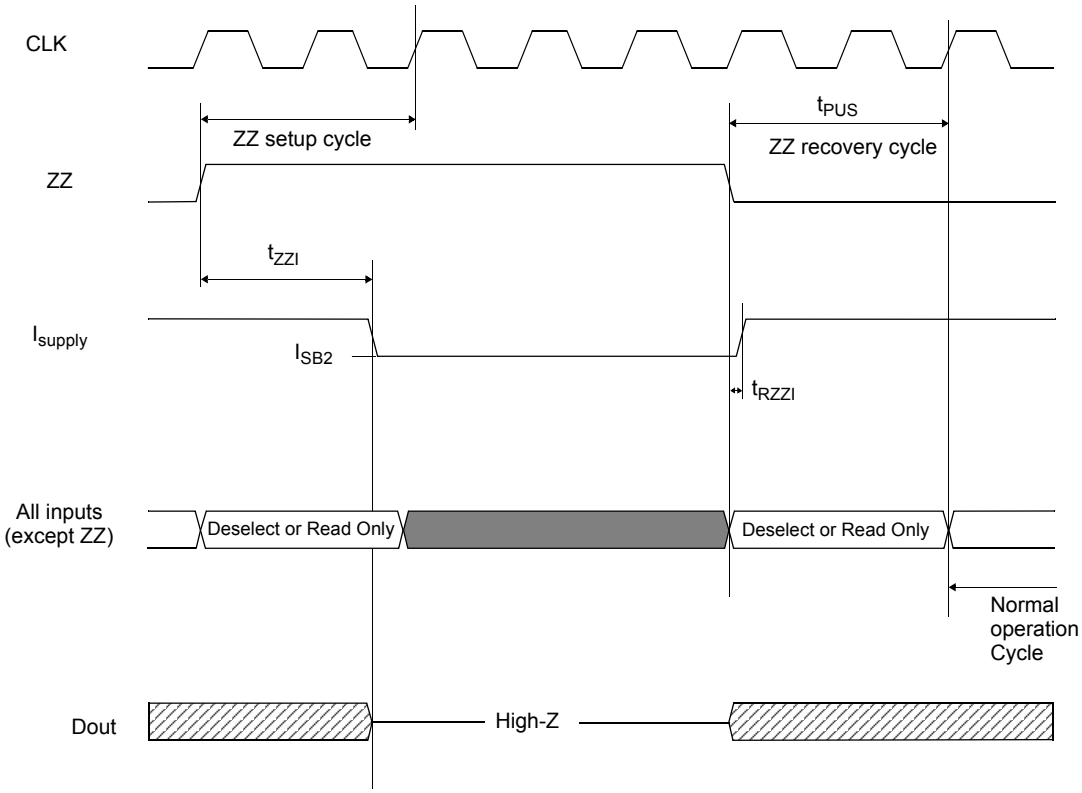
Note: Ý = XOR when $\overline{LBO}$ = high/no connect. Ý = ADD when $\overline{LBO}$ = low. $\overline{BW[a:d]}$ is don't care.

NOP, stall and deselect cycles



Note: Ý = XOR when $\overline{LBO}$ = high/no connect; Ý = ADD when $\overline{LBO}$ = low. $\overline{OE}$ is low.

Timing waveform of snooze mode



AC test conditions

- Output load: For t_{LZC}, t_{LZOE}, t_{HZOE}, and t_{HZC}, see Figure C. For all others, see Figure B.
- Input pulse level: GND to 3V. See Figure A.
- Input rise and fall time (measured at 0.3V and 2.7V): 2 ns. See Figure A.
- Input and output timing reference levels: 1.5V.

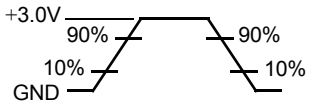


Figure A: Input waveform

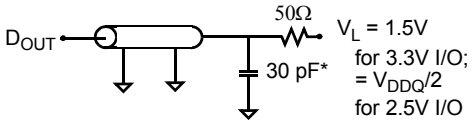


Figure B: Output load (A)

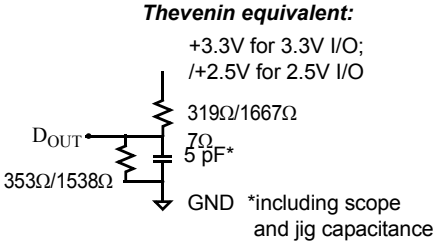


Figure C: Output load(B)

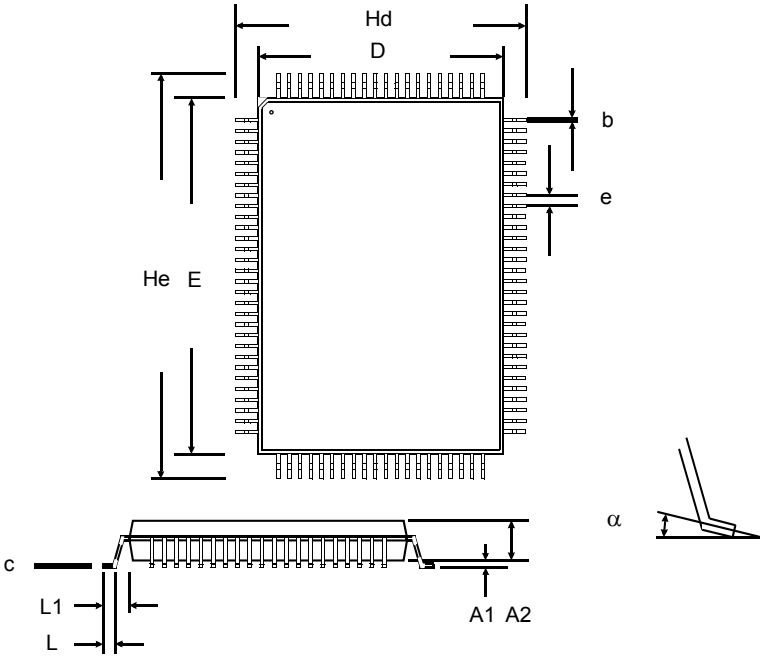
Notes

1) For test conditions, see "AC test conditions", Figures A, B, and C
2) This parameter measured with output load condition in Figure C.
3) This parameter is sampled, but not 100% tested.
4) t_{HZOE} is less than t_{LZOE}, and t_{HZC} is less than t_{LZC} at any given temperature and voltage.
5) t_{CH} is measured high above V_{IH}, and t_{CL} is measured low below V_{IL}
6) This is a synchronous device. All addresses must meet the specified setup and hold times for all rising edges of CLK. All other synchronous inputs must meet the setup and hold times with stable logic levels for all rising edges of CLK when chip is enabled.
7) Write refers to R/$\overline{W}$ and $\overline{BW[a,b,c,d]}$.
8) Chip select refers to $\overline{CE0}$, CE1, and $\overline{CE2}$.

Package dimensions

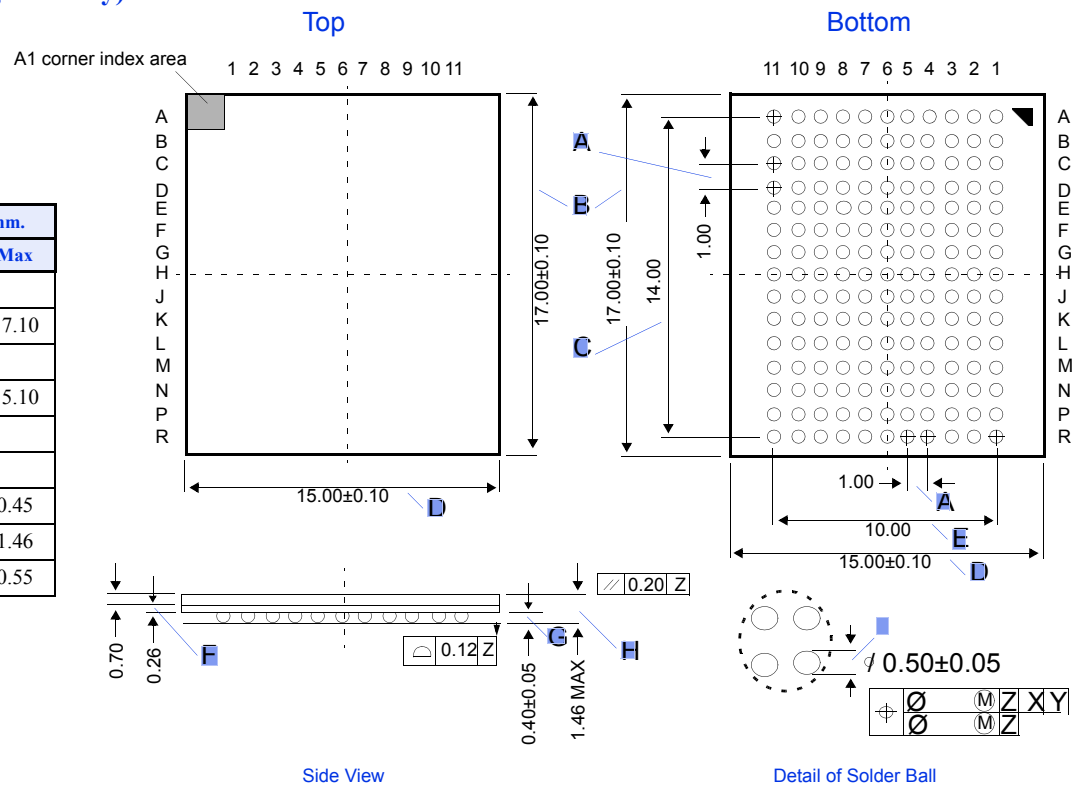
100-pin quad flat pack (TQFP)

	TQFP	
	Min	Max
A1	0.05	0.15
A2	1.35	1.45
b	0.22	0.38
c	0.09	0.20
D	13.90	14.10
E	19.90	20.10
e	0.65 nominal	
Hd	15.90	16.10
He	21.90	22.10
L	0.45	0.75
L1	1.00 nominal	
α	0°	7°
Dimensions in millimeters		



165-ball BGA (ball grid array)

All measurements are in mm.			
	Min	Typ	Max
A		1.00	
B	16.90	17.00	17.10
C		14.00	
D	14.90	15.00	15.10
E		10.00	
F		0.26	
G	0.35	0.40	0.45
H	1.26	1.36	1.46
I	0.45	0.50	0.55



Ordering information

Package & Width	–200 MHz	–166 MHz	–133 MHz
TQFP x32	AS7C331MNTD32A-200TQC	AS7C331MNTD32A-166TQC	AS7C331MNTD32A-133TQC
	AS7C331MNTD32A-200TQI	AS7C331MNTD32A-166TQI	AS7C331MNTD32A-133TQI
TQFP x36	AS7C331MNTD36A-200TQC	AS7C331MNTD36A-166TQC	AS7C331MNTD36A-133TQC
	AS7C331MNTD36A-200TQI	AS7C331MNTD36A-166TQI	AS7C331MNTD36A-133TQI
BGA x32	AS7C331MNTD32A-200BC	AS7C331MNTD32A-166BC	AS7C331MNTD32A-133BC
	AS7C331MNTD32A-200BI	AS7C331MNTD32A-166BI	AS7C331MNTD32A-133BI
BGA x36	AS7C331MNTD36A-200BC	AS7C331MNTD36A-166BC	AS7C331MNTD36A-133BC
	AS7C331MNTD36A-200BI	AS7C331MNTD36A-166BI	AS7C331MNTD36A-133BI

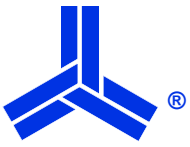
Note:

Add suffix ‘N’ to the above part number for Lead Free Parts (Ex. AS7C331MNTD32A-200TQCN)

Part numbering guide

AS7C	33	1M	NTD	32/36	A	–XXX	TQ or B	C/I	X
1	2	3	4	5	6	7	8	9	10

1. Alliance Semiconductor SRAM prefix
2. Operating voltage: 33 = 3.3V
3. Organization: 1M = 1M
4. NTD™ = No Turn-Around Delay. Pipelined mode
5. Organization: 32 = x 32, 36 = x 36
6. Production version: A = first production version
7. Clock speed (MHz)
8. Package type: TQ = TQFP; B = BGA
9. Operating temperature: C = commercial (0° C to 70° C); I = industrial (-40° C to 85° C)
10. N = Lead Free Part



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www.alsc.com

Part Number: AS7C331MNTD32A / AS7C331MNTD36A

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