MAY - 6 1992

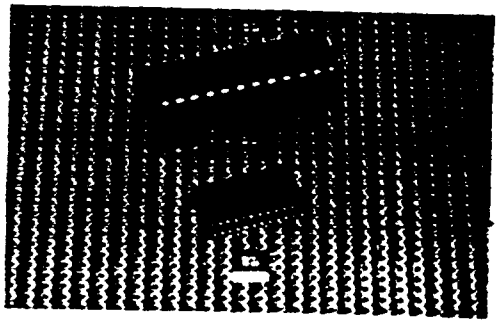
Sipex

SP7800

12-Bit 3µs Sampling A/D Converter

Features

- 333k Samples Per Second
- Standard ±10V and ±5V Input
- DC Performance Over Temp: No Missing Codes
  1/2 LSB Integral Linearity Error
  3/4 LSB Differential Linearity Error
- AC Performance Over Temp:
  72dB Signal-to-Noise Ratio
  80dB Spurious-free Dynamic Range
  -80dB Total Harmonic Distortion
- Internal Sample/Hold, Reference, Clock, and 3-State Outputs
- Power Dissipation: 215mW max
- Package: 24-Pin Single-wide DIP
  24-Lead SOIC



Description

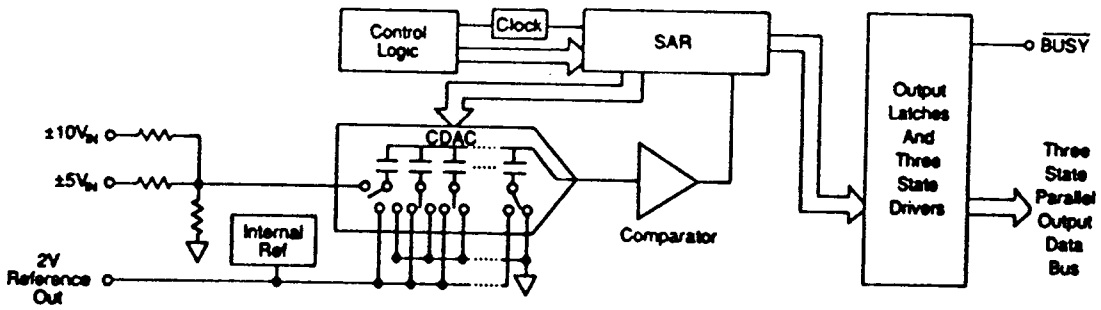
The **SP7800** is a complete 12-bit sampling A/D converter using state-of-the-art CMOS structures. It contains a complete 12-bit successive approximation A/D converter with internal sample/hold, reference, clock, digital interface for microprocessor control, and three-state output drives.

The **SP7800** is specified at a 333kHz sampling rate. Conversion time is factory set for 2.70µs max over temperature, and the high-speed sampling input stage insures a total acquisition and conversion time of 3µs max over temperature. Precision, laser-trimmed scaling resistors provide industry-standard input ranges of ±5V or ±10V.

AD and DC performance are completely specified. Two grades based on linearity and dynamic performance are available to provide the optimum price/performance fit in a wide range of applications.

The 24-pin **SP7800** is available in plastic and side-braze hermetic 0.3" wide DIPs, and in SOIC packages. It operates from a +5V supply and either a -12V or -15V supply. The **SP7800** is available in grades specified over both the 0°C to +70°C commercial and, with full MIL-STD-883 processing over the -55°C to +125°C temperature ranges.

Functional Diagram



Specifications

$T_A = T_{min}$ to T_{max}. Sampling Frequency. f_s = 333kHz. $-V_S$ = -15V. V_S = +5V. unless otherwise specified.

Absolute Maximum Ratings

$-V_S$ to Analog Common ..... -16.5V
VS to Digital Common ..... +7V
Pin 23 (V_{SD}) to Pin 24 (V_{SA}) ..... ±0.3V
Analog Common to Digital Common ..... ±1V
Control Inputs to Digital Common ..... -0.3 to V_S + 0.3 V
Analog Input Voltage ..... ±20V

Maximum Junction Temperature ..... 160°C
Internal Power Dissipation 750mW
Lead Temperature (soldering, 10s) ..... +300°C
Thermal Resistance $Ø_{JA}$
Plastic DIP ..... 50°C/W
SOIC ..... 100°CC/W
Ceramic ..... 50°C/W

PARAMETER	CONDITIONS	SP7800J/S			SP7800K/T			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
RESOLUTION				12			•	Bits
ANALOG INPUT								
Voltage Ranges			±10V/±5V			•		V
Impedance	±10V Range	4.4	6.3	8.1	•	•	•	kΩ
	±5V Range	2.9	4.2	5.4	•	•	•	kΩ
THROUGHPUT SPEED								
Conversion Time	Conversion Alone		2.5	2.7		•	•	µs
Complete Cycle	Acquisition + Conversion		2.8	3.0		•	•	µs
Throughput Rate		333	380		•	•		kHz
DC ACCURACY								
Full Scale Error[1]				±0.50			±0.35	%
Integral Linearity Error				±1			±1/2	LSB[2]
Differential Linearity Error				±1			±3.4	LSB
No Missing Codes		Guaranteed			Guaranteed			
Bipolar Zero[1]				±4			±2	LSB
Power Supply Sensitivity	-16.5V<V_S<-13.5V			±1/2			•	LSB
	-12.6V<V_S<-11.4V			±1/2			•	LSB
	+4.75V<V_S<+5.25V			±1			±1/2	LSB
Transition Noise[3]			0.1			•		LSB
AC ACCURACY								
Spurious-Free Dynamic Range	f_{IN} = 47kHz	74	77		77	80		dB[4]
Total Harmonic Distortion	f_{IN} = 47kHz		-77	-74		-80	-77	dB
Two-tone Intermodulation Distortion	f_{IN1} = 24.4kHz (-6dB) f_{IN2} = 28.5kHz (-6dB)		-77	-74		-80	-77	dB
Signal to (Noise + Distortion) Ratio	f_{IN} = 47kHz	67	70		69	72		dB
Signal to Noise Ratio (SNR)	f_{IN} = 47kHz	68	71		70	73		dB
SAMPLING DYNAMICS								
Aperture Delay			13			•		ns
Aperture Jitter			150			•		ps. rms
Transient Response[5]			130			•		ns
Overvoltage Recovery[6]			150			•		ns
INTERNAL REFERENCE VOLTAGE								
Voltage		1.9	2.0	2.1	•	•	•	V
Source Current Available 10 µA for External Loads			10			•		µA
DIGITAL INPUTS								
Logic Levels								
V_{IL}		-0.3		+0.8	•		•	V
V_{IH}		+2.4		+5.3	•		•	V
I_{IL}		-5			•			µA
I_{IH}		+5			•			µA

Specifications *(continued)*

PARAMETER	CONDITIONS	SP7800J/S			SP7800K/T			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
RESOLUTION				12			•	Bits
DIGITAL OUTPUTS								
Data Format				Parallel, 12-bit or 8-bit/4-bit				
Data Coding				Binary Offset Binary				
V_{OL}	I_{SINK} = 1.6mA	0.0		+0.4	•		•	V
V_{OH}	I_{SOURCE} = 500µA	+2.4		+5.0	•		•	V
$I_{LEAKAGE}$ (High-Z State)			±0.1	±5		•	•	µA
POWER SUPPLIES								
Rated Voltage								
$-V_S$		-11.4	-15	-16.5	•	•	•	V
V_S (V_{SA} and V_{SD})		+4.75	+5.0	+5.25	•	•	•	V
Current								
$-I_S$			3.5	6		•	•	mA
I_S			18	25		•	•	mA
Power Consumption			135	215		•	•	mW
TEMPERATURE RANGE								
Specification J,K		0		+70	•		•	°C
S,T		-55		+125	•		•	°C
Storage		-65		+150	•		•	°C

NOTES

1. Adjustable to zero with external potentiometer.
2. LSB means Least Significant Bit. For SP7800, 1LSB = 2.44mV for ±5V range. 1 LSB = 4.88mV for ±10V range.
3. Noise was characterized over temperature near full scale, 0V, and negative full scale. 0.1LSB represents a typical rms level of noise at the worst case, which was near full scale input at +125°C.
4. All specifications in dB are referred to a full-scale input, either ±10V or ±5V.
5. For full-scale step input, 12-bit accuracy attained in specified time.
6. Recovers to specified performance in specified time after 2 x F_S input overvoltage.

Pin Assignments

PIN	# NAME	DESCRIPTION
1	AN1	±10V Analog Input. Connected to GND for ±5V range.
2	AN2	±5V Analog Input. Connected to GND for ±10V range.
3	REF	+2V Reference Output. Bypass to GND with 22µF to 47µF Tantalum. Buffer for external loads.
4	AGND	Analog Ground. Connect to pin 13.
5	D11	Data Bit 11. Most Significant Bit (MSB).
6	D10	Data Bit 10.
7	D9	Data Bit 9.
8	D8	Data Bit 8.
9	D7	Data Bit 7 if HBE is LOW; LOW if HBE is HIGH.
10	D6	Data Bit 6 if HBE is LOW; LOW if HBE is HIGH.
11	D5	Data Bit 5 if HBE is LOW; LOW if HBE is HIGH.
12	D4	Data Bit 4 if HBE is LOW; LOW if HBE is HIGH.
13	DGND	Digital Ground. Connect to pin 4.
14	D3	Data Bit 3 if HBE is LOW; Data Bit 11 if HBE is HIGH.
15	D2	Data Bit 2 if HBE is LOW; Data Bit 10 if HBE is HIGH.
16	D1	Data Bit 1 if HBE is LOW; Data Bit 9 if HBE is HIGH.
17	D0	Data Bit 0 if HBE is LOW. Least Significant Bit (LSB). Data Bit 8 if HBE is HIGH.
18	HBE	High Byte Enable. When held LOW, data output as 12-bits in parallel. When held HIGH, four MSBs presented on pins 14–17, pins 9–12 output LOWs. Must be LOW to initiate conversion.
19	R/$\overline{C}$	Read/$\overline{\text{Convert}}$. Falling edge initiates conversion when $\overline{CS}$ is LOW, HBE is LOW, and BUSY is HIGH.
20	$\overline{CS}$	Chip Select. Outputs in Hi-Z state when HIGH. Must be LOW to initiate conversion or read data.
21	$\overline{BUSY}$	Busy. Output LOW during conversion. Data valid on rising edge in Convert Mode.
22	$-V_S$	Negative Power Supply. -12V or -15V. Bypass to GND.
23	V_{SD}	Positive Digital Power Supply. +5V. Connect to pin 24, and bypass to GND.
24	V_{SA}	Positive Analog Power Supply. +5V. Connect to pin 23, and bypass to GND.

Operation

Basic Operation

Figure 1 shows the simple hookup circuit required to operate the **SP7800** in a ±10V range in the Convert Mode. A convert command arriving on pin 19, R/$\overline{C}$, (a pulse taking pin 19 LOW for a minimum of 40ns) puts the **SP7800** in the hold mode, and a conversion is started. Pin 21, $\overline{BUSY}$, will be held LOW during the conversion, and rises only after the conversion is completed and the data has been transferred to the output latches. Thus, the rising edge of the signal on pin 21 can be used to read the data from the conversion. Also, during conversion, the $\overline{BUSY}$ signal puts the output data lines in Hi-Z states and inhibits input lines. This means that pulses on pin 19 are ignored, so that new conversions cannot be initiated during a conversion, either as a result of spurious signals or to short-cycle the **SP7800.**

In the Read Mode, the input to pin 19 is kept normally LOW, and a HIGH pulse is used to read data and initiate a conversion. In this mode, the rising edge of R/$\overline{C}$ on pin 19 will enable the output data pins, and the data from the previous conversion becomes valid. The falling edge then puts the **SP7800** in a hold mode, and initiates a new conversion.

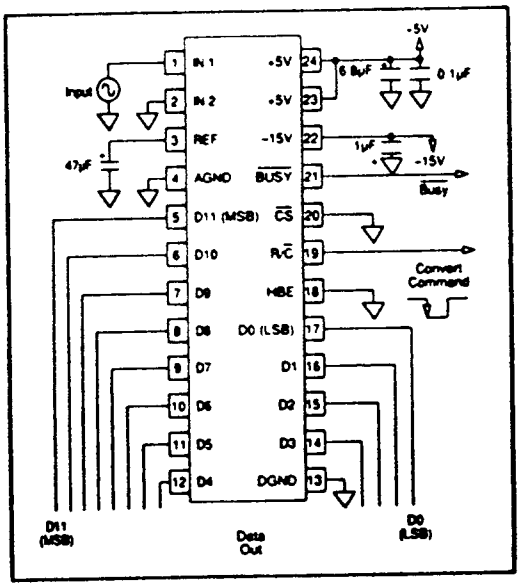


Figure 1. Basic ±10V Operation

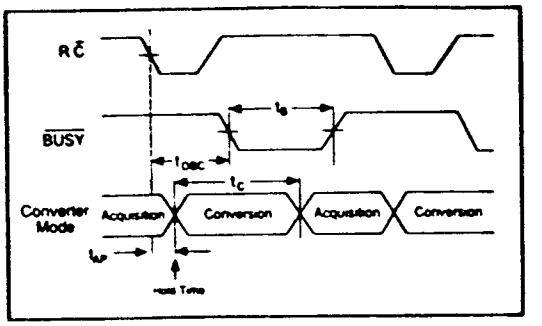


Figure 2. Acquisition and Conversion Timing

The **SP7800** will begin acquiring a new sample as soon as the conversion is completed, even before the $\overline{BUSY}$ output rises on pin 21, and will track the input signal until the next conversion is started, whether in the Convert Mode or the Read Mode.

For use with an 8-bit bus, the data can be read out in two bytes under the control of pin 18, HBE. With a LOW input on pin 18, at the end of a conversion, the 8 LSBs of data are loaded into the latches on pins 9 through 12 and 14 through 17. Taking pin 18 HIGH then loads the 4 MSBs on pins 14 through 17, with pins 9 through 12 being forced LOW.

Analog Input Ranges

The **SP7800** offers two standard bipolar input ranges: ±10V and ±5V. If a ±10V range is required, the analog input signal should be connected to pin 1. A signal requiring a ±5V range should be connected to pin 2. In either case, the other pin of the two must be grounded or connected to the adjustment circuits described in the section on calibration. (See Figure 3 or 4).

Controlling The SP7800

The **SP7800** can be easily interfaced to most microprocessor-based and other digital systems. The microprocessor may take full control of each conversion, or the **SP7800** may operate in a stand-alone mode, controlled only by the R/$\overline{C}$ input. Full control consists of initiating the conversion and reading the output data at user command, transmitting data either all 12-bits in one parallel word, or in two 8-bit bytes. The three control inputs ($\overline{CS}$, R/$\overline{C}$ and HBE) are all TTL/CMOS compatible. The functions of the control lines are shown in Table 1.

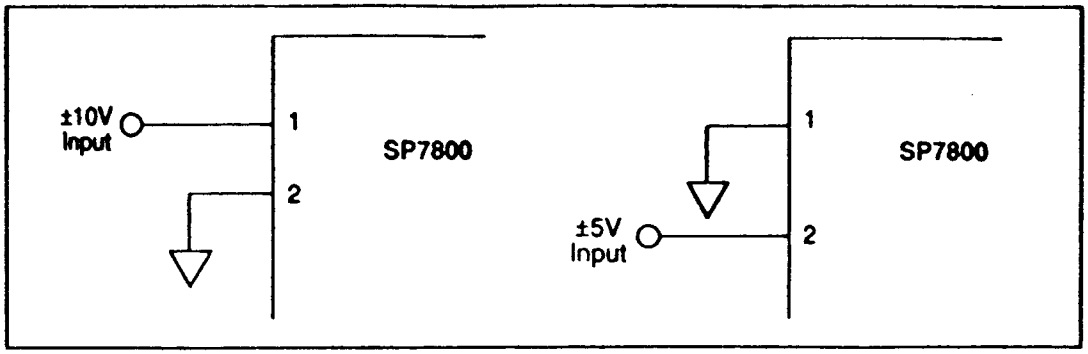


Figure 3. a) ±10V Range Without Trims; b) ±5V Range Without Trims

For stand-alone operation, control of the **SP7800** is accomplished by a single control line connected to R/$\overline{C}$. In this mode, $\overline{CS}$ and HBE are connected to GND. The output data are presented as 12-bit words. The stand-alone mode is used in systems containing dedicated input ports which do not require full bus interface capability.

Conversion is initiated by a HIGH-to-LOW transition on R/$\overline{C}$. The three-state data output buffers are enabled when R/$\overline{C}$ is HIGH and $\overline{BUSY}$ is HIGH. Thus, there are two possible modes of operation: conversion can be initiated with either positive or negative pulses. In either case, the R/$\overline{C}$ pulse must remain LOW a minimum of 40ns.

Figure 4 illustrates timing when conversion is initiated by an R/$\overline{C}$ pulse which goes LOW and returns HIGH during the conversion. In this case (Convert Mode), the three-state outputs go into the Hi-Z state in response to the falling edge of R/$\overline{C}$, and are enabled for external access of the data after completion of the conversion.

Figure 5 illustrates the timing when conversion is initiated by a positive R/$\overline{C}$ pulse. In this mode (Read Mode), the output data from the previous conversion is enabled during the HIGH portion of R/$\overline{C}$. A new conversion starts on the falling edge of R/$\overline{C}$, and the three-state outputs return to the Hi-Z state until the next occurrence of a HIGH on R/$\overline{C}$.

$\overline{CS}$	R/$\overline{C}$	HBE	$\overline{BUSY}$	OPERATION
1	X	X	1	None - outputs in Hi-Z state.
0	1→0	0	1	Holds signal and initiates conversion.
0	1	0	1	Output three-state buffers enabled once conversion has finished.
0	1	1	1	Enable hi-byte in 8-bit bus mode.
0	1→0	1	1	Inhibit start of conversion.
0	0	1	1	None - outputs in Hi-Z state.
X	X	X	0	Conversion in progress. Outputs Hi-Z state. New conversion inhibited until present conversion has finished.

Table 1. Control Line Functions

Conversion Start

A conversion is initiated on the **SP7800** only by a negative transition occurring on R/$\overline{C}$, as shown in Table 2. No other combination of states or transitions will initiate a conversion. Conversion is inhibited if either $\overline{CS}$ or HBE are HIGH, or if $\overline{BUSY}$ is LOW. $\overline{CS}$ and HBE should be stable a minimum of 25ns prior to the transition on R/$\overline{C}$. Timing relationships for start of conversion are illustrated in Figure 7.

The BUSY output indicates the current state of the converter by being LOW only during conversion. During this time the three-state output buffers remain in a Hi-Z state, and therefore data cannot be read during conversion. During this period, additional transitions on the three digital inputs ($\overline{CS}$, R/$\overline{C}$ and HBE) will be ignored, so that conversion cannot be prematurely terminated or restarted.

Internal Clock

The **SP7800** has an internal clock that is factory trimmed to achieve a typical conversion time of 2.47µs, and a maximum

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{DBC}	BUSY delay from R/$\overline{C}$		80	150	ns
t_B	$\overline{BUSY}$ Low		2.5	2.7	µs
t_{AP}	Aperture Delay		13		ns
Δt_{AP}	Aperture Jitter		150		ps, rms
t_C	Conversion Time		2.47	2.70	µs

Table 2. Acquisition and Conversion Timing

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_W	R/$\overline{C}$ Pulse Width	40	10		ns
t_{DBC}	$\overline{BUSY}$ delay from R/$\overline{C}$		80	150	ns
t_B	$\overline{BUSY}$ LOW		2.5	2.7	µs
t_{AP}	Aperture Delay		13		ns
Δt_{AP}	Aperture Jitter		150		ps, rms
t_C	Conversion Time		2.47	2.70	µs
t_{DBE}	$\overline{BUSY}$ from End of Conversion		100		ns
t_{DS}	$\overline{BUSY}$ Delay after Data Valid	25	75	200	ns
t_A	Acquisition Time		130	300	ns
$t_A + t_C$	Throughput Time		2.6	3.0	µs
t_{HDR}	Valid Data Held After R/$\overline{C}$ LOW	20	50		ns
t_S	$\overline{CS}$ or HBE LOW before R/$\overline{C}$ Falls	25	5		ns
t_H	$\overline{CS}$ or HBE LOW after R/$\overline{C}$ Falls	25	0		ns
t_{DD}	Data Valid from $\overline{CS}$ LOW, R/$\overline{C}$ HIGH, and HBE in Desired State (Load = 100pF)		65	150	ns
t_{HDR}	Valid Data Held After R/$\overline{C}$ Low	20	50		ns
t_{HL}	Delay to Hi-Z State after R/$\overline{C}$ Falls or $\overline{CS}$ Rises (3kΩ Pullup or Pulldown		50	150	ns

Table 3: Timing Relationships

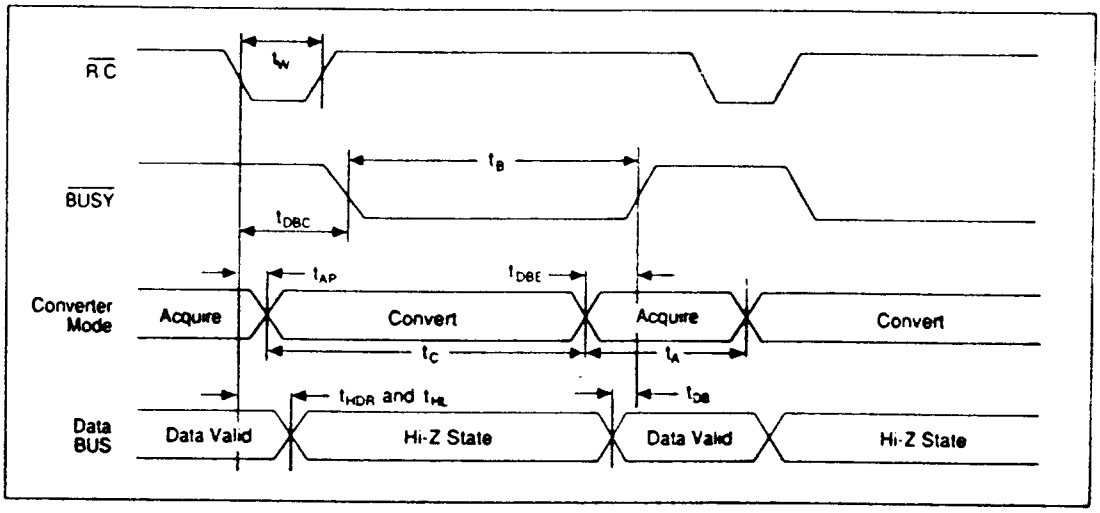


Figure 4: Convert Mode: R/C Pulse LOW – Outputs Enabled After Conversion

conversion time over the full operating temperature range of 2.7µs. No external adjustments are required, and with the guaranteed maximum acquisition time of 300ns, throughput performance is assured with convert pulses as close as 3µs.

Reading Data

After conversion is initiated, the output buffers remain in a Hi-Z state until the following three logic conditions are simultaneously met: R/$\overline{C}$ is HIGH, $\overline{BUSY}$ is HIGH and $\overline{CS}$ is LOW. Upon satisfaction of these conditions, the data lines are enabled according to the state of HBE. See Figure 8 and Table 3 for timing relationships and specifications.

Calibration

Optional External Gain And Offset Trim

Offset and full-scale errors may be trimmed to zero using external offset and full-scale trim potentiometers connected to the **SP7800** as shown in Figure 8.

If adjustment of offset and full scale is not required, connections as shown in Figure 3 should be used.

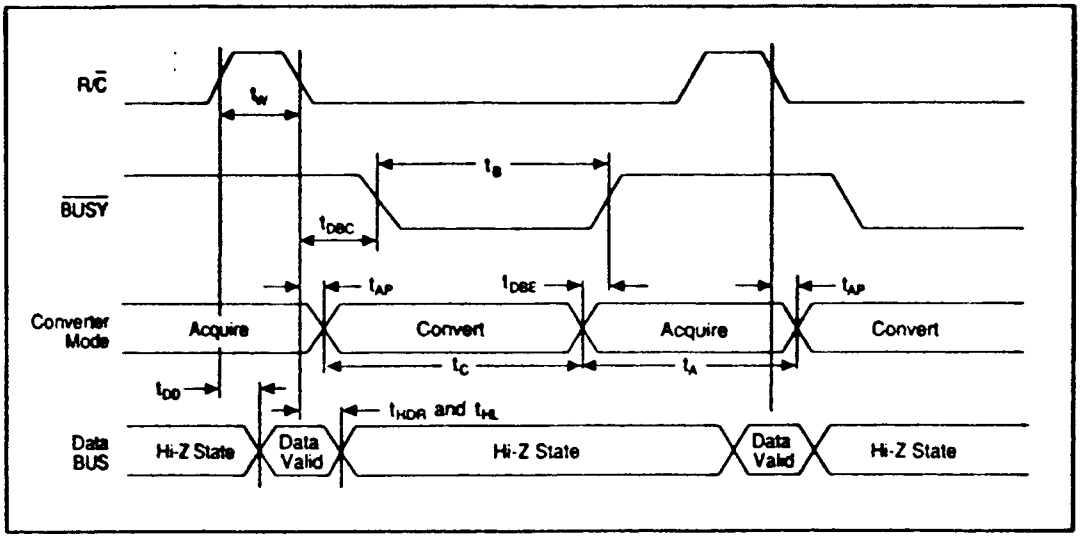


Figure 5. Read Mode: R/C Pulse HIGH – Outputs Enabled Only When R/C is High

Calibration Procedure

First, trim offset, by applying at the input (pin 1 or 2) the mid-point transition voltage (-2.44mV for the ±10V range, -1.22mV for the ±5V range). With the SP7800 converting continually, adjust potentiometer R_1 until the MSB (D11 on pin 5) is toggling alternately HIGH and LOW.

Next adjust full scale, by applying at the input a DC input signal that is 3/2LSB below the nominal full scale voltage (+9.9927V for the ±10V range, +4.9963 for the ±5V range). With the SP7800 converting continually, adjust R2 until the LSB (D0 on pin 17) is toggling HIGH and LOW with all of the other bits HIGH.

Layout Considerations

Because of the high resolution and linearity of the SP7800, system design problems such as ground path resistance and contact resistance become very important.

Analog Signal Source Impedance

The input resistance of the SP7800 is 6.3kΩ or 4.2kΩ (for the ±10V and ±5V ranges respectively). To avoid introducing distortion, the source resistance must be very low, or constant with signal level. The output impedance provided by most op amps is ideal.

Pins 23 (V_{SD}) and 24 (V_{SA}) are not connected internally on the SP7800, to maximize accuracy on the chip. They should be connected together as close as possible to the unit. Pin 24 may be slightly more sensitive than pin 23 to supply variations, but to maintain maximum system accuracy, both should be well isolated from digital supplies with wide load variations.

To limit the effects of digital switching elsewhere in a system on the analog performance of the system, it often makes sense to run a separate +5V supply conductor from the supply regulator to any analog components requiring +5V, including the SP7800.

The V_S pins (23 and 24) should be connected together and bypassed with a

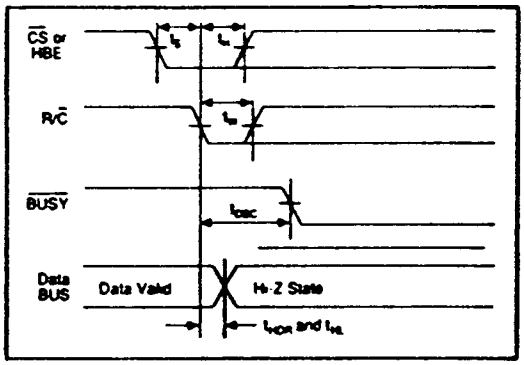


Figure 6. Conversion Start Timing

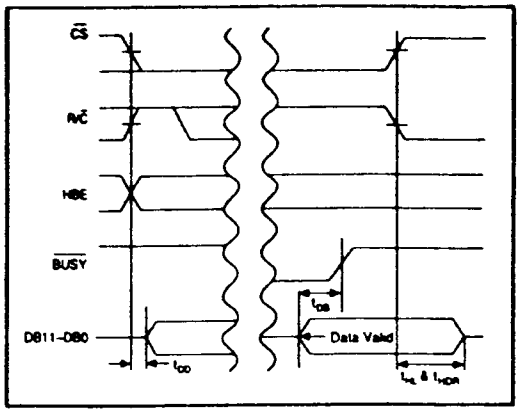


Figure 7. Read Cycle Timing

parallel combination of a 6.8µF Tantalum capacitor and a 0.1µF ceramic capacitor located close to the converter to obtain noise-free operation. (See Figure 1). The $-V_S$ pin 22 should be bypassed with a 1µF tantalum capacitor, again as close as possible to the **SP7800.**

Noise on the power supply lines can degrade converter performance, especially noise and spikes from a switching power supply. Appropriate supplies or filters must be used.

The GND pins (4 and 13) are also separated internally, and should be directly connected to a ground plane under the converter if at all possible. A ground plane is usually the best solution for preserving dynamic performance and reducing noise coupling into sensitive converter circuits. Where any compromises must be made, the common return of the analog input signal should be referenced to pin 4, AGND, on the **SP7800,** which prevents any voltage drops that might occur in the power supply common returns from appearing in series with the input signal.

Coupling between analog input and digital lines should be minimized by careful layout. For instance, if the lines must cross, they should do so at right angles. Parallel analog and digital lines should be separated from each other by a pattern connected to common.

If external full scale and offset potentiometers are used, the potentiometers and related resistors should be located as close to the **SP7800** as possible.

Reference Bypass

Pin 3 (REF) should be bypassed with a 22µF to 47µF tantalum capacitor. A rated working voltage of 2V or more is acceptable here. This pin is used to enhance the system accuracy of the internal reference circuit, and is not recommended for driving external signals. If there are important system reasons for using the **SP7800** reference externally, the output of pin 3 must be appropriately buffered.

"Hot Socket" Precaution

Two separate +5V V_S pins, 23 and 24, are used to minimize noise caused by digital transients. If one pin is powered and the other is not, the **SP7800** may "Latch Up" and draw excessive current. In normal operation, this is not a problem because both pins will be soldered together. However, during evaluation, incoming inspection, repair, etc., where the potential of a "Hot Socket" exists, care should be taken to power the **SP7800** only after it has been socketed.

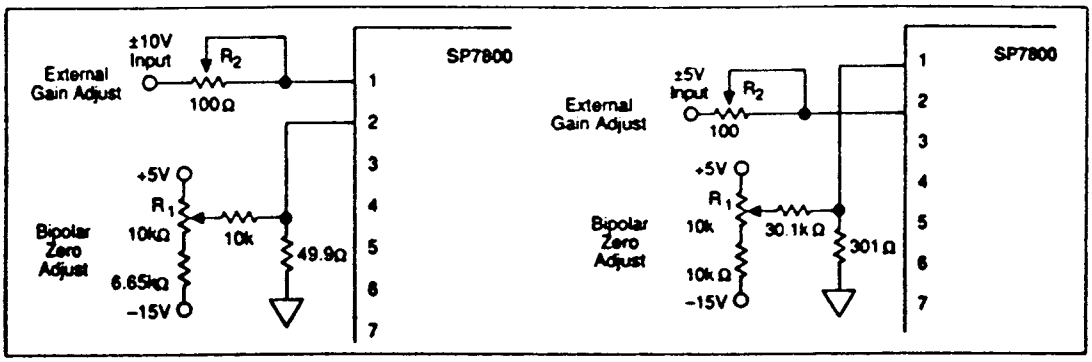


Figure 8. a) ±10V Range With External Trims; b) ±5V Range With External Trims

INPUT VOLTAGE RANGE AND LSB VALUES			
Input Voltage Range Defined As:		±10V	±5V
Analog Input Connected to Pin		1	2
Pin Connected to GND		2	1
One Least Significant Bit (LSB)	$FSR/2^{12}$	$20V/2^{12}$ 4.88mV	$10V/2^{12}$ 2.44mV
OUTPUT TRANSITION VALUES			
FFEH TO FFFH	+ FULL SCALE	+10V-3/2LSB +9.9927V	+5V-3/2LSB +4.9963V
7FFH TO 800H	Mid Scale (Bipolar Zero)	0V-1/2LSB -2.44mV	0V-1/2LSB -1.22mV
000H to 001H	-Full Scale	-10V+1/2LSB -9.9976V	-5V+1/2LSB -4.9988V

Table 4. Input Voltages, Transition Values, and LSB Values

Minimizing "Glitches"

Coupling of external transients into an analog-to-digital converter can cause errors which are difficult to debug. In addition to the discussions earlier on layout considerations for supplies, bypassing and grounding, there are several other useful steps that can be taken to get the best analog performance out of a system using the **SP7800**. These potential system problem sources are particularly important to consider when developing a new system, and looking for the causes of errors in breadboards.

First, care should be taken to avoid glitches during critical times in the sampling and conversion process. Since the **SP7800** has an internal sample/hold function, the signal that puts it into the hold state (R/$\overline{C}$ going LOW) is critical, as it would be on any sample/hold amplifier. The R/$\overline{C}$ falling edge should be sharp and have minimal ringing, especially during the 20ns after it falls.

Although not normally required, it is also good practice to avoid glitching the **SP7800** while bit decisions are being made. Since the above discussion calls for a fast, clean rise and fall on R/$\overline{C}$, it makes sense to keep the rising edge of the convert pulse outside the time when bit decisions are being made. In other words, the convert pulse should either be short (under 100ns so that it transitions before the MSB decision), or relatively long (over 2.75µs to transition after the LSB decision).

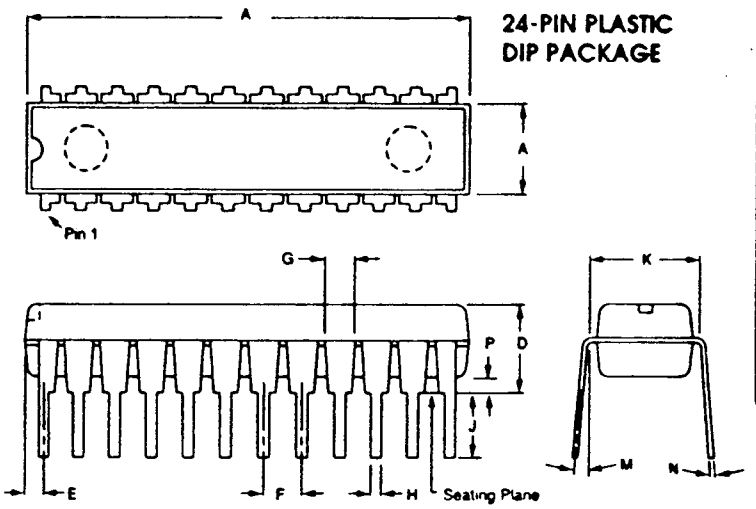
Next, although the data outputs are forced into a Hi-Z state during conversion, fast bus transients can still be capacitively coupled into the **SP7800**. If the data bus experiences fast transients during conversion, these transients can be attenuated by adding a logic buffer to the data outputs. The $\overline{BUSY}$ output can be used to enable the buffer.

Naturally, transients on the analog input signal are to be avoided, especially at times within ±20ns of R/$\overline{C}$ going LOW, when they may be trapped as part of the charge on the capacitor array. This requires careful layout of the circuit in front of the **SP7800.**

Finally, in multiplexed systems, the timing on when the multiplexer is switched may affect the analog performance of the system. In most applications, the multiplexer can be switched as soon as R/$\overline{C}$ goes LOW (with appropriate delays), but this may affect the conversion if the switched signal shows glitches or significant ringing at the **SP7800** input. Whenever possible, it is safer to wait until the conversion is completed before switching and multiplexer. The extremely fast acquisition time and conversion time of the **SP7800** make this practical in many applications.

Mechanical Dimensions

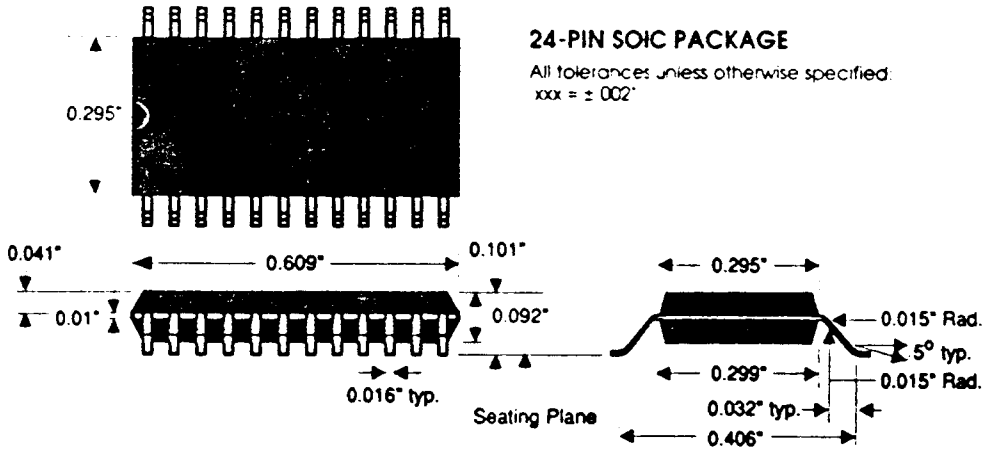
24-PIN PLASTIC DIP PACKAGE



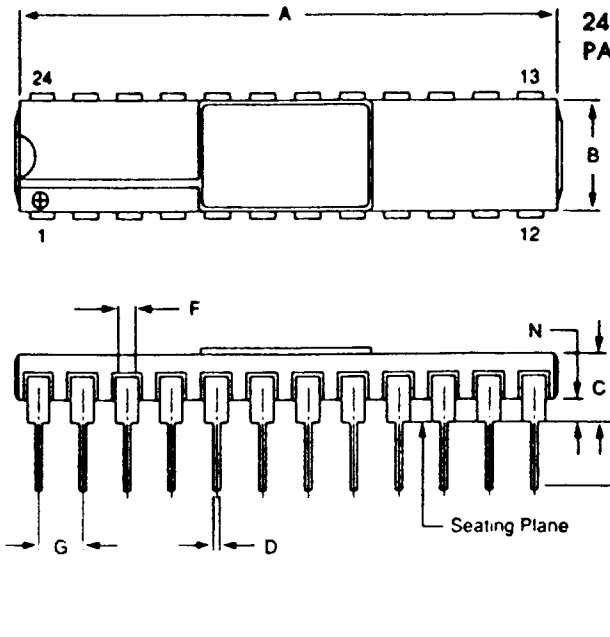
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.125	1.255	28.58	31.88
B	.250	.290	6.35	7.37
D	.150	.170	3.81	4.32
E	.010	.080	.25	2.03
F	.100 BASIC		2.54 BASIC	
G	.050	.070	1.27	1.78
H	.016	.020	0.41	0.51
J	.125		3.18	
K	.300 BASIC		7.63 BASIC	
M	0°	15°	0°	15°
N	.008	.015	0.20	0.38
P	.010	.030	.25	.76

24-PIN SOIC PACKAGE

All tolerances unless otherwise specified:
xxx = ± 002"



Mechanical Dimensions



24-PIN SIDE-BRAZED CERAMIC PACKAGE

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.188	1.212	30.18	30.78
B	.300	.320	7.62	8.13
C	–	.160	–	4.06
D	.016	.020	0.41	0.51
F	.050 TYP		1.27 TYP	
G	.095	.105	2.41	2.67
J	.009	.012	0.23	0.31
K	.170 BASIC		4.32 BASIC	
L	.290	.310	7.37	7.87
N	.040	.060	1.02	1.52

Ordering Information

0 C to +70°C

±1 LSB INL, Plastic DIP **SP7800JP**
±1/2 LSB INL, Plastic DIP **SP7800KP**
±1 LSB INL, Plastic SOIC **SP7800JU**
±1/2 LSB INL, Plastic SOIC **SP7800KU**

-55°C to +125°C, MILSTD-883 processed

±1 LSB INL, Side-brazed Ceramic DIP **SP7800SQ/883**
±1/2 LSB INL, Side-brazed Ceramic DIP . **SP7800TQ/883**

CAUTION: ESD (Electro-Static Discharge) sensitive device. Permanent damage may occur when unconnected devices are subjected to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. Protective foam should be discharged to the destination socket before devices are removed. Devices should be handled at static safe workstations only. Unused digital inputs must be grounded or tied to the logic supply voltage. Unless otherwise noted, the supply voltage at any digital input should never exceed the supply voltage by more than 0.5 volts or go below -0.5 volts. If this condition cannot be maintained, limit input current on digital inputs by using series resistors or contact Sipex for technical assistance.

Specifications subject to change without notice

Sipex

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