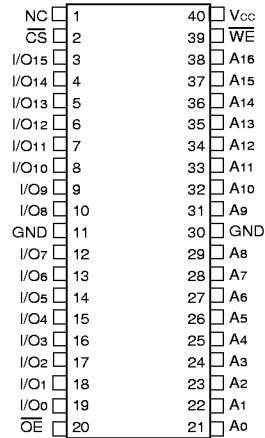




128Kx16 CMOS EEPROM

FIG. 1

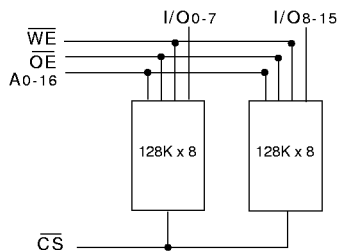
PIN CONFIGURATION



PIN DESCRIPTION

A ₀₋₁₆	Address Inputs
I/O ₀₋₁₅	Data Input/Output
\overline{CS}	Chip Select
\overline{OE}	Output Enable
\overline{WE}	Write Enable
V _{CC}	+5.0V Power
GND	Ground

BLOCK DIAGRAM



128Kx16 BIT CMOS EEPROM MODULE FEATURES

- Read Access Times of 150, 200, 250, 300ns
- 40 Pin, Hermetic Ceramic DIP (Package 303)
- Commercial, Industrial and Military Temperature Ranges
- MIL-STD-883 Compliant Devices Available
- Write Endurance 10,000 Cycles
- Data Retention at 25°C, 10 Years
- Low Power CMOS Operation
- Automatic Page Write Operation
- Page Write Cycle Time 10ms Max.
- Data Polling for End of Write Detection
- Hardware and Software Data Protection
- TTL Compatible Inputs and Outputs
- 256Kx16 Organization Also Available In The Same Package



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol		Unit
Operating Temperature	T _A	-55 to +125	°C
Storage Temperature	T _{STG}	-65 to +150	°C
Signal Voltage Any Pin	V _G	-0.6 to +6.25	V
Voltage on OE and A9		-0.6 to +13.5	V
Thermal Resistance junction to case	θ _{Jc}	28	°C/W
Lead Temperature (soldering -10 secs)		+300	°C

NOTE:

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V _{CC}	4.5	5.5	V
Input High Voltage	V _{IH}	2.0	V _{CC} + 0.3	V
Input Low Voltage	V _{IL}	-0.3	+0.8	V
Operating Temp. (Mil.)	T _A	-55	+125	°C
Operating Temp. (Ind.)	T _A	-40	+85	°C

TRUTH TABLE

CS	OE	WE	Mode	Data I/O
H	X	X	Standby	High Z
L	L	H	Read	Data Out
L	H	L	Write	Data In
X	H	X	Out Disable	High Z/Data Out
X	X	H	Write	
X	L	X	Inhibit	

CAPACITANCE

(T_A = +25°C)

Parameter	Symbol	Condition	Max	Unit
Input Capacitance	C _{IN}	V _{IN} = 0V, f = 1MHz	50	pF
Output Capacitance	C _{OUT}	V _{I/O} = 0V, f = 1MHz	40	pF

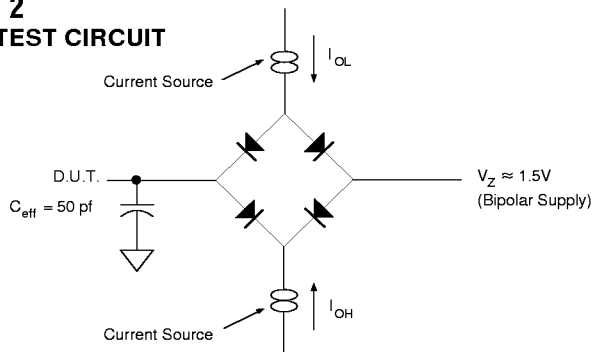
This parameter is guaranteed by design but not tested.

DC CHARACTERISTICS

(V_{CC} = 5.0V, GND = 0V, T_A = -55°C to +125°C)

Parameter	Symbol	Conditions	128K x 16			Unit
			Min	Typ	Max	
Input Leakage Current	I _{LI}	V _{CC} = 5.5, V _{IN} = GND to V _{CC}			10	µA
Output Leakage Current	I _{LO}	CS = V _{IH} , OE = V _{IH} , V _{OUT} = GND to V _{CC}			10	µA
Dynamic Supply Current	I _{CC}	CS = V _{IL} , OE = V _{IH} , f = 5MHz, V _{CC} = 5.5			125	mA
Standby Current	I _{SB}	CS = V _{IH} , OE = V _{IH} , f = 5MHz, V _{CC} = 5.5			1.2	mA
Output Low Voltage	V _{OL}	I _{OL} = 2.1mA, V _{CC} = 4.5V			0.45	V
Output High Voltage	V _{OH}	I _{OH} = -400µA, V _{CC} = 4.5V	2.4			V

FIG. 2 AC TEST CIRCUIT



AC TEST CONDITIONS

Parameter	Typ	Unit
Input Pulse Levels	V _{IL} = 0, V _{IH} = 3.0	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

NOTES:

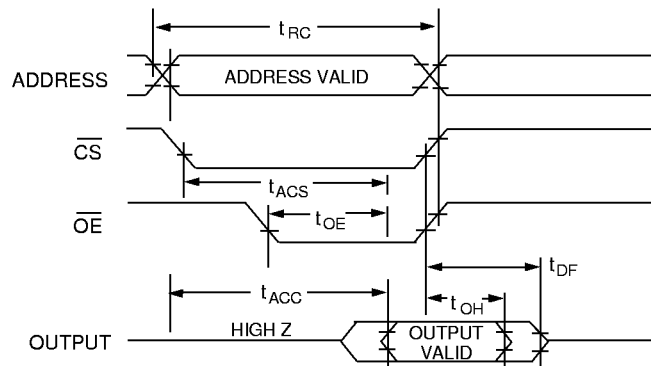
V_Z is programmable from -2V to +7V.
I_{OL} & I_{OH} programmable from 0 to 16mA.
Tester Impedance Z₀ = 75 Ω.
V_Z is typically the midpoint of V_{OH} and V_{OL}.
I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.



READ

Figure 3 shows read cycle waveforms. A read cycle begins with selection address, chip select and output enable. Chip select is accomplished by placing the CS line low. Output enable is done by placing the OE line low. The memory places the selected data byte on I/O0 through D7 after the access time. The output of the memory is placed in a high impedance state shortly after either the OE line or CS line is returned to a high level.

**FIG. 3
READ WAVEFORMS**



NOTE:
OE may be delayed up to tACS-
tOE after the falling edge of CS
without impact on tOE or by tACC-
tOE after an address change
without impact on tACC.

AC READ CHARACTERISTICS (SEE FIGURE 3)

(VCC = 5.0V, GND = 0V, TA = -55°C to +125°C)

Parameter	Symbol	-150		-200		-250		-300		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t _{RC}	150		200		250		300		ns
Address Access Time	t _{ACC}		150		200		250		300	ns
Chip Select Access Time	t _{ACS}		150		200		250		300	ns
Output Hold from Address Change, OE or CS	t _{OH}	0		0		0		0		ns
Output Enable to Output Valid	t _{OE}		85		85		100		125	ns
Chip Select or Output Enable to High Z Output	t _{DF}		70		70		70		70	ns



WRITE

Write operations are initiated when both CS and WE are low and OE is high. The EEPROM devices support both a CS and WE controlled write cycle. The address is latched by the falling edge of either CS or WE, whichever occurs last.

The data is latched internally by the rising edge of either CS or WE, whichever occurs first. A byte write operation will automatically continue to completion.

WRITE CYCLE TIMING

Figures 4 and 5 show the write cycle timing relationships. A write cycle begins with address application, write enable and chip select. Chip select is accomplished by placing the CS line low. Write enable consists of setting the WE line low. The write cycle begins when the last of either CS or WE goes low.

The WE line transition from high to low also initiates an internal 150µsec delay timer to permit page mode operation. Each subsequent WE transition from high to low that occurs before the completion of the 150µsec time out will restart the timer from zero. The operation of the timer is the same as a retriggerable one-shot.

AC WRITE CHARACTERISTICS
(VCC = 5V, GND = 0V, TA = -55°C to +125°C)

Table with 5 columns: Parameter, Symbol, 128K x 16 (Min/Max), and Unit. Rows include Write Cycle Time, Address Set-up Time, Write Pulse Width, Chip Select Set-up Time, Address Hold Time, Data Hold Time, Chip Select Hold Time, Data Set-up Time, Output Enable Set-up Time, Output Enable Hold Time, and Write Pulse Width High.



FIG. 4
WRITE WAVEFORMS
WE CONTROLLED

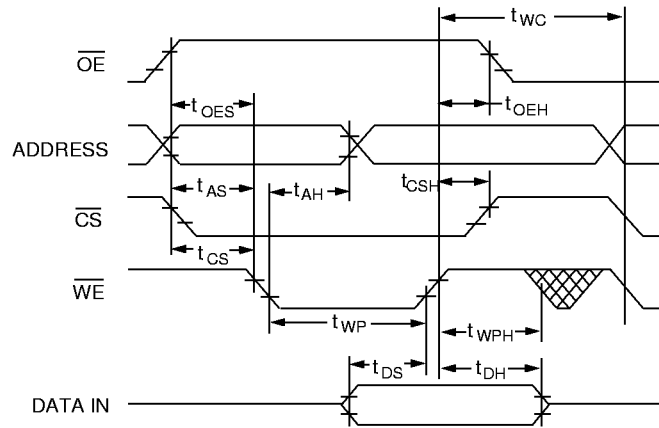
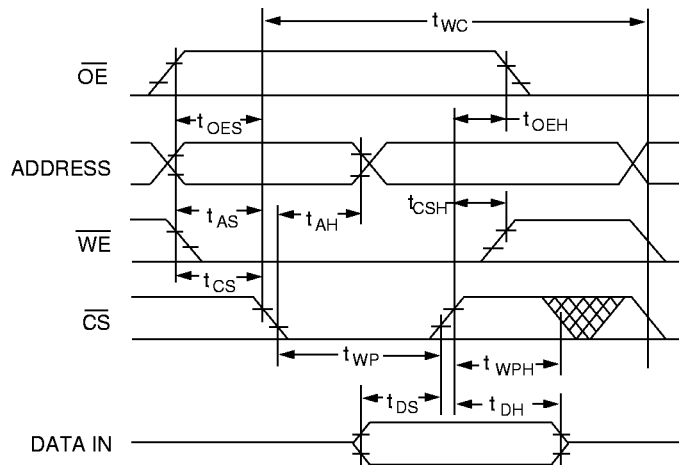


FIG. 5
WRITE WAVEFORMS
CS CONTROLLED





DATA POLLING

Operation with data polling permits a faster method of writing to the EEPROM. The actual time to complete the memory programming cycle is faster than the guaranteed maximum.

The EEPROM features a method to determine when the internal programming cycle is completed. After a write cycle is initiated, the EEPROM will respond to read cycles to provide the microprocessor with the status of the programming cycle. The status consists of the last data byte written being returned with data bit I/O7 and I/O15 complemented during the programming cycle, then I/O7 and I/O15 true after completion.

Data polling allows a simple bit test operation to determine the status of the EEPROM. During the internal programming cycle, a read of the last word written will produce the complement of the data on I/O7 and I/O15. For example, if the data written consisted of I/O7 and I/O15 = HIGH, then the data read back would consist of I/O7 and I/O15 = LOW.

A polled word write sequence would consist of the following steps:

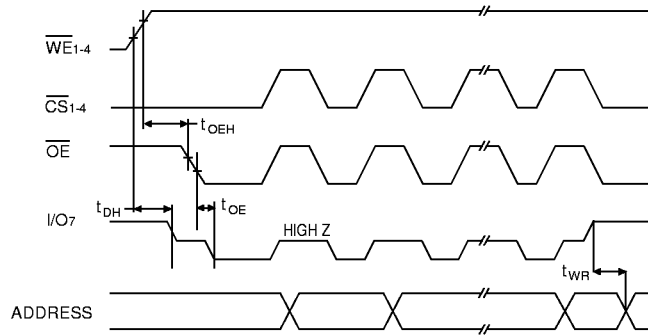
1. write word to EEPROM
2. store last word and last address written
3. release a time slice to other tasks
4. read word from EEPROM - last address
5. compare I/O7 and I/O15 to stored value
 - a) If different, write cycle is not completed, go to step 3.
 - b) If same, write cycle is completed, go to step 1 or step 3.

DATA POLLING AC CHARACTERISTICS

(Vcc = 5V, GND = 0V, TA = -55°C to +125°C)

Parameter	Symbol	Min	Max	Unit
Data Hold Time	t _{DH}	10		ns
Output Enable Hold Time	t _{OEH}	10		ns
Output Enable To Output Delay	t _{OE}		100	ns
Write Recovery Time	t _{WR}	0		ns

**FIG. 6
DATA POLLING
WAVEFORMS**





PAGE WRITE OPERATION

These devices have a page write operation that allows one to 128 words to be written into the device and then simultaneously written during the internal programming period. Successive words may be loaded in the same manner after the first data word has been loaded. An internal timer begins a time out operation at each write cycle. If another write cycle is completed within 150µs or less, a new time out period begins. Each write cycle restarts the delay period. The write cycles can be continued as long as the interval is less than the time out period.

The usual procedure is to increment the least significant address lines from A0 through A6 at each write cycle. In this manner a page of up to 128 words can be loaded into the EEPROM in a burst mode before beginning the relatively long interval programming cycle.

After the 150µs time out is completed, the EEPROM begins an internal write cycle. During this cycle the entire page of words will be written at the same time. The internal programming cycle is the same regardless of the number of words accessed.

The page address must be the same for each word load and must be valid during each high to low transition of WE (or CS). The block address also must be the same for each word load and must remain valid throughout the WE (or CS) low pulse. The page and block address lines are summarized below:

PAGE MODE CHARACTERISTICS

(Vcc = 5.0V, GND = 0V, TA = -55°C to +125°C)

Parameter	Symbol	Min	Max	Unit
Write Cycle Time, TYP = 6ms	t _{WC}		10	ms
Data Set-up Time	t _{DS}	100		ns
Data Hold Time	t _{DH}	10		ns
Write Pulse Width	t _{WP}	150		ns
Word Load Cycle Time	t _{BLC}		150	µs
Write Pulse Width High	t _{WPH}	50		ns

**FIG. 7
PAGE WRITE WAVEFORMS**

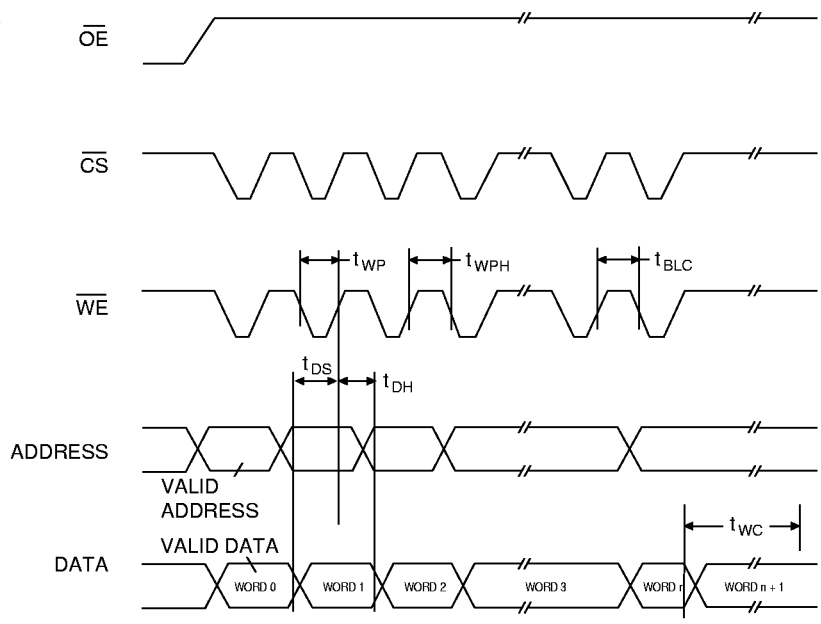
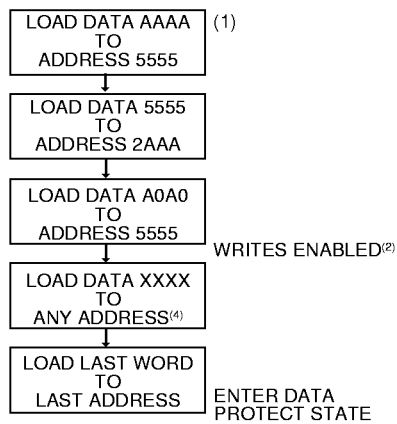




FIG. 8
SOFTWARE BLOCK DATA
PROTECTION ENABLE ALGORITHM

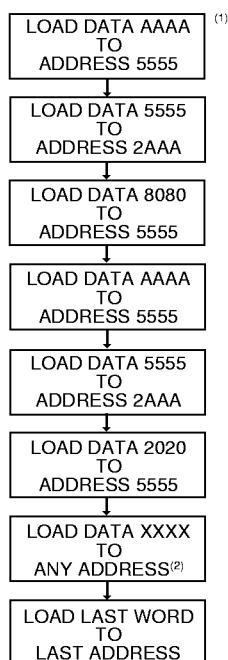


NOTES:

1. Data Format: I/O₁₅ - I/O₀ (Hex);
Address Format: A₁₆ - A₀ (Hex).
2. Write Protect state will be activated at end of write even if no other data is loaded.
3. Write Protect state will be deactivated at end of write period even if no other data is loaded.
4. 1 to 128 words of data may be loaded in the 128Kx16.



FIG. 9
SOFTWARE BLOCK DATA
PROTECTION DISABLE ALGORITHM



NOTES:

1. Data Format: I/O₁₅ - I/O₀ (Hex);
Address Format: A₁₅ - A₀ (Hex).
2. 1 to 128 words of data may be loaded in the 128Kx16.

SOFTWARE DATA PROTECTION

A software write protection feature may be enabled or disabled by the user. When shipped by White Microelectronics, the devices have the feature disabled. Write access to the device is unrestricted.

To enable software write protection, the user writes three access code words to three special internal locations. Once write protection has been enabled, each write to the EEPROM must use the same three byte write sequence to permit writing. After setting software data protection, any attempt to write to the device without the three-byte command sequence will start the internal write timers. No data will be written to the device, however, for the duration of twc. The write protection feature can be disabled by a six byte write sequence of specific data to specific locations. Power transitions will not reset the software write protection.

The software write protection guards against inadvertent writes during power transitions or unauthorized modification using a PROM programmer.

HARDWARE DATA PROTECTION

Several methods of hardware data protection have been implemented in the White Microelectronics EEPROM. These are included to improve reliability during normal operations.

a) Vcc power on delay

As Vcc climbs past 3.8V typical the device will wait 5msec typical before allowing write cycles.

b) Vcc sense

While below 3.8V typical write cycles are inhibited.

c) Write inhibiting

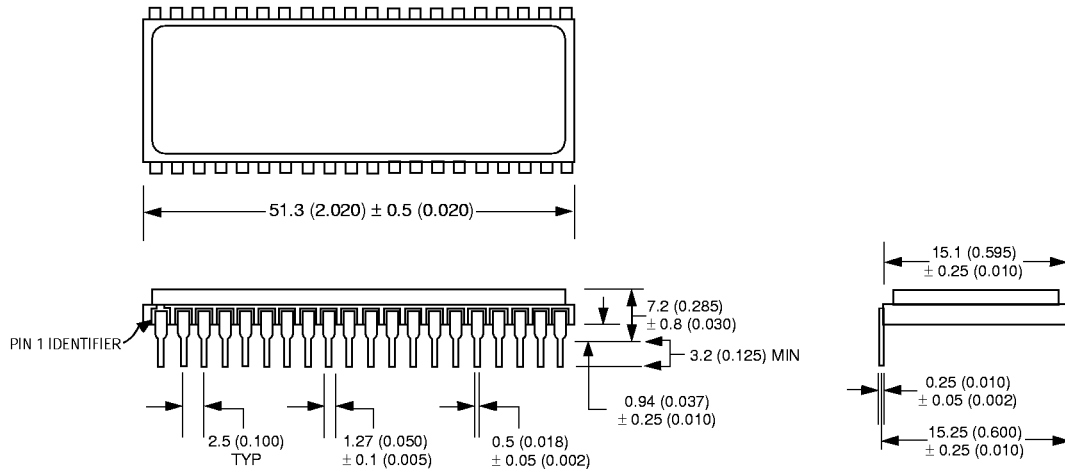
Holding \overline{OE} low and either \overline{CS} or \overline{WE} high inhibits write cycles.

d) Noise filter

Pulses of <8ns (typ) on \overline{WE} or \overline{CS} will not initiate a write cycle.



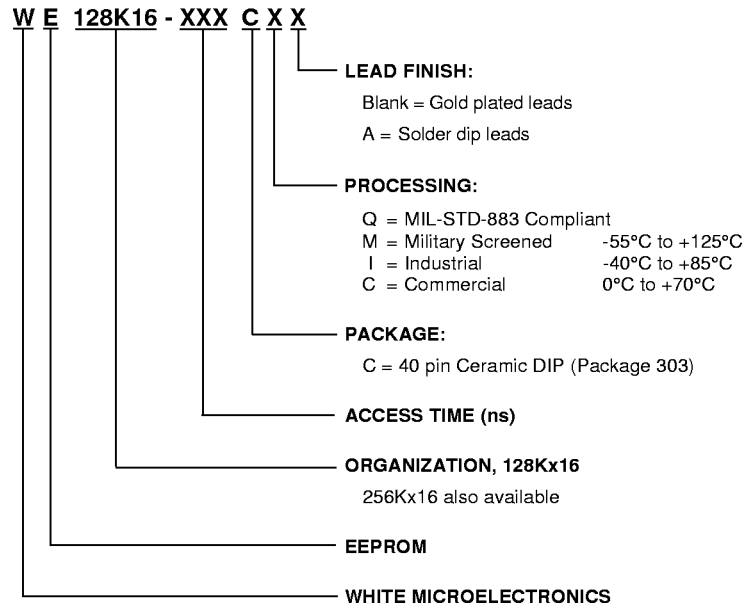
PACKAGE 303: 40 PIN, CERAMIC DIP, SINGLE CAVITY SIDE BRAZED



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES



ORDERING INFORMATION



DEVICE TYPE	SPEED	PACKAGE	SMD NO.
128K x 16 EEPROM Module	300ns	40 pin DIP (C)	5962-96689 01HXX*
128K x 16 EEPROM Module	250ns	40 pin DIP (C)	5962-96689 02HXX*
128K x 16 EEPROM Module	200ns	40 pin DIP (C)	5962-96689 03HXX*
128K x 16 EEPROM Module	150ns	40 pin DIP (C)	5962-96689 04HXX*