Integrated Device Technology, Inc.

64K x 32 Fusion Memory™ SYNCHRONOUS CACHE RAM

ADVANCE INFORMATION
IDT71F632

FEATURES:

- Uses IDT's Fusion Memory™ technology
- 66 and 75 MHz speed grades
- 3-1-1-1 Pipelined Burst Read
- 3-1-1-1 Pipelined Burst Write
- 3-1-1-1-1-1-1-1... extended pipelined operation
- Refresh overhead consumes less than 0.5% of cycles
- Pinout is superset of industry standard PBSRAM
- Interchangeable with PBSRAM in new designs
- Low operating and standby power consumption 1/3 the power of standard PBSRAM
- Packaged in a JEDEC Standard 100-pin rectangular plastic thin quad flatpack (TQFP)

DESCRIPTION:

The IDT71F632 CacheRAM™ is a high-performance, low-power replacement for standard 64K x 32 pipelined burst SRAM (PBSRAM) in cache applications. The 71F632 is built using IDT's Fusion Memory technology, which combine the performance of SRAM with the cost structure of DRAM. It is fundamentally compatible with standard PBSRAM, with additional features to accommodate the internal DRAM operation of the memory. These additional features are defined so that 71F632 compatible system controllers and properly implemented PC boards can work transparently with either the 71F632 or PBSRAM in cache memory applications.

Four pins, identified as No Connect (NC) on the standard PBSRAM specifications, are used to support 71F632 operation. These pins are host bus W/R#, RESET# and two proprietary functions labeled F0 and F1. When using standard PBSRAM, these pins have no effect and the associated functions in the 71F632-compatible chipset are not activated.

The 71F632 supports PBSRAM operating modes, including burst read (3-1-1-1), burst write (3-1-1-1) and pipelined burst read or write (3-1-1-1-1-1...). As with all DRAM devices, refresh is required. The memory is not accessible during the refresh interval. System performance reduction due to refresh is negligible at less than 0.5%.

ABOUT IDT'S Fusion Memory TECHNOLOGY:

What is Fusion Memory?

- Fusion Memory is a new kind of memory technology that combines the high performance and ease-of-use of SRAM with the manufacturing costs of DRAM.

What are the advantages of Fusion Memory?

- Fusion memory products use about 1/3 as much power as SRAMs and they can be built on dice that are about 1/3 the size. The smaller die size not only makes them cheaper, but also means that higher levels of integration are possible than with SRAM.

Why are Fusion Memory chips so much smaller than SRAM?

- Traditional SRAM uses four or six transistors to make each memory cell. Fusion Memory uses only one transistor for each memory cell, so the memory array itself is only about 1/4 the size of an SRAM.

Is Fusion Memory the same as Dynamic Memory?

- Not exactly. While both Fusion Memory and DRAMs use single-transistor dynamic cells for storage, Fusion Memories use much different designs for all the surrounding circuitry, such as address drivers, sense amps, and control circuitry. This gives Fusion Memory a performance level that is much higher than DRAM.

If Fusion Memory uses dynamic storage, are there refresh cycles?

- Yes, but the refresh control is handled automatically and nearly invisibly, using either on-chip circuitry or circuitry in the chip set used with the memory device. The performance penalty is typically less than 0.5%.

How does the performance of Fusion Memory cache RAMs compare with synchronous burst SRAMS?

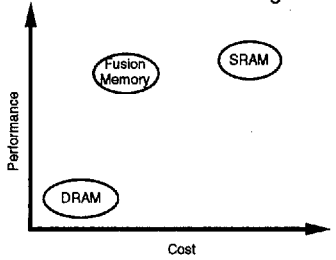
- The Fusion Memory devices equal the performance of the SRAMs they are designed to replace.

Are Fusion Memory and PBSRAMs interchangeable?

- A system designed to use the Fusion Memory cache RAMs can use standard PBSRAMs instead.

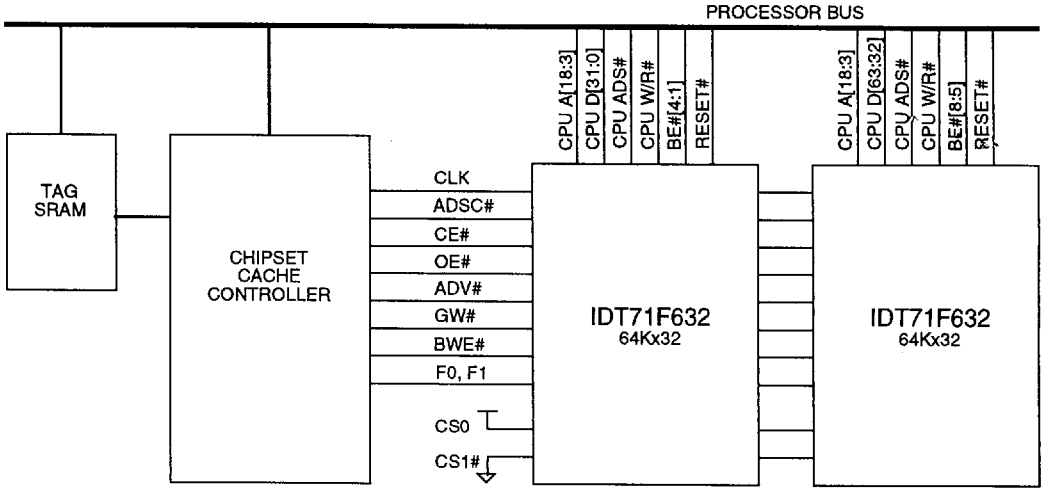
What is the difference between MoSys MCache™ and IDT's Fusion Memory?

- MCache is MoSys' trademark for their cache memory devices. Fusion Memory is IDT's trademark for the underlying technology. IDT will use the technology in other products besides cache RAMs. The IDT71F632 and MoSys' MCache devices are interchangeable.



Fusion Memory™ Provides SRAM Performance at DRAM Cost

256KB CACHE BLOCK DIAGRAM



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PIN DESCRIPTION SUMMARY

SYMBOL	DESCRIPTION	TYPE	PIN NUMBER
A15 – A0	Address Inputs	Input	49, 48, 47, 46, 45, 44, 81, 82, 99, 100, 32, 33, 34, 35, 36, 37
CE#	Chip Enable	Input	98
CS0, CS1#	Chip Selects	Input	97, 92
OE#	Output Enable	Input	86
GW#	Global Write Enable	Input	88
BWE#	Byte Write Enable	Input	87
BW1#, BW2#, BW3#, BW4#	Individual Byte Write Selects	Input	93, 94, 95, 96
CLK	Clock	Input	89
ADV#	Burst Address Advance	Input	83
ADSC#	Address Status (Cache Controller)	Input	85
ADSP#	Address Status (Processor)	Input	84
I/O31-I/O0	Data Input/Output	I/O	29, 28, 25, 24, 23, 22, 19, 18, 13, 12, 9, 8, 7, 6, 3, 2, 79, 78, 75, 74, 73, 72, 69, 68, 63, 62, 59, 58, 57, 56, 53, 52
NC	Reserved for LBO# (burst order)	NC	31
NC	Reserved for ZZ (sleep)	NC	64
RESET#	Host Bus Reset Signal	Input	38
W/R#	Host Bus W/R#	Input	39
F0	Function 0	Special	43
F1	Function 1	Special	42
VDD5	5V Power	Pwr	16, 66
VDD	3.3V Power	Pwr	4, 11, 15, 20, 27, 41, 54, 61, 65, 70, 77, 91
VSS	Ground	Gnd	5, 10, 17, 21, 26, 40, 55, 60, 67, 71, 76, 77

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ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Unit
V_{DD5}	V_{DD5} Voltage with Respect to Vss	0 to 5.5	V
V_{DD}	V_{DD} Voltage with Respect to Vss	0 to 3.6	V
V_{TERM}	Terminal Voltage with Respect to Vss	–0.5 to V_{DD}+0.5	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–55 to +125	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	20	mA

NOTE: 3620 tbl 02

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD5}	Supply Voltage	4.75	5.0	5.25	V
V_{DD}	Supply Voltage	3.135	3.3	3.6	V
Vss	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.0	—	V_{DD}+0.3	V
V_{IL}	Input Low Voltage	–0.3(3)	—	0.8	V

NOTES: 3620 tbl 03

1. Power sequencing. V_{DD5} must be ≥ V_{DD} at all times, including during power up.
2. V_{IH} (max.) must be observed at all times, including during power up.
3. V_{IL} (min.) = –1.0V for pulse width less than $t_{CYC}/2$, once per cycle.

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (V_{DD} = 3.3V +10/-5%, V_{DD5} = 5V ± 5%)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{DD} = Max., V_{IN} = 0V to V_{DD}	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	Outputs disabled, V_{OUT} = 0V to V_{DD}, V_{DD} = Max.	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = 5mA, V_{DD} = Min.	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = –5mA, V_{DD} = Min.	2.4	—	V

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DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE(1,2) (V_{DD} = 3.3V +10/-5%, V_{DD5} = 5V ± 5%)

Symbol	Parameter	Test Condition	5V Supply	3.3V Supply	Unit
I_{DD}	Operating Supply Current	Device Selected, V_{IN} ≥ V_{IH} or ≤ V_{IL}, Outputs Open, V_{DD} = Max., V_{DD5} = Max., f = f_{MAX}(3)	55	18	mA
I_{SB}	Idle Supply Current	Device Selected, ADSP#, ADSC#, GW#, BW#s, ADV# ≥ V_{HD}, All Other Inputs ≥ V_{IH} or ≤ V_{IL}, Outputs Open, V_{DD}, V_{DD5} = Max., f = f_{MAX}(3)	35	2	mA
I_{SB1}	Clock Stopped Supply Current	V_{IN} ≥ V_{HD}, Outputs Open, V_{DD} = Max., V_{DD5} = Max., f = 0(3)	15	0.1	mA

NOTES: 3620 tbl 05

1. All values are maximum guaranteed values.
2. V_{HD} = V_{DD}-0.2V, V_{LD} = 0.2V
3. At f = f_{MAX}, address inputs are cycling at the maximum frequency of read cycles; f=0 means no address input lines are changing.

AC ELECTRICAL CHARACTERISTICS

(V_{DD} = 3.3V +10/-5%, T_A = 0 to 70°C)

Symbol	Parameter	IDT71F632S75		IDT71F632S66		Unit
		Min.	Max.	Min.	Max.	
Clock Parameters						
t_F	Clock Frequency	—	75	—	66.7	ns
t_{CYC}	Clock Cycle Time	13.3	—	15	—	ns
t_{CH}(1)	Clock High Pulse Width	5	—	6	—	ns
t_{CL}(1)	Clock Low Pulse Width	5	—	6	—	ns
Output Parameters						
t_{CD}	Clock High to Valid Data	—	6	—	7	ns
t_{CDC}	Clock High to Data Change	2	—	2	—	ns
t_{CLZ}(2)	Clock High to Output Active	0	—	0	—	ns
t_{CHZ}(2)	Clock High to Data High-Z	2	15	2	15	ns
t_{OE}	Output Enable Access Time	—	6	—	7	ns
t_{OLZ}(2)	Output Enable Low to Data Active	0	—	0		ns
t_{OHZ}(2)	Output Enable High to Data High-Z	—	6	—	7	ns
Set Up and Hold Times						
t_{Sxx}	Input Setup Time	2.0	—	2.0	—	ns
t_{Hxx}	Input Hold Time	3.0	—	3.0	—	ns

NOTES:

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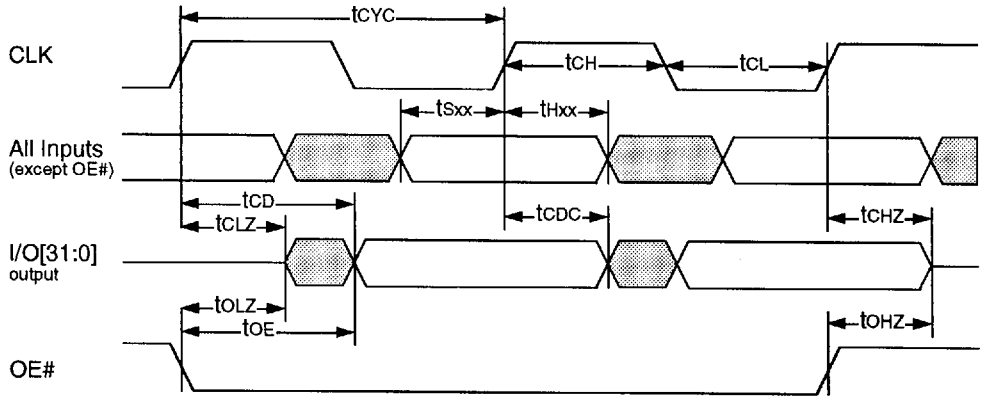
1. Measured as HIGH above 2.0V and LOW below 0.8V.
2. Transition is measured ±200mV from steady-state.

TIMING WAVEFORMS



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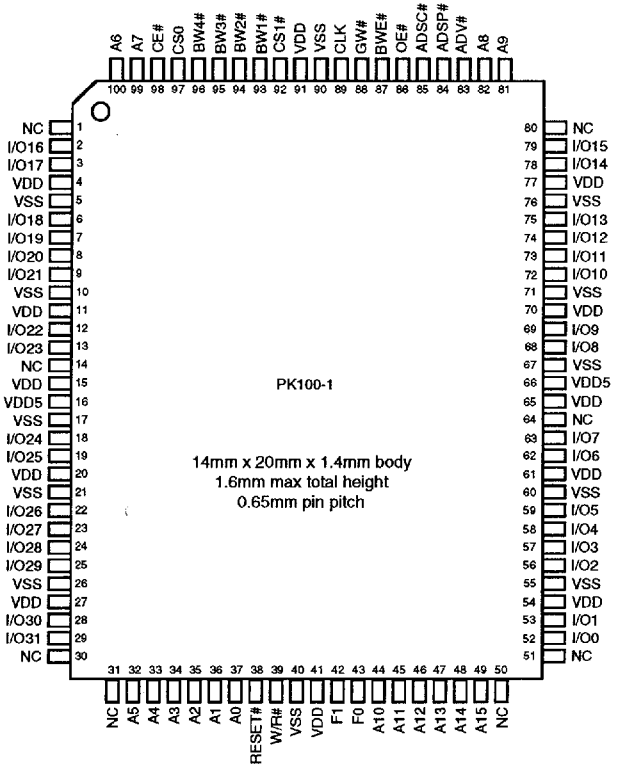
PIN CONFIGURATION



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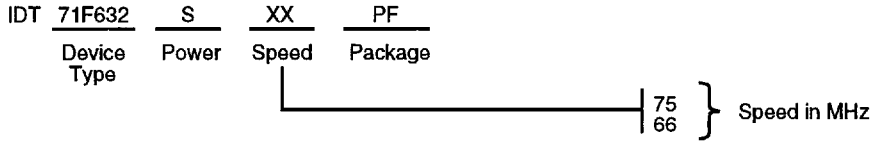
TOP VIEW
TQFP

ORDERING INFORMATION



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