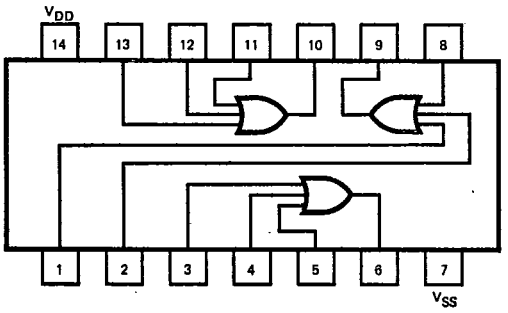
GD4075B

TRIPLE 3-INPUT OR GATE

DESCRIPTION — This CMOS logic element provides the positive Triple 3-Input OR function. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.

LOGIC AND CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE: The SO Package has the same pinouts (Connection Diagram) as the Dual In-line Package..

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			1			2			4	μA	MIN, 25°C	All inputs at 0 V or V_{DD}
					7.5			15			30		MAX	
		XM			0.25			0.5			1	μA	MIN, 25°C	
					7.5			15			30		MAX	

AC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay		59	130		34	65		28	50	ns	C_L = 50 pF,
t_{PHL}			62	130		30	65		24	50		R_L = 200 kΩ
t_{TLH}	Output Transition Time		70	135		35	75		25	35	ns	Input Transition
t_{THL}			70	135		35	75		25	35		Times ≤ 20 ns

NOTES:
1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.