Signetics

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FAST Products	

FAST 74F269 Counter

8-Bit Bidirectional Binary Counter

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F269	115MHz	95mA

FEATURES

- **Synchronous counting and loading**
- **Built-in look-ahead carry capability**
- **Count frequency 115 MHz typ**
- **Supply current 95mA typ**

DESCRIPTION

The 74F269 is a fully synchronous 8-stage Up/Down Counter featuring a preset capability for programmable operation, carry look-ahead for easy cascading and a U/$\overline{D}$ input to control the direction of counting. All state changes, whether in counting or parallel loading, are initiated by the rising edge of the clock.

ORDERING INFORMATION

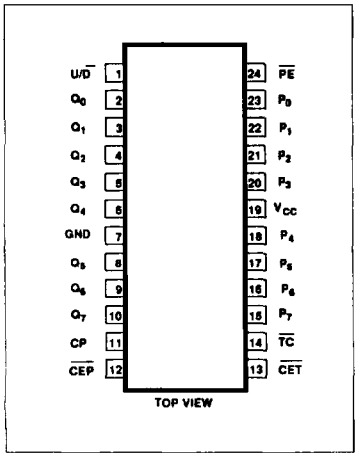
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
24-Pin Plastic Slim Dip (300 mil)	N74F269N
24-Pin Plastic SOL	N74F269D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

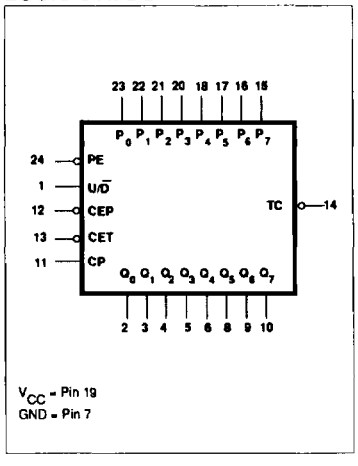
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
P_0 - P_7	Parallel Data inputs	1.0/1.0	20µA/0.6mA
$\overline{PE}$	Parallel Enable input (active Low)	1.0/1.0	20µA/0.6mA
U/$\overline{D}$	Up/Down count control input	1.0/1.0	20µA/0.6mA
$\overline{CEP}$	Count Enable Parallel input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{CET}$	Count Enable Trickle input (active Low)	1.0/1.0	20µA/0.6mA
CP	Clock input	1.0/1.0	20µA/0.6mA
$\overline{TC}$	Terminal Count output (active Low)	50/33	1.0mA/20mA
Q_0 - Q_7	Flip-flop outputs	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

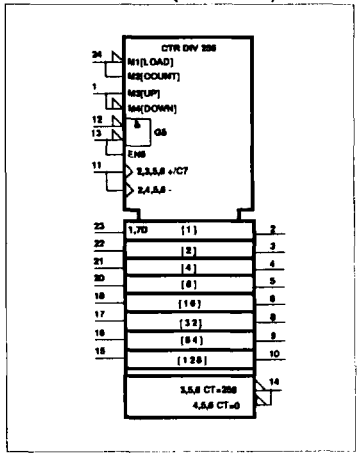
PIN CONFIGURATION



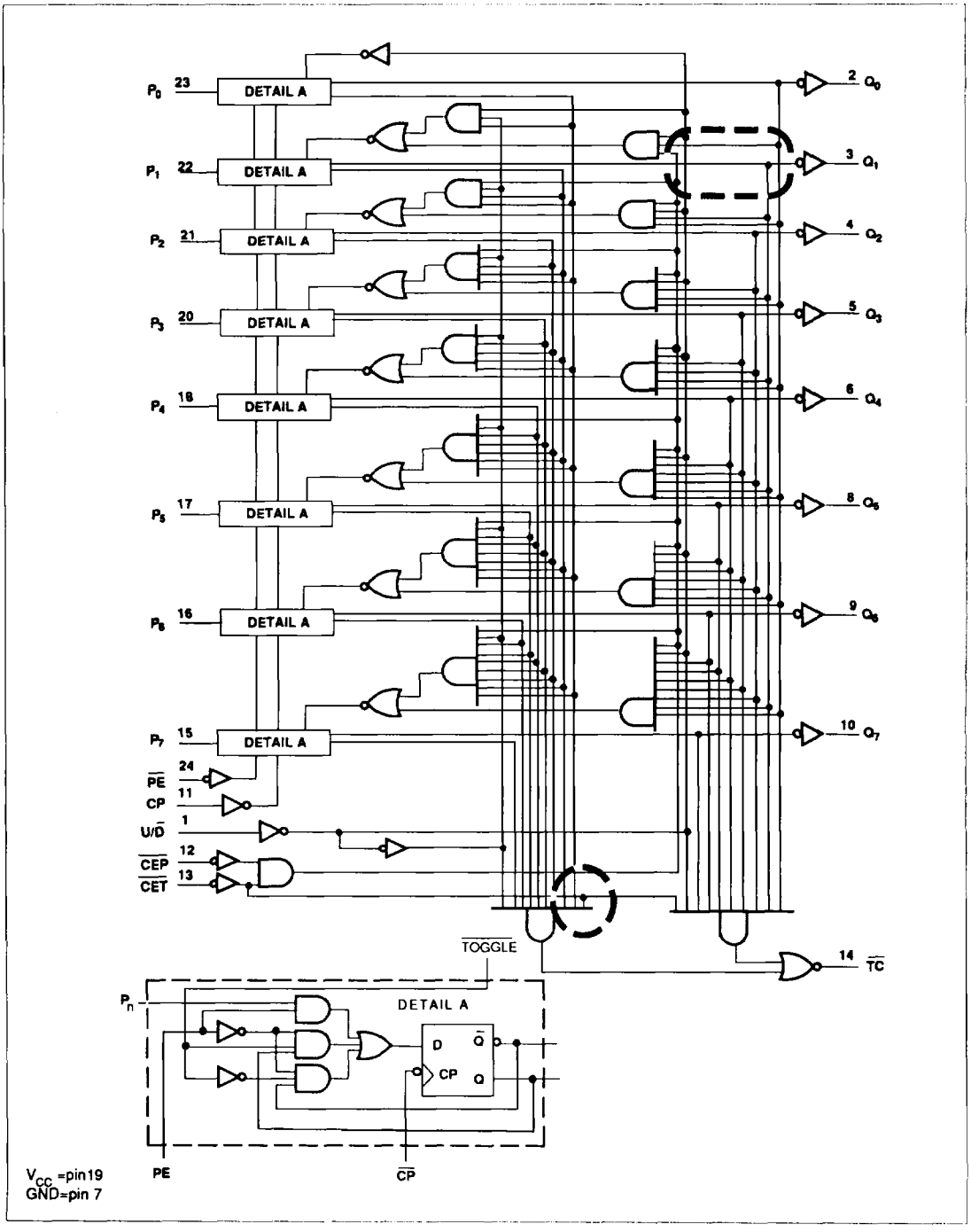
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



MODE SELECT-FUNCTION TABLE

INPUTS						OUTPUTS		OPERATING MODE
CP	U/$\overline{D}$	$\overline{CEP}$	$\overline{CET}$	$\overline{PE}$	P_n	Q_n	$\overline{TC}$	
↑	X	X	X	l	l	L	(a)	Parallel load
↑	X	X	X	l	h	H	(a)	
↑	h	l	l	h	X	Count up	(a)	Count up
↑	l	l	l	h	X	Count down	(a)	Count down
↑	X	h	l	h	X	q_n	(a)	Hold (do nothing)
↑	X	X	h	h	X	q_n	H	

H = High voltage level
h = High voltage level one setup prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one setup prior to the Low-to-High clock transition
q = Lower case letters indicate the state of the referenced output prior to the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition
(a) = $\overline{TC}$ is Low when $\overline{CET}$ is Low and the counter is at Terminal Count. The Terminal Count up is with all Q_n outputs High andTerminal Count Down is with all Q_n outputs Low.

APPLICATION

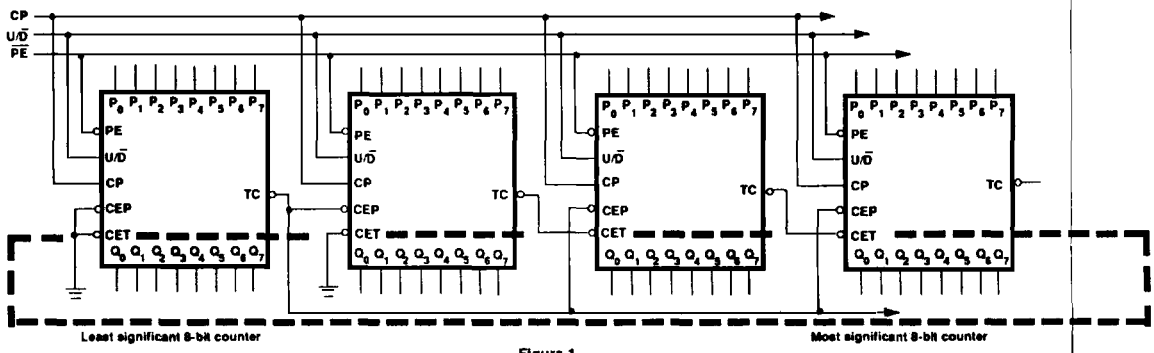


Figure 1

Synchronous multistage counting scheme