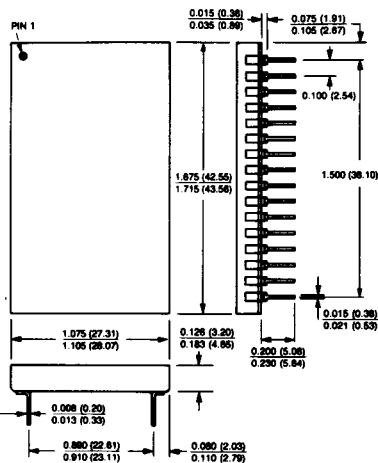


## FEATURES

- Small 32-Pin DIP
- Internal Clock and Reference
- Maximum Conversion Time:  
MN5280 100 $\mu$ sec  
MN5282 50 $\mu$ sec
- Maximum Linearity Error:  
 $\pm 0.003\%$ FSR @ +25°C  
 $\pm 0.006\%$ FSR 0°C to +70°C
- 14-Bit No Missing Codes
- $\pm 12$ ppm/°C Gain Drift  
 $\pm 2$ ppm/°C Offset Drift
- 6 User-Selectable Input Ranges
- Optional Offset and Gain Adjustments

## 32 PIN DIP



## DESCRIPTION

MN5280 and MN5282 are low-cost, 16-bit, successive approximation A/D converters that combine excellent performance with the convenience of dual-in-line packaging. Designed to be low-cost, physically small alternatives to currently available modular and p.c. card, high-resolution A/D converters, MN5280 and MN5282 have an extremely versatile pinout (6 user-selectable input ranges, short-cycle pin, status line, clock output, reference output, gain and offset adjust points) and a specification technique that makes them the most convenient, easy-to-use, high-resolution A/D's available. Linearity error is guaranteed not to exceed  $\pm 0.003\%$ FSR (equivalent to  $\pm 1/2$ LSB for 14 bits) at room temperature or  $\pm 0.006\%$ FSR over the devices' entire 0°C to +70°C operating temperature range. Accuracy at room temperature and over temperature is fully specified in terms of absolute accuracy (for the user who is not using initial gain and offset adjustments) and in terms of gain and offset initial error and drift specifications (for the user who adjusts these parameters at room temperature).

MN5280 and MN5282 are functionally identical except MN5280 is guaranteed to perform a conversion in less than 100 $\mu$ sec while MN5282 converts in under 50 $\mu$ sec. Both devices use contemporary hybrid construction techniques to combine the best monolithic chips available with Micro Networks own sputtered thin-film resistor networks in a single functional design. Outstanding room temperature performance comes from active, functional laser trimming of resistor networks.

MN5280 and MN5282 fill the need for a reliable, high-resolution A/D converter in a microprocessor-compatible package. Applications include electronic weighing equipment; high-resolution biomedical scanning equipment; nuclear accelerator and seismological instrumentation; and other precision-measurement and data-acquisition applications. Other high-resolution A/D's available from Micro Networks include MN5284 (16 bits, 300mW), MN5290/91 (16 bits, 40 $\mu$ sec), MN5295/96 (16 bits, 17 $\mu$ sec), MN6290/91 (internal T/H, 20kHz) and MN6295/96 (internal T/H, 50kHz).

# MN5280 MN5282 DIP-PACKAGED 16-Bit A/D CONVERTERS

## ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	-25°C to +85°C
Specified Temperature Range	0°C to +70°C
Storage Temperature Range	-55°C to +125°C
+15V Supply (+V <sub>CC</sub> , Pin 30)	-0.5 to +18 Volts
-15V Supply (-V <sub>CC</sub> , Pin 31)	+0.5 to -18 Volts
+5V Supply (+V <sub>DD</sub> , Pin 17)	-0.5 to +7 Volts
Analog Input (Pins 24 and 25)	±25 Volts
Digital Inputs (Pins 18 and 22)	0 to +5.5 Volts

## ORDERING INFORMATION

PART NUMBER \_\_\_\_\_ **MN528X**

Select MN5280 for 100μsec conversion time, MN5282 for 50μsec conversion time \_\_\_\_\_

Either unit is fully specified for 0°C to +70°C (ambient) operation

## SPECIFICATIONS (T<sub>A</sub> = +25°C, Supply Voltages ±15V and +5V unless otherwise indicated).

ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Input Voltage Ranges: Unipolar Bipolar		0 to +5, 10, 20 ±2.5, 5, 10		Volts Volts
Input Impedance: 0 to +5V, ±2.5V 0 to +10V, ±5V 0 to +20V, ±10V		2.5 5 10		kΩ kΩ kΩ
<b>DIGITAL INPUTS (Note 1)</b>				
Start Convert Command: Positive Pulse Width (Note 2) Logic Loading (Note 3)	50	1		nsec TTL Load
<b>TRANSFER CHARACTERISTICS (Note 4)</b>				
Linearity Error (Note 5): +25°C 0°C to +70°C		±0.0015 ±0.003	±0.003 ±0.006	%FSR %FSR
Linearity Drift		±1	±2	ppm of FSR/°C
Differential Linearity Error Differential Linearity Drift		±0.003 ±2	±0.006 ±4	%FSR ppm of FSR/°C
No Missing Codes (14 Bits) (Note 6)		Guaranteed		
Full Scale Absolute Accuracy Error (Notes 7,8): +25°C 0°C to +70°C		±0.075 ±0.15	±0.15 ±0.3	%FSR %FSR
Unipolar Offset Error (Notes 7,8): +25°C 0°C to +70°C Drift		±0.04 ±0.08 ±2	±0.08 ±0.12	%FSR %FSR ppm of FSR/°C
Bipolar Zero Error (Notes 7,8): +25°C 0°C to +70°C		±0.05 ±0.08	±0.1 ±0.015	%FSR %FSR
Bipolar Offset Error (Notes 7,8): +25°C 0°C to +70°C Drift		±0.05 ±0.12 ±7	±0.1	%FSR %FSR ppm of FSR/°C
Gain Error (Notes 7,8): +25°C 0°C to +70°C Drift		±0.08 ±0.12 ±12		% % ppm/°C
Conversion Time (Notes 9, 10) 16 Bits: MN5280 MN5282		80 40	100 50	μsec μsec
Warmup Time (To Specified Accuracy)		3		Min.
<b>DIGITAL OUTPUTS (Note 1)</b>				
Parallel Output Coding (Note 11): Unipolar Ranges Bipolar Ranges		CSB COB, CTC		
Output Drive Capability (Note 3): Parallel Outputs Status Output Internal Clock Output		2 2 2		TTL Loads TTL Loads TTL Loads
Internal Clock Frequency: MN5280 MN5282	160 320	200 400		kHz kHz
<b>REFERENCE OUTPUT</b>				
Internal Reference: Voltage Accuracy Tempco External Current		+10.000 ±0.05 ±10		Volts % ppm/°C mA

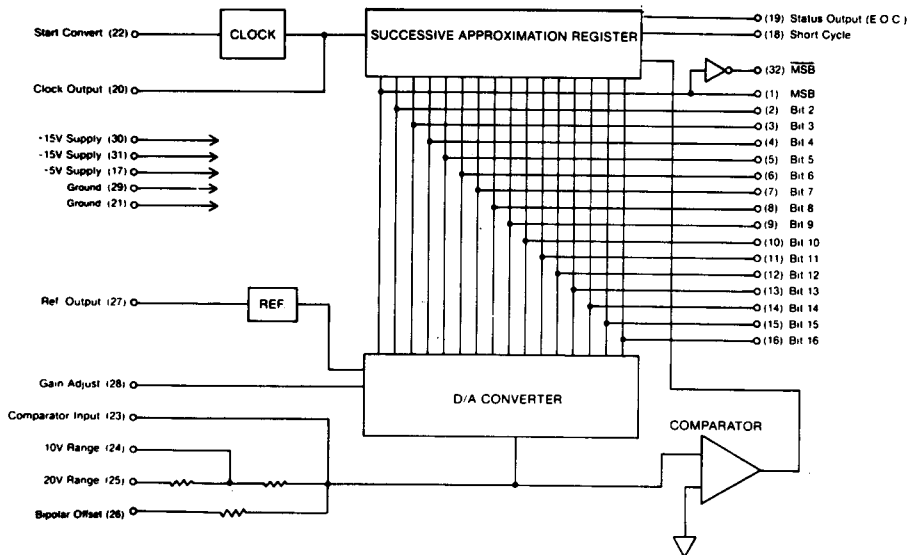
POWER SUPPLIES	MIN.	TYP.	MAX.	UNITS
Power Supply Range (Note 12): ± 15V Supplies + 5V Logic Supply	± 14.55 + 4.75	± 15 + 5	± 15.45 + 5.25	Volts Volts
Power Supply Rejection: + 15V Supply - 15V Supply + 5V Logic Supply		± 0.004 ± 0.004 ± 0.001		%FSR/% Supply %FSR/% Supply %FSR/% Supply
Current Drain: + 15V Supply - 15V Supply + 5V Logic Supply		25 - 35 100	35 - 45 120	mA mA mA
Power Consumption		1400	1800	mW

### SPECIFICATION NOTES:

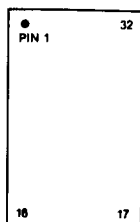
- DTL/TTL compatible, i.e., logic "0" = 0.8V max, logic "1" = 2.0V min for digital inputs. Logic "0" = 0.4V max, logic "1" = 2.4V min for digital outputs.
- Conversion is initiated on falling edge of start convert command. See timing diagram.
- One TTL load is defined as sinking 40 $\mu$ A with a logic "1" applied and sourcing 1.6mA with a logic "0" applied.
- FSR = Full Scale Range. A unit connected for  $\pm$  10V analog input range has a 20V FSR. A unit connected for  $\pm$  5V or 0 to + 10 analog input range has a 10V FSR. For a 16 bit converter, 1 LSB is equivalent to 0.00153% FSR.
- $\pm$  0.003% FSR is equivalent to  $\pm$  1/2 LSB for 14 bits.  $\pm$  0.006% FSR is equivalent to  $\pm$  1/2 LSB for 13 bits. Micro Networks tests and guarantees maximum linearity error at 0°C, + 25°C, and + 70°C.
- No Missing Codes for 13 bits is guaranteed over the entire specified temperature range.
- Full Scale Absolute Accuracy Error and Bipolar Zero Error include offset, gain, linearity, noise, and all other errors and are specified without adjustment. For operation over temperature, the MN5280 and MN5282

- are specified with absolute accuracies for the user who is not using initial gain and offset adjustments and with gain and offset drift specifications for the user who is gain and offset adjusting at room temperature. See page 6 of this data sheet and the tutorial section of the Micro Networks Product Guide and Applications Manual for more detailed discussions of converter specifications.
- Offset and gain errors are specified without adjustment. Both are adjustable to zero (at a given temperature) with external trim. See page 5.
  - Conversion time is specified using internal clock. For external clock use, see page 5.
  - Conversion time may be shortened, with lower resolution, by short cycling. See page 5.
  - CSB = Complementary Straight Binary  
COB = Complementary Offset Binary  
CTC = Complementary Two's Complement  
See page 6 for details.
  - Power supplies should be kept within  $\pm$  3% to yield rated accuracy. The MN5280 and MN5282 can be operated from  $\pm$  14V to  $\pm$  16V supplies with reduced accuracy.

### BLOCK DIAGRAM

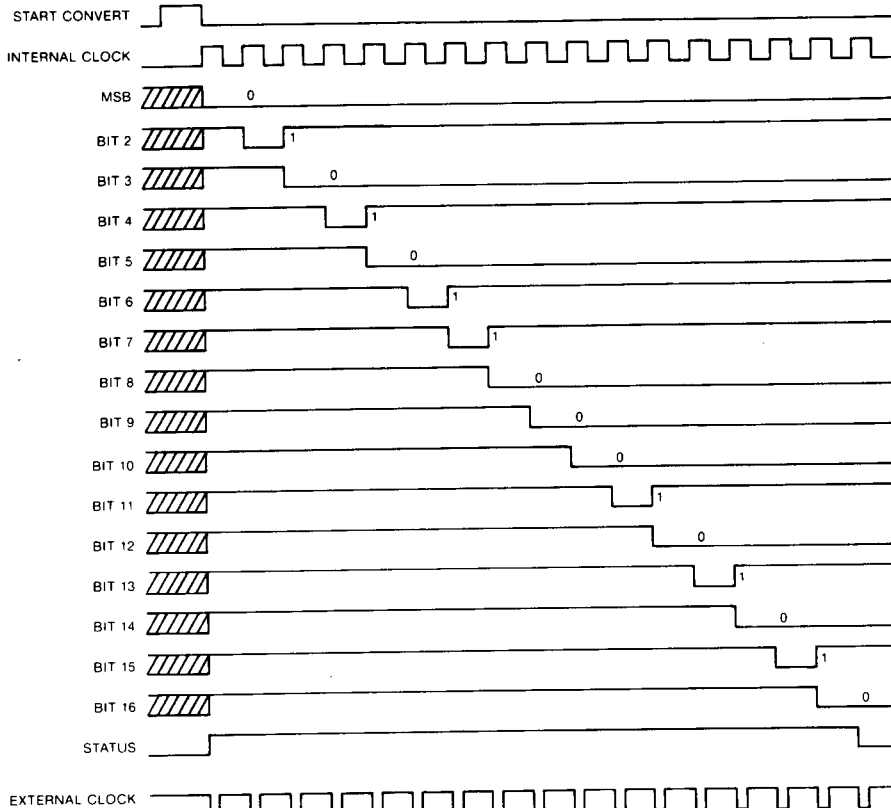


### PIN DESIGNATIONS



- |                 |                             |
|-----------------|-----------------------------|
| 1 Bit 1 (MSB)   | 32 MSB                      |
| 2 Bit 2         | 31 -15V Supply              |
| 3 Bit 3         | 30 +15V Supply              |
| 4 Bit 4         | 29 Ground                   |
| 5 Bit 5         | 28 Gain Adjust              |
| 6 Bit 6         | 27 Ref. Output (+10V)       |
| 7 Bit 7         | 26 Bipolar Offset           |
| 8 Bit 8         | 25 Analog Input (20V Range) |
| 9 Bit 9         | 24 Analog Input (10V Range) |
| 10 Bit 10       | 23 Comparator Input         |
| 11 Bit 11       | 22 Start Convert            |
| 12 Bit 12       | 21 Ground                   |
| 13 Bit 13       | 20 Clock Output             |
| 14 Bit 14       | 19 Status Output (E.O.C.)   |
| 15 Bit 15       | 18 Short Cycle              |
| 16 Bit 16 (LSB) | 17 +5V Supply               |

# TIMING DIAGRAM



### TIMING DIAGRAM NOTES:

1. Operation shown is for the digital word 0101 0110 0010 1010 which corresponds to +6.6306V on the 0 to +10V input range.
2. The START CONVERT command must be at least 50 nsec wide and must remain low during conversion.
3. The internal clock is enabled and the conversion cycle commences on the falling edge of the START CONVERT signal.
4. Data will be valid 90 nsec after the STATUS (E.O.C.) output goes low and will remain valid until another conversion is initiated.
5. When using an external clock, the converter will continuously convert. Each conversion will be initiated by the falling edge of the first external clock pulse following E.O.C.'s going low at the end of the previous conversion. See EXTERNAL CLOCK section on page 5.
6. Once a conversion has begun, a second start pulse will not reset the converter. See START CONVERT section on page 5.
7. When the converter is initially "powered up", it may come on at any point in the conversion cycle.

## APPLICATIONS INFORMATION (Applies for both MN5280 and MN5282)

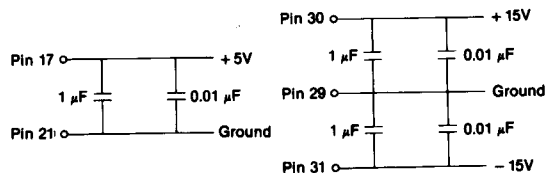
**LAYOUT CONSIDERATIONS**—Proper attention to layout and decoupling is necessary to obtain specified accuracy from the MN5282. The unit's two ground pins (pins 21 and 29) are not connected to each other internally. They must be tied together as close to the unit as possible and both connected to system analog ground, preferably to a large analog ground plane underneath the package. If these commons must be run separately, a nonpolarized 0.01  $\mu\text{F}$  ceramic bypass capacitor should be connected between pins 29 and 21 as close to the unit as possible and wide conductor runs employed.

Coupling between analog inputs and digital signals should be minimized to avoid noise pick-up. Pin 23, the high impedance input to the internal comparator, is particularly susceptible. Care should be taken to avoid long runs, or runs close to digital lines when utilizing the comparator input. In bipolar operation, where pin 26 is connected to pin 27, a short jumper should be used, and for external offset

adjustment, the 1.8 megohm resistor should be located as close to the package as possible.

Power supplies should be decoupled with tantalum and ceramic capacitors located close to the MN5282. For optimum performance and noise rejection, 1  $\mu\text{F}$  tantalum capacitors paralleled with 0.01  $\mu\text{F}$  ceramic capacitors should be used as shown in the diagrams below.

### POWER SUPPLY DECOUPLING



Whether or not external gain adjustment is used, an additional 0.01  $\mu\text{F}$  ceramic bypass capacitor should be located close to the package connecting the gain adjust point (pin 28) to analog ground (see section describing offset and gain adjustments on page 5).

If short-cycling is not used (see page 5) the short-cycle pin (pin 18) must be connected to +5V (pin 17).

**START CONVERT**—The START CONVERT signal must be a positive pulse with a minimum pulse width of 50 nsec. The falling edge of the START CONVERT signal resets the converter and turns on the internal clock. STATUS going low at the end of a conversion turns off the internal clock. If the START CONVERT input is brought high after a conversion has been initiated, the internal clock will be disabled halting the conversion. If the START CONVERT input is then brought low, the original conversion will continue with a possible error in the output bit that was about to be set when the internal clock was stopped.

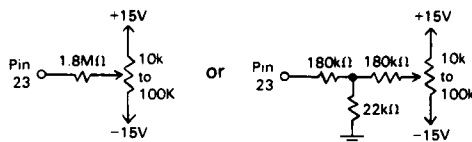
**EXTERNAL CLOCK**—An external clock may be connected to the START CONVERT input. This external clock must consist of negative-going pulses 100 to 200 nsec wide and must be at a lower frequency than the internal clock. The result is that each falling edge of the external clock turns on the internal clock for a single cycle, completing a conversion in 17 clock cycles. The internal clock will be disabled whenever the START CONVERT input is held high. When using an external clock, a START CONVERT command is unnecessary. The converter will begin to convert when the external clock is started and will provide a continuous string of conversions with each conversion starting on the first falling edge of the external clock after the STATUS output has gone low signaling the end of the previous conversion. When continuously converting in this manner, the STATUS output will go low for one external clock period following the completion of each conversion.

**STATUS OUTPUT**—The STATUS or END OF CONVERSION (E.O.C) output will be set to a logic "1" by the falling edge of the START CONVERT signal; will remain high during conversion; and will drop to a logic "0" when conversion is complete. Due to propagation delays, the least significant bit of any conversion will not be valid until a maximum of 90 nsec after the STATUS output has gone low.

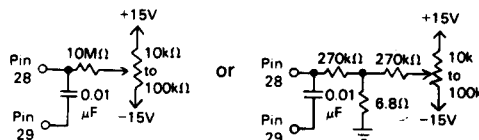
**SHORT CYCLING**—For applications requiring less than 16 bits resolution, the MN5282 can be truncated or short cycled at the desired number of bits with a proportionate decrease in conversion time. To truncate at  $n$  bits, simply connect the  $n + 1$  bit output to the SHORT CYCLE pin (pin 18). For example, to truncate at 14 bits, connect pin 15 (bit 15) to pin 18; converting will stop and the STATUS output will go low after bit 14 has been set. Due to propagation delays, the least significant bit of any conversion will not be valid until a maximum of 90 nsec after the STATUS output has gone low.

**OPTIONAL EXTERNAL OFFSET AND GAIN ADJUSTMENTS**—Initial offset and gain errors may be trimmed to zero using external potentiometers as shown in the following diagrams. Adjustments should be made following warm-up, and to avoid interaction, offset should be adjusted before gain. Fixed resistors can be  $\pm 20\%$  carbon composition or better. Multiturn potentiometers with TCR's of 100 ppm/ $^{\circ}\text{C}$  or less are recommended to minimize drift with temperature. If these adjustments are not used, pin 23 should be connected as described in the range selection section, and pin 28 should be decoupled to ground with a 0.01  $\mu\text{F}$  ceramic capacitor.

**OFFSET ADJUSTMENT**—Connect the offset potentiometer as shown, and apply the input voltage at which the 1111 1111 1111 to 1111 1111 1111 1110 transition is ideally supposed to occur (see Output Coding Table). While continuously converting, adjust the offset potentiometer until all the output bits are "1" and the LSB "flickers" on and off.



**GAIN ADJUSTMENT**—Connect the gain potentiometer as shown, and apply the input voltage at which the 0000 0000 to 0000 0000 0000 0001 transition is ideally supposed to occur. While continuously converting, adjust the gain potentiometer until all the output bits are "0" and the LSB "flickers" on and off.



**USING A SAMPLE/HOLD AMPLIFIER WITH THE MN5282**—When using a sample/hold (S/H) or track/hold (T/H) amplifier with the MN5282, the S/H can be driven directly (or inverted) from the MN5282's START CONVERT signal. When the start is high prior to the beginning of a conversion, the S/H can be in the tracking or signal acquisition mode. The falling edge of the start signal initiates the conversion and can simultaneously put the S/H into the hold mode. The MSB output will be set to its final value one internal clock period later (approximately 3  $\mu\text{sec}$ ), and the sample to hold transient of the chosen S/H should have settled to within  $\pm 0.003\%$  FSR of its final value by that time. The width of the start convert pulse may have to be lengthened to accommodate the acquisition time spec of the chosen S/H.

## INPUT RANGE SELECTION

PIN CONNECTIONS	ANALOG INPUT VOLTAGE RANGE					
	0 to +5V	0 to +10V	0 to +20V	$\pm 2.5\text{V}$	$\pm 5.0\text{V}$	$\pm 10\text{V}$
Connect Pin 26 to Pin 23	29	29	29	27	27	27
Connect Pin 25 to Pin 23	23	Open	Input	23	Open	Input
Connect Pin 23 to Pin 24	25	Open	Open	25	Open	Open
Connect Input to Pin 24	24	24	25	24	24	25
Input Impedance (K $\Omega$ )	2.5	5	10	2.5	5	10

# DIGITAL OUTPUT CODING

ANALOG INPUT						DIGITAL OUTPUT			
0 to +5V.	+10V.	+20V.	±2.5V.	±5V.	±10V	MSB	LSB		
+ F.S. + F.S. - 1 LSB			+ F.S. + F.S. - 1 LSB			0000	0000	0000	0000
+ ½ F.S. + 1 LSB + ½ F.S.			+ 1 LSB 0			0111	1111	1111	1111 <sup>#</sup>
+ ½ F.S. - 1 LSB			- 1 LSB			<del>0000</del>	<del>0000</del>	<del>0000</del>	<del>0000</del> <sup>#</sup>
+ 1 LSB 0			- F.S. + 1LSB - F.S.			1111	1111	1111	1111 <sup>#</sup>
						1111	1111	1111	1111

**CODING NOTES:**

1. For 5 volts FSR, 1 LSB = 76.3µV.
2. For 10 volts FSR, 1 LSB = 152.6µV.
3. For 20 volts FSR, 1 LSB = 305.2µV.
4. For unipolar ranges, the coding is complementary straight binary.
5. For bipolar ranges, the coding in complementary offset binary.
6. For bipolar ranges, if MSB is used instead of MSB, the coding will be complementary two's complement.

\*Analog voltages listed are the theoretical values for the transitions indicated. Ideally, with the MN5282 continuously converting, the output bits indicated as # will change from a "1" to a "0" or vice versa as the input voltage passes through the level indicated. See the section on Absolute

Accuracy Error for an explanation of Output Transition Voltages and a sketch of the MN5282's 0 to +10V and ±10V input/output transfer functions.

EXAMPLE: For the ±10V range, the transition from output code 0000 0000 0000 0000 to output code 0000 0000 0000 0001 (or vice versa) will ideally occur at an input voltage of +9.999695V (+ F.S. - 1 LSB). Subsequently, any voltage greater than +9.999695V will give a digital output of all "0's." The transition from digital output 1000 0000 0000 0000 to 0111 1111 1111 1111 (or vice versa) will ideally occur at an input of zero volts. The 1111 1111 1111 1111 to 1111 1111 1111 1110 transition will occur at -9.999695V. An input more negative than this level will give all "1's".

## ABSOLUTE ACCURACY ERROR

For any A/D converter, a given digital output code represents a band of analog input voltages that is ideally 1 LSB wide. This is demonstrated below where portions of the theoretical analog input/digital output transfer functions for the MN5282's 0 to +10V and ±10V analog input ranges are sketched.

For the 0 to +10V range, any analog input between +0.000153V (1 LSB = 0.000153 volts) and +0.000305V will give a digital output of 1111 1111 1111 1110. If we assign this code to the nominal midrange of the analog input band for which it is valid, we can say that the 1111 1111 1111 1110 digital code corresponds to analog inputs of 229 µV ± 76µV, which can be written as +229µV ± ½ LSB. The ± ½ LSB is a quantization uncertainty unavoidable in A/D conversion. It is referred to as Inherent Quantization Error, and its magnitude can be reduced only by going to higher resolution converters, i.e., converters that have smaller LSB's. It is difficult and time consuming to measure the center of a quantization level (the +229µV in this example). The points along an A/D converter's analog input/digital output transfer function that can be quickly and accurately be detected and measured are the transition voltages, the analog input voltages at which the digital outputs change from one code to the next. Refer to Figure 1. The digital output is supposed to change from 1111 1111 1111 1111 to 1111 1111 1111 1110 at exactly +0.000153V. By slowly ramping the A/D converter's input voltage and monitoring its digital outputs, you can easily find the exact voltage at which this transition actually occurs for a real A/D. The Absolute Accuracy Error of a voltage input A/D converter is the difference between the actual, unadjusted, analog input voltage at which a given digital transition occurs and the analog input voltage at which that transition is ideally supposed to occur. This difference is usually expressed in LSB's or %FSR. Absolute Accuracy Error includes gain, offset, linearity, and noise errors, and when specified over temperature, encompasses the individual drifts of these errors. As an example, look at the positive full scale end of the MN5282's 0 to +10V transfer function. The digital output code is supposed to change from 0000 0000 0000 0001 to

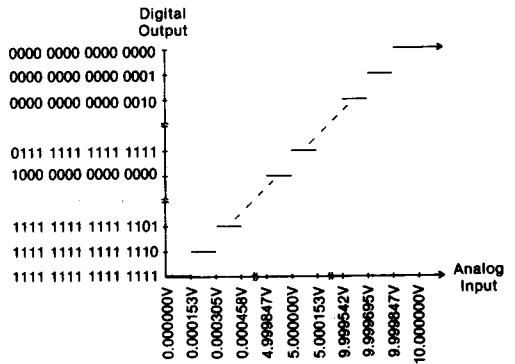


Figure 1. Input/output transfer function 0 to +10V input range.

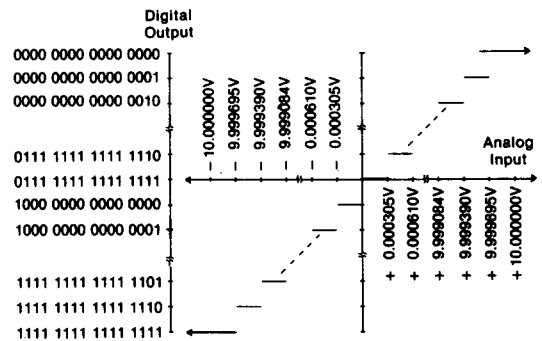


Figure 2. Input/output transfer function ±10V input range.

0000 0000 0000 at an analog input voltage of +9.999847V. If this digital output transition actually occurs at an analog input of +10.005V, the device would have a full scale absolute accuracy error of  $(+10.005V - 9.999847V) \div (10V) = +0.052\%$  FSR. If the 1111 1111 1111 1111 to 1111 1111 1111 1110 transition occurred at +0.003V instead of the ideal +0.000153V, the device would have a zero error of  $(+0.003V - 0.000153V) \div (10V) = +0.028\%$  FSR.

For all practical purposes, the transfer function of a high resolution data converter with good linearity can be considered a straight line, and the converter's accuracy specifications will describe the position of the straight line relative to its axes, i.e., they will describe how close the straight line comes to the ideal. Presently, there are two accepted techniques for describing the accuracy of data converters, and they are the same as the techniques normally used to describe the plot of a straight line on a set of axes. The line can be described by two points or by a point and a slope (angle). For the transfer function of a unipolar data converter, the first method (also called the absolute accuracy method) would normally specify a device's absolute accuracy at the two endpoints of the transfer function. The appropriate specs would be the zero error and the full scale absolute accuracy error (see Figure 3 below). The second method (point-slope) would specify the absolute accuracy at one endpoint of the transfer function (this would be the unipolar offset error) and subsequently specify the limits of the transfer function slope.

For a unipolar converter, unipolar offset error and gain error result from completely independent error sources. Therefore, at room temperature, the worst case full scale absolute accuracy of a unipolar device specified with the point-slope method would be equal to the sum of its initial unipolar offset and gain error specifications (see Figure 4). For example, if a device specified a maximum room temperature unipolar offset error of  $\pm 0.1\%$  FSR and a maximum room temperature gain error of  $\pm 0.2\%$ , its maximum room temperature full scale absolute accuracy could be as bad as  $\pm 0.3\%$  FSR.

For a bipolar converter, specifiers using the absolute accuracy method will normally list three absolute accuracy specifications; one at positive full scale, one at negative full scale and one at the bipolar zero point (the 1000 0000 0000 0000 to 0111 1111 1111 1111 transition in the case of the

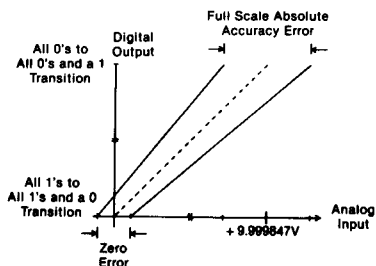


Figure 3. The absolute accuracy of a unipolar converter is normally specified at both ends of the transfer function. The dashed line shows the locus of the ideal transfer function. The solid lines show the absolute accuracy limits.

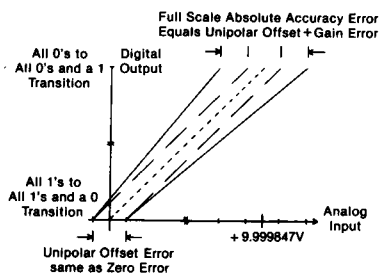


Figure 4. If a unipolar converter is specified in terms of unipolar offset and gain errors, the unipolar offset error is usually equivalent to the zero error. The worst case full scale absolute accuracy error will be equal to the sum of the unipolar offset and gain errors.

MN5282). The accuracy limits are normally in the shape of a butterfly (see Figure 5). People using the offset-gain method will still specify the absolute accuracy at one endpoint of the transfer function (this would be the bipolar offset error) and then list a gain error. The accuracy limits of a device specified in this manner are normally in the shape of a fan. For a bipolar converter, *initial* bipolar offset and gain errors result from independent error sources. Therefore, at room temperature, the worst case positive full scale absolute accuracy error of a bipolar device specified with the offset-gain method would be equal to the sum of its initial bipolar offset and gain errors. The bipolar zero error will be equivalent to the sum of the bipolar offset error and  $\frac{1}{2}$  the gain error (see Figure 6).

Unipolar and Bipolar Offset Errors are types of absolute accuracy errors. These specifications describe the accuracy of a particular output transition. For a successive approximation type of A/D converter, offset error is defined as the absolute accuracy error for the output transition that brings all of the current or voltage steering switches in the device's internal D/A converter to the "off" position. For the MN5282, this is the 1111 1111 1111 1110 to 1111 1111 1111 1111 transition. For the unipolar ranges, this transition is supposed to occur 1 LSB above zero volts, and unipolar offset error

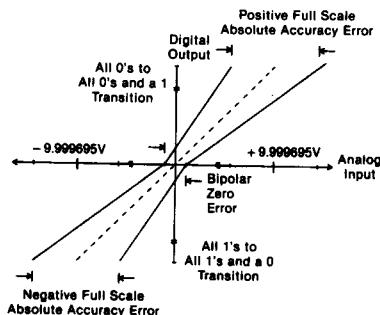
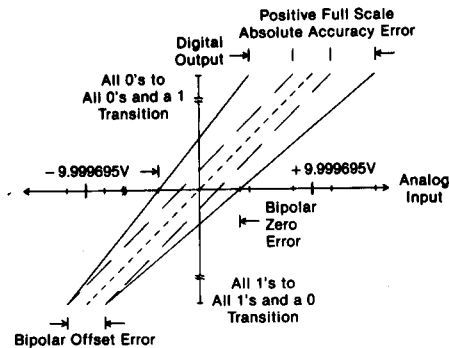


Figure 5. The absolute accuracy of a bipolar converter is normally specified at three points along the transfer function.



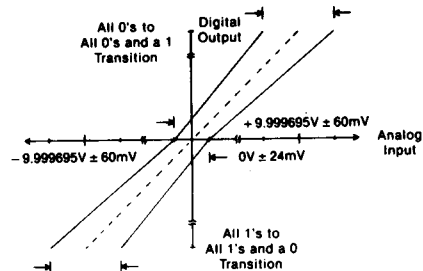
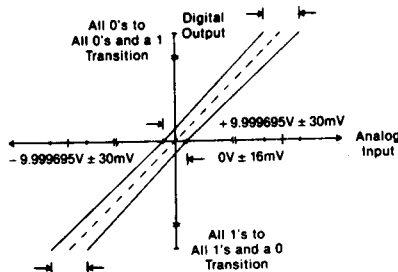
**Figure 6.** If a bipolar converter is specified in terms of bipolar offset and gain errors, the bipolar offset error is usually equivalent to the negative full scale error. The worst case positive full scale error will equal the sum of the bipolar offset and gain errors. The worst case bipolar zero error will equal the sum of the bipolar offset error and  $\frac{1}{2}$  the gain error.

has the same definition as unipolar zero error. For the bipolar ranges, this transition is supposed to occur 1 LSB above the minus full scale voltage, and bipolar offset error has the same definition as negative full scale absolute accuracy error. Bipolar offset error is not the same as bipolar zero error. Bipolar zero error describes the accuracy of the zero volt transition.

The accuracy of the MN5282's transfer function is specified using both the absolute accuracy and the point-slope methods. We list unipolar zero (unipolar offset), bipolar zero, bipolar offset, and full scale absolute accuracy errors. The full scale absolute accuracy specification applies to unipolar positive, bipolar positive, and bipolar negative full scale transition voltages. For operation over temperature, the absolute accuracy technique normally calls for unipolar zero, bipolar zero, and full scale absolute accuracy errors that apply as absolute maximums over the device's entire operating temperature range. The point-slope technique usually calls for unipolar offset drift, bipolar offset drift, and gain drift specifications that the user can use to calculate accuracy errors at given temperatures. The technique of specifying maximum absolute accuracy limits that apply over a device's entire operating temperature range is most applicable in situations in which designers are not using initial gain and offset adjustments and must concern themselves with accuracy limits or error budgets that apply over a system's entire operating temperature range. The technique of listing gain and offset drift specifications is more useful to the user who employs initial gain and offset drift adjustments and then concerns himself with accuracy drift over some limited temperature range.

The guaranteed absolute accuracy limits of the MN5282 operating on its bipolar  $\pm 10V$  input range are summarized in the sketches above. All three limits shown are fully tested and guaranteed at  $0^\circ C$ ,  $+25^\circ C$ , and  $+70^\circ C$ .

If a converter is specified using the absolute accuracy method, its accuracy at temperatures other than  $0^\circ C$ ,  $+25^\circ C$ , and  $+70^\circ C$  can usually be found through interpolation. If a converter is specified using only the point-slope (offset-gain) technique, the device's accuracy at temperatures other than  $+25^\circ C$  can be found by using the following rules. For a unipolar converter, unipolar offset drift will slide the transfer function parallel to itself along the



**Figures 7 and 8.** Unadjusted absolute accuracy limits for the MN5282's  $\pm 10V$  input range at  $+25^\circ C$  (Fig. 7) and at  $0^\circ C$  and  $+70^\circ C$  (Fig. 8).

voltage axis, and gain drift will rotate the transfer function around the point at which unipolar offset error occurs. Therefore, for the MN5282's unipolar input ranges, the zero end of the transfer function will drift according to the device's unipolar offset drift specification, and the positive full scale end of the transfer function, in the worst case situation, will drift according to the sum of the unipolar offset and gain drift specifications ( $\pm 2\text{ppm of FSR}/^\circ C \pm 12\text{ppm of FSR}/^\circ C = \pm 14\text{ppm of FSR}/^\circ C$ ). For the MN5282's bipolar input ranges, bipolar offset drift slides the transfer function parallel to itself along the voltage axis, and gain drift rotates the transfer function around the point at which bipolar offset error occurs (the minus full scale point). Because of the way the bipolar converter is designed, however, bipolar offset and the bulk of gain drift will *always* be in opposite directions with the net result that the transfer function appears to rotate around the bipolar zero point. The positive full scale drift is *not* equal to the sum of the bipolar offset and gain drift specifications but is a smaller number. It is normally a number smaller than the unipolar full scale drift. This number can usually be found using the following rules. Bipolar positive full scale accuracy drift =  $\frac{1}{2}$  reference drift + bipolar offset drift exclusive of reference drift + gain drift exclusive of reference drift. Bipolar offset drift exclusive of reference drift will normally equal bipolar offset drift minus  $\frac{1}{2}$  reference drift, and gain drift exclusive of reference drift will normally equal gain drift minus reference drift. For the MN5282, bipolar positive full scale accuracy drift will typically equal  $5 + 2 + 2 = 9\text{ppm of FSR}/^\circ C$ .