1.0 INTRODUCTION

1.1 GENERAL DESCRIPTION

This document describes the Philips Semiconductors 90C24LC Windows Accelerated High Resolution VGA LCD Controller for Low Power Applications (hereinafter referred to as the 90C24LC Controller).

The Philips Semiconductors 90C24LC is a 0.9 micron CMOS VLSI device with the capability to drive flat panel displays and standard CRTs. The 90C24LC allows simultaneous display of a CRT and a monochrome dual-panel, or a CRT and a color panel. This device is backwards compatible with previous video standards including MDA, EGA, and CGA.

The 90C24LC provides enhanced power management with 3.3 VDC power input or a mix of 3.3 VDC and 5 VDC power input. Its performance-scaling capability makes it an ideal video solution for low battery drain portable computer applications.

1.2 FEATURES OF THE 90C24LC

- Hardware Windows Acceleration
- Hardware Bit Block Transfers (BITBLT)
- Hardware line draw
- Programmable Hardware Cursor (64 by 64 by 2)
- Simultaneous Display on all CRT and LCDs for all Standard Modes
- Programmable Power Management
- Support for 256K color STN and color TFT LCDs
- Single chip for 8-bit or 16-bit AT Bus Interface and 32-bit VESA VL-Bus (local bus) interface
- Supports 16-bit or 32-bit memory interface
- Integrated 16-bit High Color RAMDAC
- Integrated Programmable Pixel Clock Synthesizer
- Integrated Programmable Dithering Logic for the Highest Contrast Video with Utility Support.
- Support for 64K simultaneous colors on CRT, single-panel color STN LCD, and color TFT LCD
- Direct interface to single-panel (1/480) or dual-panel (1/240) monochrome STN LCD, single or dual panel color STN or color TFT LCD and plasma display
- Provides 64 True Shade gray scale support for monochrome STN LCD flat panel display
- Up to 65 MHz video clock for the CRT display, up to 65 MHz for color TFT LCD display, and up to 50 MHz video clock for the monochrome STN LCD display
- Up to 50 MHz memory clock
- Supports memory configuration of 256 Kbytes to 1 Mbyte with 256K by 16, or 256K by 4 DRAMs
- With 256K of DRAM installed, supports all IBM VGA modes for CRT and LCD display
- With 1 Mbyte of DRAM installed, supports high resolution graphics with up to 1024 by 768 by 256 colors in CRT and flat-panel modes.
- Provides host data bus interface for 8- or 16-bit CPU I/O and memory cycles.
- Supports high 16-bit color for CRT or flat panel display at up to 640 by 480 resolution for 64K color simultaneous display on one frame for CRT, color STN LCD, and color TFT LCD displays
- Fast page display memory fetching for both graphic and text modes
- Programmable virtual memory addressing for CPU memory address space
- Four levels of write cache for zero wait state CPU operation during memory write
- Emulates planar mode addressing for packed pixel mode operation to achieve faster block transfers

- Operates with 5 volt and 3.3 volt power supplies (mixed voltage operation)
- Intelligent power management control to reduce the power requirement for the display subsystem
- Supports 132-column text mode
- Provides a signature analyzer to help with IC and board-level test of video data output from the controller.
- PINSCAN I/O mapping allows the 90C24LC to enter a test mode to enable quick open and short checks for board-level test
- Uses 208-pin EIAJ package
- Directly drives all 640 by 480 (400) monochrome and color flat panel displays, such as STN, TFT, EL, and plasma displays without external components
- Provides a Dual panel (1/240) color STN LCD interface.
- Supports monochrome 640 by 480 single-panel (1/480) STN, 4-bit or 8--bit, flat-panel
- Provides algorithm enhancement to support vertical screen expansion in text mode. Raster lines are duplicated above or below the character block. This takes care of not creating breaks in continuous vertical lines.
- A Strip Line Draw algorithm is implemented in hardware to further improve Windows performance.
- I/O pins are remapped to improve the ICT (In-Circuit Test) of the device. Because there are more input pins than output pins, pairs of input pins had to be ORed to each output. There was a conflict in 3 pairs of pins in that they were next to each other, which would not allow for a "short test" on those pins. These 3 pairs of pins were AMD12 and AMD3, BMD12 and BMD3, and $\overline{\text{EBROM}}$ and $\overline{\text{VLBICS}}$.
- Supports hardware cursor for Dual panel (1/240) monochrome STN LCD panels.
- The PCLK output (pin 175) can now be turned off by a programmable bit to reduce EMI emissions.
- Configuration bit (CNF15) is added to accept the 2X clock from the new Intel S-series 486 microprocessors.
- Supports 800 by 600 color TFT panel.
- Supports enhanced power-down mode on VESA-VL local bus ($\overline{\text{REFLCL}}$)
- In Power-down mode, register PR4 bit 5 is used to turn off the panel data and control pins (XSCLK, RPTL/, WPTL/, UD(7:0), LD(7:0), FP, LP and FR). In the 90C24 these pins are tristated.

1.3 ORDERING INFORMATION

The 90C24LC controller is supplied in a 208-pin MQFP package under the following order number:

90C24LCZZ00

1.4 DOCUMENT SCOPE

In addition to this introduction to the 90C24LC controller, the following sections of this document provide a description of the controller architecture and related interfaces, memory configurations, signal descriptions, and internal register descriptions. In addition, this document contains application information for the hardware cursor, hardware BITBLT, hardware line drawing, embedded clock generator, internal RAMDAC, configuration registers, and associated application and program notes. Also included are the device specifications, timing information, and package dimensions. Special features of the 90C24LC including the signature analyzer, and I/O mapping for test purposes are also described.

This document includes the following two appendices:

Appendix A lists reference documents that may be useful to users of this document.

Appendix B provides a change history for this document.

2.0 ARCHITECTURE

2.1 INTRODUCTION

The 90C24LC controller is made up of the following major internal modules:

- CRT Controller
- Sequencer
- Graphics Controller
- Attribute Controller
- Flat Panel Controller and Interface
- VESA VL-Bus (Local Bus) Interface
- Hardware Cursor
- Dithering Engine
- Weight and Mapping Logic
- RAMDAC
- Clock Synthesizer
- Power-down Management
- Hardware Bit Block Transfer (BITBLT)
- Hardware Line Drawing
- Frame Buffer Controller

Each module is described in this section. Their interconnections are shown in Figures 2-1 and 2-2.

The 90C24LC uses a four-level write cache to achieve fast memory writes. Therefore, with a 32-bit display memory interface, zero wait states can be realized for most memory write operations.

Fast Page mode memory fetching is used to improve memory bandwidth. The 90C24LC uses a FIFO to provide the video display bandwidth necessary to interleave CPU accesses and display refresh cycles.

Weighting and Mapping Logic provides color-to-gray-scale mapping, and a dithering engine, that works like a digital DAC, generating the gray scale level for monochrome flat-panel displays. The dithering engine also generates colors for color flat-panel display. While driving the flat panel, a Row Buffer supports the split screen displays.

To support a split screen display when driving a flat panel and a CRT simultaneously, an external Frame Buffer may be required

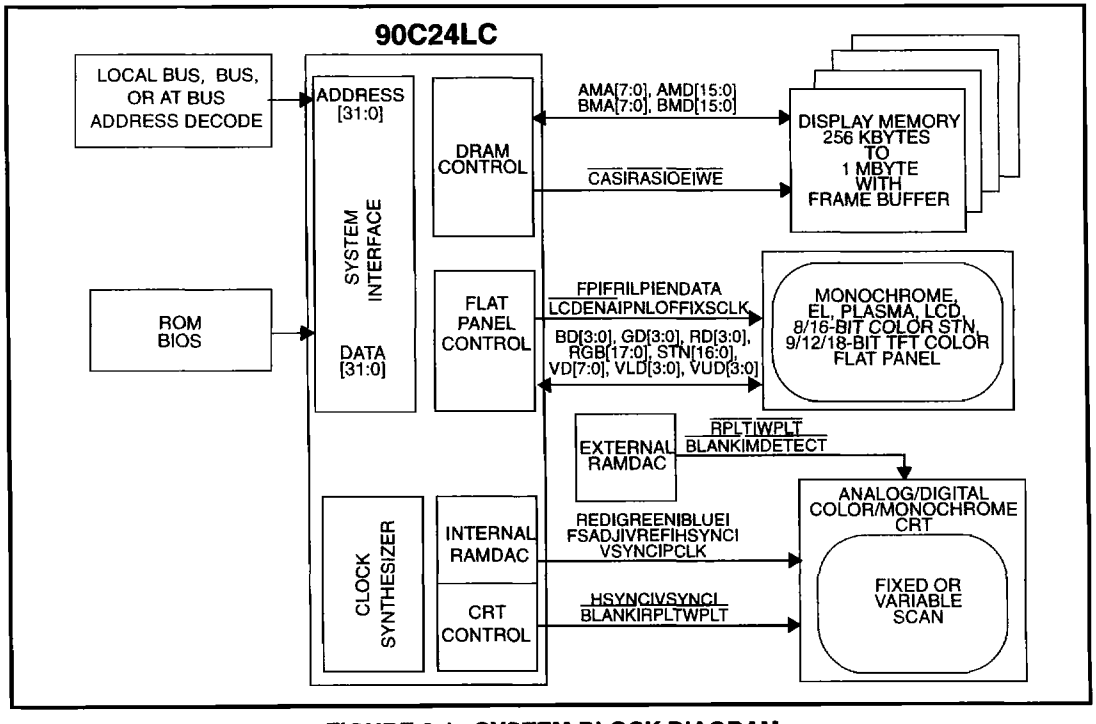

FIGURE 2-1. SYSTEM BLOCK DIAGRAM

2.2 CRT CONTROLLER

The CRT Controller performs the following functions:

- Generates horizontal sync (HSYNC) and vertical sync (VSYNC) for the CRT display monitor
- Simultaneous CRT and dual flat panel display is performed using frame buffer architecture
- Hidden display timing registers meet the fixed display timing for the flat panel display
- CRT display screen refresh is maintained for the various display modes defined by the BIOS ROM resident firmware
- Performs video split screen refresh and screen size mapping

2.3 SEQUENCER

The Sequencer performs the following functions:

- Timing generator for the display memory cycles
- Character clock in the alphanumeric mode, and the dot clock in the graphics mode
- Arbitrates between the video display refresh, memory refresh, and CRT access of the display memory for CRT only, flat panel only, or simultaneous CRT and single panel displays
- Arbitrates between the video display refresh, frame buffer access, memory refresh, and CRT access of the display memory for simultaneous CRT and dual panel displays
- Arbitrates cursor pattern access to the off-screen display memory when the hardware cursor is activated
- Provides the write cache control for CPU memory write to the video display memory

2.4 GRAPHICS CONTROLLER

The Graphics Controller manipulates the data flow between the CPU and the display memory for CPU write and read cycles. The Graphics Controller also controls data written to the CPU display memory.

2.5 ATTRIBUTE CONTROLLER

The Attribute Controller allows the following functions:

- Serializes the display memory data into a video data stream according to different display formats
- Controls the following features in all display modes:
  - Blinking
  - Underlining
  - Text cursor
  - Pixel panning
  - Reverse video
  - Background and foreground color
  - Border Controller

2.6 FLAT PANEL CONTROLLER AND INTERFACE

The Flat Panel Controller and Interface Module performs the following functions:

- Controls the video data flow after video data exits the RAMDAC palette RAM until the video data is output to the flat panel interface
- Generates the flat panel control signals:
  - Frame Rate (FR)
  - Frame Pulse (FP)
  - Latch Pulse (LP)
  - Shift Clock (XSCLK)
  - Data Enable (ENABLE)

These signals are generated with different timing and polarity in order to drive different types of panels without external components

- Split screen refresh for dual panel display and screen size mapping for both single and dual panel displays
- Performs split screen refresh and screen size mapping using frame buffer architecture (screen mapping includes vertical expansion and auto-centering)
- Controls the video data flow into and out of the row buffer (using frame buffer architecture)
- Controls the video data flow into and out of the frame buffer (using frame buffer architecture)

2.7 VESA VL-BUS INTERFACE

The 90C24LC provides a VESA VL-Bus (local bus) Interface for both the 486 and 386 CPU architectures. This interface can be implemented directly on the system motherboard or on a separate option card without adding extra glue logic. Through this interface, the 90C24LC connects directly to the host CPU address, data, and control lines. Using the VESA VL-Bus significantly improves system performance.

2.8 FRAME BUFFER CONTROLLER

The Frame Buffer Controller supports simultaneous display on a dual-flat panel or on a flat panel and CRT. This feature is fully supported for memory configuration 2 (refer to Section 4).

2.9 WEIGHT AND MAPPING LOGIC

For monochrome panel displays, the weight and mapping logic converts color information from the palette RAM into gray scale information using the following weighting equation:

I =.3R +.59G +.11B.

For monochrome display panels, the output code generated by the weighting equation selects gray shades depending on the modulation type:

- **Frame-Rate Modulation**

  The weighting code selects gray shades from the mapping RAM, which is loaded with 64 user-selected codes of shades with the optimum intensity.

- **Pulse-Width Modulation**

  The weighting code truncates or rounds off the shading information and sends it to the panel directly. With this information, the panel uses pulse-width modulation to generate related gray shades.

For color panel displays, the red, green, and blue color information that comes from the palette RAM provides the code for each color. Colors are selected depending on the color panel modulation type as follows:

- **Frame-Rate Modulation**

  The red, green, blue color data selects color shades from the dithering engine.

- **Pulse-Width Modulation**

  The color data can be sent directly to the panel or truncated and then sent to the panel.

2.10 DITHERING ENGINE

The Dithering Engine uses a dithering pattern and frame-rate modulation to constantly generate 64 gray shades. The dithering pattern for each shade is designed so that it creates minimum flicker on the panel screen.

2.11 HARDWARE BIT BLOCK TRANSFER (BITBLT)

The 90C24LC was designed with hardware support for Microsoft Windows, which supports accelerated Windows performance.

The 90C24LC Bit Block Transfer (BITBLT) increases speed. With BITBLT, blocks of pixels are transferred directly between regions of display memory and between display memory and system memory through a system I/O or memory port. For additional BITBLT information refer to Section 19.

2.12 HARDWARE LINE DRAWING

The 90C24LC provides a hardware line drawing engine that implements the Microsoft strip line algorithm. With this algorithm, the line draw engine interacts with software to determine the slope of the line and the number of pixels to be turned on. Line Draw operation is described in Section 20.

2.13 HARDWARE CURSOR

The Hardware Cursor provides up to a 64 by 64 pattern. Each pixel in the pattern is represented by two bits. These two bits determine how the cursor is displayed based on the color mode selected. The pattern is stored in the off-screen display memory. The hardware cursor is controlled by the following registers:

- Cursor Control
- Cursor Pattern Address

- Cursor Primary Color
- Cursor Secondary Color
- Cursor Auxiliary Color
- Cursor Origin
- Cursor Display Address X
- Cursor Display Address Y

The Cursor Display Address is the location for the origin of the cursor on the display screen. The Cursor Pattern Address is the starting memory location where the cursor pattern is stored in the display memory.

The Cursor Origin and the Cursor Display Address are used to calculate the cursor's starting display address. The cursor pattern is displayed on the window and the controller clips off the pattern. The pattern fetching request is sent to the sequencer. The cursor pattern is displayed when the display location matches the cursor start location. For additional information on the Hardware Cursor, refer to Section 18.

2.14 RAMDAC

The on-chip RAMDAC is low-power, PS/2-compatible with power-down control and built-in monitor detection logic with the following features:

- Three 256 by 6 RAMs as the R, G, B Color look-up tables
- Three 6-bit DACs
- Mask register
- Supports 16-bit high color

The 16 bits of video data are formed by five red bits, six green bits, and five blue bits, or five bits of each color with one bit ignored.

When in high color mode, video data bypasses the color palette RAM.

The LSB bit of the three DACs are forced to zero for 5-bit color configuration. The LSB bits of the Red DAC and Blue DAC are forced to zero for the 5-bit red, 6-bit green, and 5-bit blue configuration.

The DAC generates RS-343A/RS-170 compatible output and has 1/2 LSB of integral and differential linearity errors.

2.15 CLOCK SYNTHESIZER

The on-chip Clock Synthesizer is a dual clock generator for VGA applications. It simultaneously generates display memory clock (MCLK) and video dot clock (VCLK).

Both clock frequencies can be programmed by the user and are derived from the 14.318 MHz system clock available in the IBM PC/XT/AT and PS/2 computer systems.

The clock synthesizer has power-down control to achieve a low power consumption.

When programing a new clock frequency for both MCLK and VCLK, the Clock Synthesizer requires 20 ms to achieve a stable frequency. All the registers, palette RAM, and Mapping RAM must be reloaded after the clock frequency is stable.

2.16 POWER-DOWN MANAGEMENT

The 90C24LC provides four major power down modes:

- Deep Sleep Mode
- Suspend/Resume Mode (System Power-down Mode)
- General Power Down Mode (Internal)
- Display Idle Mode

Each of the power-down management modes is described briefly in the following paragraphs. Additional information about power-down management is provided in Section 26.

Deep Sleep Mode is used when the entire display subsystem can be turned off. This mode is designed to conserve the most power and also requires the most system overhead. In this mode, the 90C24LC current sink is less than 1 mA.

Suspend/Resume mode (also called System Power Down Mode) is used when a display is not required but minimum access to the display registers is required. In this mode, all supply voltages (VDD) remain active, but the Clock Synthesizers are shut down. For Suspend/Resume mode the 90C24LC current sink is less than 10 mA.

General Power Down Mode is used to turn off the display when the keyboard has been idle for a preset time interval. In this mode all the supply voltages (VDD) and the Clock Synthesizers remain on. The MCLK and VCLK clock rates can be slowed down to 1/8 of their normal frequency.

The Display Idle Mode is used to turn off the display when the keyboard has been idle for a preset time interval. The DAC and LCD panel interfaces are turned off in this mode. The CPU can access I/O registers of the 90C24LC, but it can not access display memory.

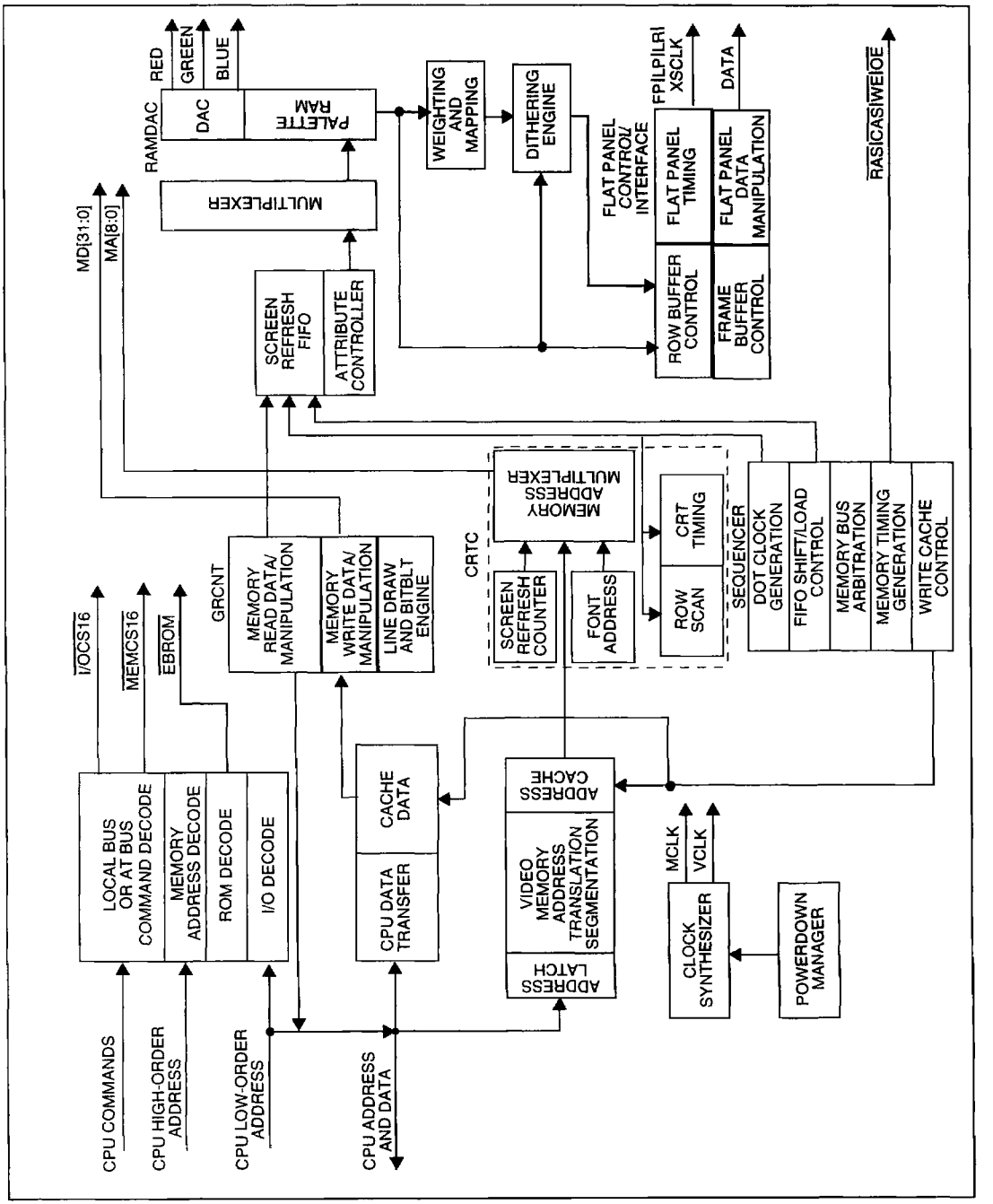

FIGURE 2-2. BLOCK DIAGRAM

3.0 INTERFACES

3.1 INTRODUCTION

The 90C24LC has five major interfaces, which are described in this section.

- System Interface
- BIOS ROM Interface
- Display Memory Interface
- ISA Bus Interface
- VESA VL-Bus Interface
- CRT Display Interface
- Flat Panel Display Interface

3.2 SYSTEM INTERFACE

The system interface operates with the following bus architectures:

- PC/XT/AT (ISA) bus (see Figure 3-1)
- VESA VL- Bus (local bus) (see Figure 3-3)
- Intel 386 DX local bus
- Intel 486 SX/DX local bus

The selection of the bus architecture depends on the setting of configuration bits CNF17 and CNF2 as listed in Table 3-1.

CNF17	CNF2	SYSTEM MODES
0	0	Reserved
0	1	ISA Bus
1	0	Reserved
1	1	Local Bus including VESA VL-Bus

TABLE 3-1. BUS ARCHITECTURE SELECTION

The bus architecture is selected during power-on and reset as described in Section 24 *90C24LC Configuration Registers.*

Other features of the system interface include:

- $\overline{\text{IOCS16}}$ and $\overline{\text{MEMCS16}}$ signals are generated to indicate 16-bit operation
- Minimal use of external circuitry
- Provides all signals, decodes all memory and I/O addresses to interface with any of the bus configurations in 8-bit or 16-bit mode.
- Decoding for video BIOS ROM while in extension card application (8-bit operation only)
- Reduced CPU wait states while writing to display memory with use of a display memory data and address write cache that holds CPU write data until it can be transferred to the display memory
- Improved performance of CPU display memory access -- PR0(A) and PR0(B) registers may be addressed indirectly
- Improved performance of CPU display memory access -- 32-bit memory data latch is addressable by the I/O port
- Sixteen segments of 1 Mbyte virtual memory addressing range or 32 segments of 512K-byte virtual memory addressing range for flexibility in memory allocation

3.3 BIOS ROM INTERFACE

The 90C24LC can be configured to provide an enable signal ($\overline{\text{EBROM}}$) for an external 8-bit video BIOS PROM. The 90C24LC is then configured to automatically map this video BIOS into the system memory map during power-on and reset. The external video BIOS can be selectively mapped out of system memory as required. Decodes are provided for 64 Kbytes of VGA video BIOS address space as defined in the VGA architecture.

3.4 DISPLAY MEMORY INTERFACE

For a 16-bit display memory interface, the following DRAM configurations can be used:

- One 256K by 16 DRAM or four 256K by 4 DRAMs
- Two 256K by 16 DRAMs

For a 32-bit memory interface, the following DRAM configurations can be used:

- Two 256K by 16 DRAMs
- Eight 256K by 4 DRAMs

Refer to Section 4 for a summary of display memory configurations.

In all cases, 90C24LC uses DRAM fast page mode for optimum performance.

3.4.1 Minimum Configuration

In the minimum configuration, which is one 256K by 16 DRAM, the 90C24LC can support all standard IBM VGA modes.

When additional DRAMs are installed, the 90C24LC is capable of supporting high color resolution video modes of up to 1024 by 768 by 256 colors, non-interlaced and 1280 by 1024 by 16 colors, interlaced.

3.4.2 Display Memory Features

- Supports 70 ns, 80 ns, and 100 ns DRAMs with the dedicated MCLK which can operate from 37.5 MHz to 44.3 MHz

NOTE

Longer DRAM access times require slower clock frequencies. Table 3-2 lists typical DRAM access times and memory clock limitations.

DRAM ACCESS TIME IN NANOSECONDS	MCLK FREQUENCY IN MEGAHERTZ (MAX)
70	44.3
80	39.8
100	37.5

TABLE 3-2. DRAM ACCESS TIME VERSUS MEMORY CLOCK FREQUENCY

- Fast page DRAM timing is used for all CPU access, graphics display and text display (a choice of page mode and non-page mode operation is provided to access fonts in text modes)
- Generates $\overline{CAS}$-before-$\overline{RAS}$ DRAM refresh for the display memory

3.4.3 VCLK to MCLK Ratio

The VCLK to MCLK ratio for the 90C24LC controller is specified as 1.6 or less. Exceeding this ratio may cause FIFO underflow problems.

The following table lists the VCLK and MCLK frequencies, their ratios, and recommended DRAM speed for two high resolution displays.

	RESOLUTION	
	1024X768X256 NON-INTERLACED (60 Hz)	1024X768X16 INTERLACED (43hZ)
VCLK (MHz)	65	44.5
MCLK (MHz)	44.3	39.8
VCLK/MCLK RATIO	1.5	1.1
DRAM SPEED (ns)	70	80

TABLE 3-3. VCLK TO MCLK RATIOS

3.5 ISA BUS INTERFACE

The 90C24LC interfaces to an ISA bus at bus clock rates of up to 12.5 MHz. The 90C24LC supports full 16-bit I/O and memory transfers. Support of 16-bit memory transfers is independent of whether the 90C24LC has an 8-bit or 16-bit display memory path, although increased performance occurs when a 16-bit display memory is available (See Figure 3-1).

LA(23:17) addresses are latched internal to the 90C24LC by the ALE signal to eliminate bus timing problems in some common system implementations.

I/O and memory operation (8/16-bit I/0 and 8/16 bit memory) can be separately enabled by selectively enabling $\overline{\text{IOCS16}}$ and $\overline{\text{MEMCS16}}$ bus interface signals.

The following ISA Bus signals are directly supported by the 90C24LC:

AEN	$\overline{\text{MEMR}}$
$\overline{\text{BALE}}$	$\overline{\text{MEMW}}$
LA[23:17]	$\overline{\text{0WS}}$
$\overline{\text{IOCHRDY}}$	$\overline{\text{REFRESH}}$
$\overline{\text{IOCS16}}$	RESET
$\overline{\text{IOR}}$	SA [16:0]
$\overline{\text{IOW}}$	$\overline{\text{SBHE}}$
$\overline{\text{MCS16}}$	SD[15:0]

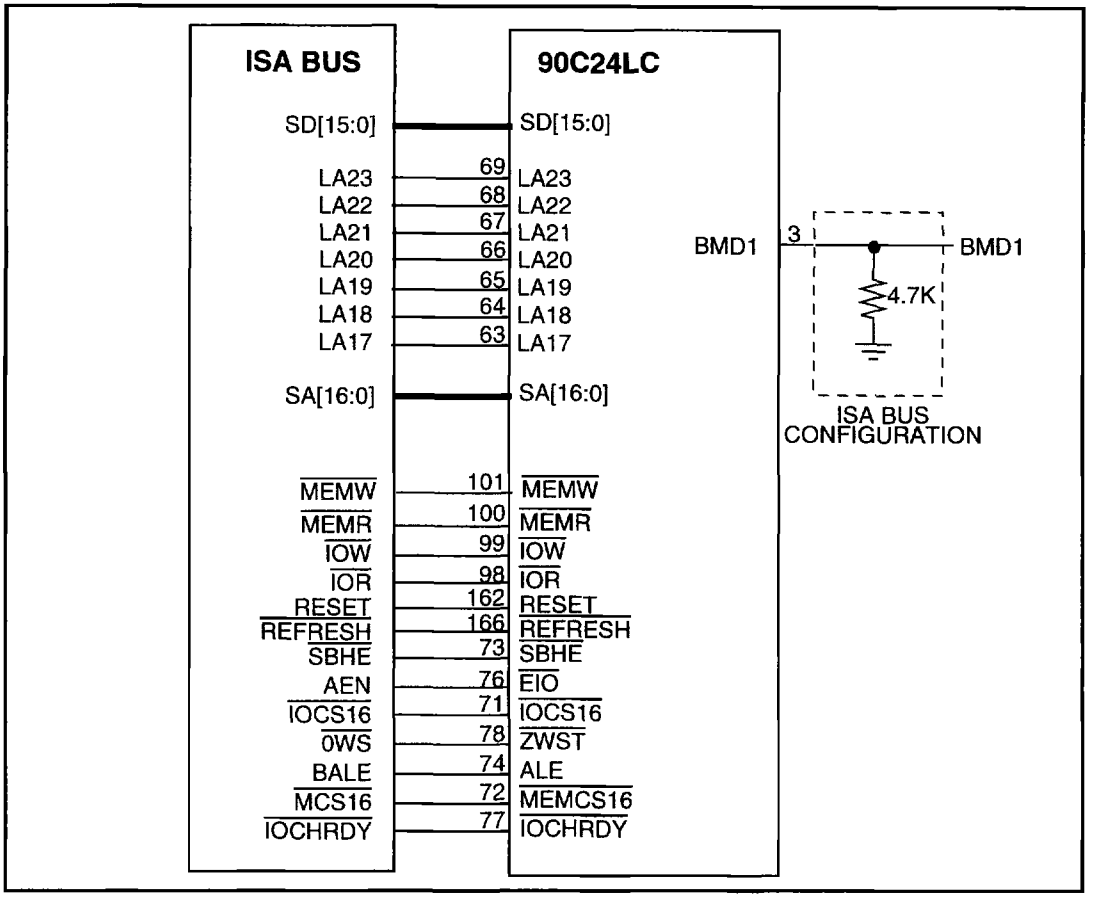

FIGURE 3-1. ISA BUS INTERFACE DIAGRAM

3.6 VESA VL-BUS INTERFACE

The 90C24LC directly supports the following VESA VL-Bus interface signals (see Figure 3-3).

ADR[31:2]	$\overline{\text{LDEV}}$
$\overline{\text{ADS}}$	$\overline{\text{LRDY}}$
$\overline{\text{BE}}$[3:0]	M/$\overline{\text{IO}}$
DAT[31:0]	RESET
D/$\overline{\text{C}}$	$\overline{\text{RDYRTN}}$
LCLK	W/$\overline{\text{R}}$

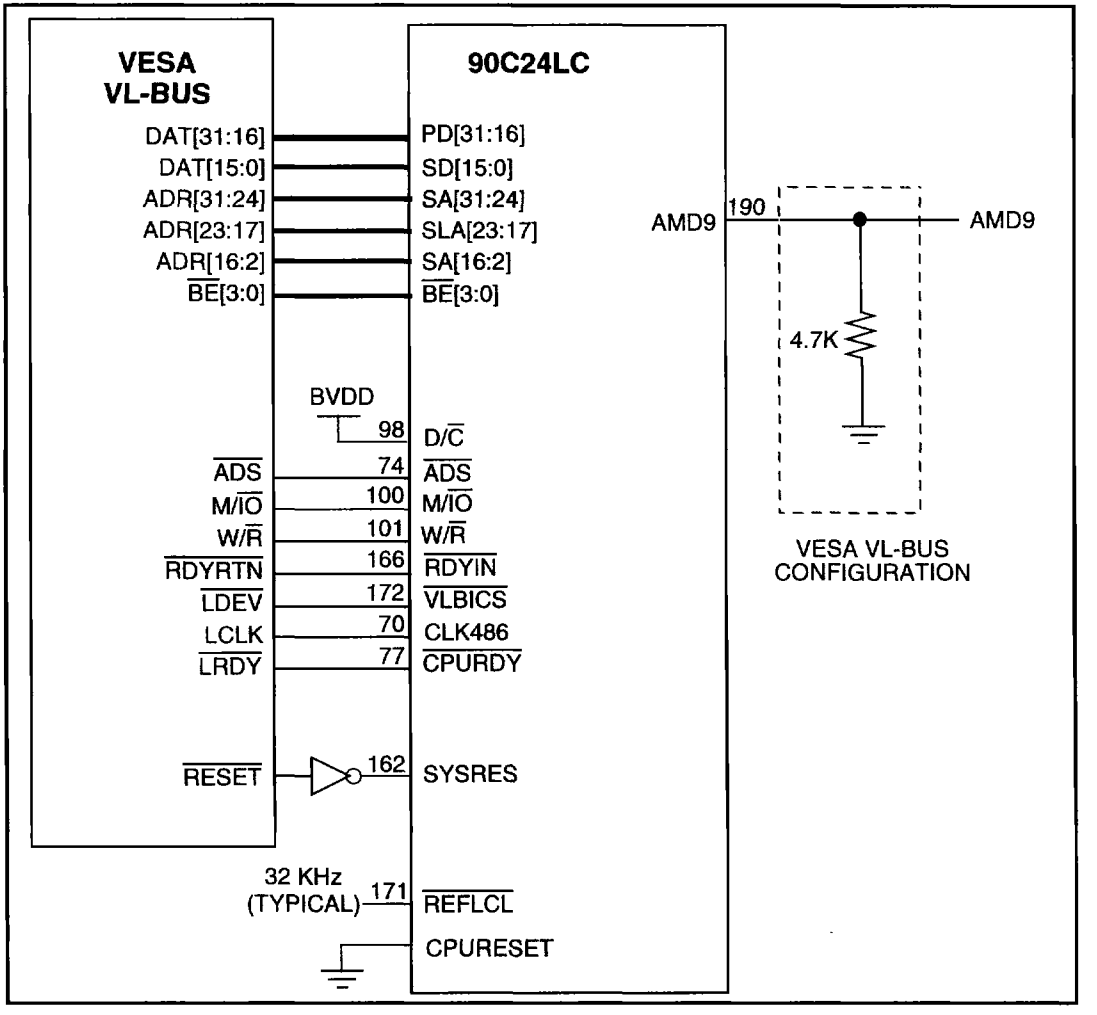

FIGURE 3-2. VESA VL-BUS INTERFACE DIAGRAM

3.7 CRT DISPLAY INTERFACE

- On-chip RAMDAC provides the RED, GREEN, and BLUE signals directly to the analog CRT monitor
- Provides HSYNC and VSYNC signals to control the monitor
- Allows use of an external RAMDAC to drive the CRT
- Supports Bt/471/478/476 compatible RAMDAC interface

3.8 FLAT PANEL DISPLAY INTERFACE

Features of the flat panel display interface include:

- Direct interface with 640 by 480 (400) STN, TFT, 1024 by 768 LCD, EL, and plasma panels
- Flat panel interface signals change function to support the panel type chosen
- Programmable timing and polarity for the flat panel control signals to meet the requirements of different panels
- Video data groupings to meet the requirements for different panels
- Controller supplies 8 pixels per shift clock with 8-bits of data for monochrome STN panels
- Controller supplies one pixel per shift clock with 4-bits of data for 16 shades for plasma panels
- Controller supplies 8-bit (2 and 2/3 pixel per shift clock) interface, and 16-bit (5 and 1/3 pixel per shift clock) interface for color STN panels
- Controller supplies 9-bit, 12-bit 18-bit (all are one pixel per shift clock) interface for TFT panels

4.0 MEMORY CONFIGURATIONS

4.1 MEMORY MODE SETUP

The following table defines how to set up the configuration registers for the desired memory mode. Refer to subsequent paragraphs for descriptions of the memory modes

The memory modes listed in Table 4-1 are selected at power-on or reset depending upon configuration bits CNF16, CNF14, and CNF13. For information about the configuration registers, refer to Section 24.

MODE	MEMORY DRAMS TYPE	MEMORY DRAMS QTY	CNF16 PR11[7]	CNF14 PR11[6]	CNF13 PR11[5]
1	256K by 16	1	1	0	1
2[3]	256K by 16	2	1	0	0

NOTES:
1. With CNF[16] set to 0, display memory uses 256K by 16 DRAMs.
2. CNF(16), CNF(14), and CNF(13) are readable via PR 11 bits 7, 6, and 5, respectively (refer to Section 24).
3. Mode 2 has no frame buffer.

TABLE 4-1. MEMORY MODE SETUP

In memory mode 1 the display memory data path is 16 bits wide.

Memory mode 2 is used with a 32-bit wide display memory data path, unless one of the DRAM banks is used as the LCD panel frame buffer. For example, one DRAM bank is used as the LCD panel frame buffer when simultaneous display with an LCD panel and CRT is used, and also when 16-bit dual-panel color STN is used.

4.2 MEMORY CONFIGURATION DESCRIPTIONS

Memory for the 90C24LC can be configured in two memory modes as listed in Table 4-1. Table 4-2 summarizes how the memory modes support combinations of memory configurations and displays. The following block diagrams are provided show how the external DRAMs are connected in typical memory configurations.

1. Single DRAM Memory Interface Configuration
2. Memory Configuration with 1 Mbyte.
3. Simultaneous Display Memory Configuration
4. High-Performance 512 Kbyte Simultaneous Display Memory Configuration

Table 4-2 lists the memory modes and which of the memory modes supports each display resolution. Where the memory mode is available, the table lists whether it supports CRT only, LCD only, or simultaneous displays (dual panel and CRT).

MEMORY CONFIGURATIONS	MEMORY MODES[1] 1[2]	2[3]
1024 x 768 x 256	---	C,L
1024 x 768 x 16	C,L	C,L
800 x 600 x 256	C	C
800 x 600 x 16	C,L	C,L
640 x 480 x 256	C,L	S,C,L
640 x 480 x 32K/64K	---	C,L
640 x 400 x 256	C,L	S,C,L
640 x 400 x 32K/64K	C,L	C,L
320 x 200 x 32K/64K	C,L	C,L
All IBM Standard Modes	S,C,L	S,C,L
Memory Data Bus Width	16 bits	32 bits

NOTES

S = Simultaneous display (dual panel and CRT)
C = CRT only
L = LCD only

1. These memory modes are also listed in Table 4-1.
2. Supports a 16-bit interface in C and L modes.
3. Supports a 32-bit interface in C and L modes.

TABLE 4-2. MEMORY CONFIGURATIONS AND MODES SUPPORTED

4.3 MEMORY MODE 1 INTERFACE CONFIGURATION

Figure 4-1 shows memory mode No. 1 with 512 Kbytes of display memory using one 256K by 16 DRAM.

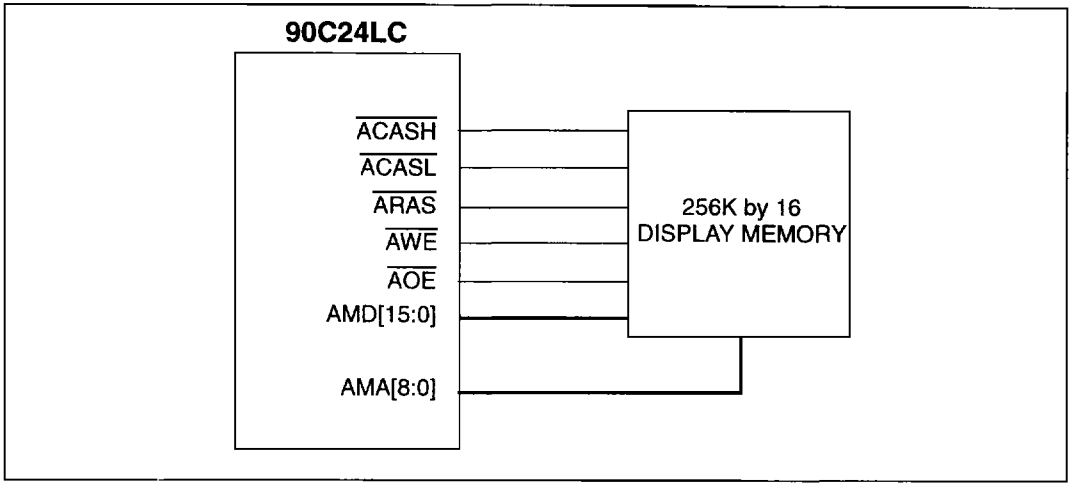

FIGURE 4-1. MEMORY MODE 1 INTERFACE CONFIGURATION

4.4 MEMORY MODE 2 INTERFACE CONFIGURATION

Figure 4-2 shows memory mode No. 2 with 1 Mbyte of display memory using two 256K by 16 DRAMs.

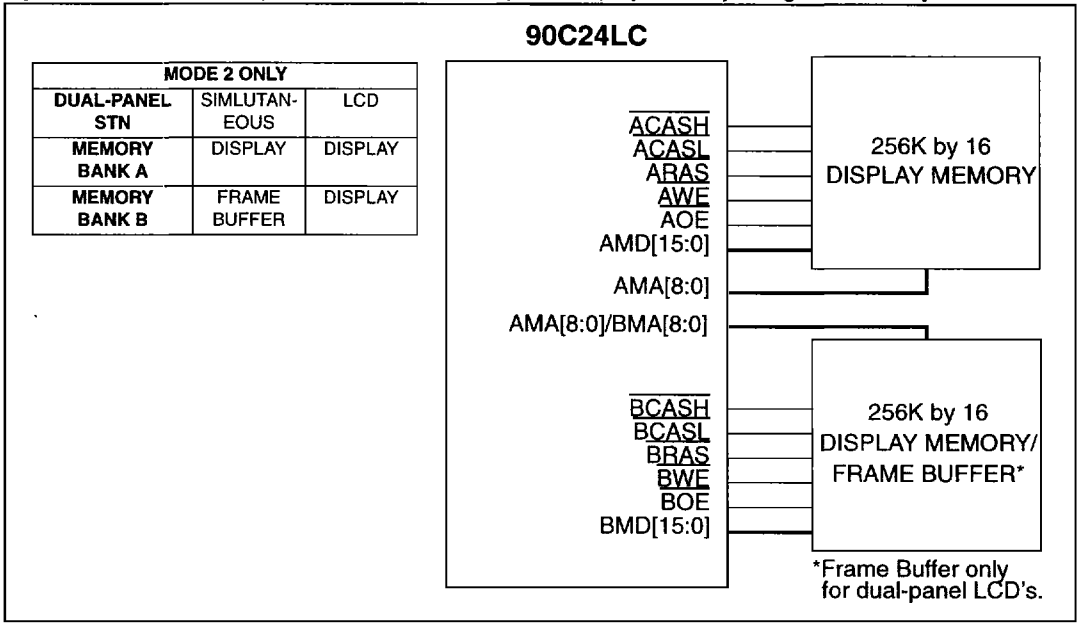

FIGURE 4-2. MEMORY MODE 2 INTERFACE CONFIGURATION USING TWO 256K BY 16 DRAMS

Figure 4-3 shows memory mode No. 2 with 1 Mbyte of display memory using eight 256K by 4 DRAMs.

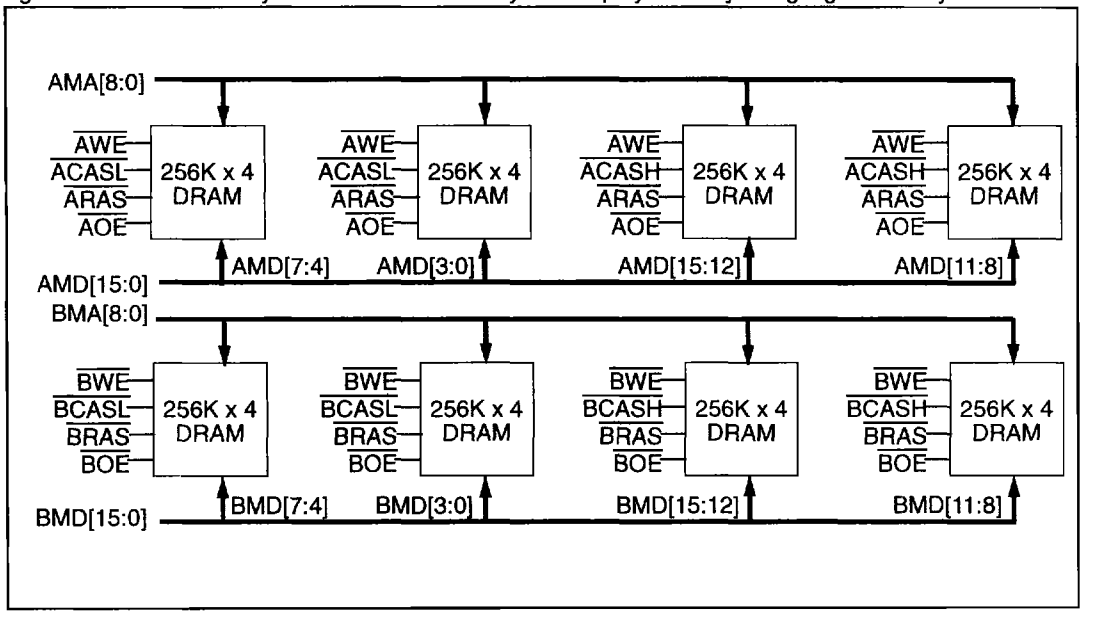

FIGURE 4-3. MEMORY MODE 2 INTERFACE CONFIGURATION USING EIGHT 256K BY 4 DRAMS

5.0 SIGNAL DESCRIPTIONS

5.1 INTRODUCTION

This section contains detailed information concerning signals and connector pins for the 90C24LC controller 208-pin MQFP package. The following information is contained in this section:

- Signal to Pin Location Table
- Signal and Pin Configuration Diagram
- Detailed Signal Descriptions
- Pin Multiplexing Reference Tables

NOTES FOR TABLE 5-1

Where multiple signal names are assigned to a pin, the names are separated by a vertical bar (|). The use for each pin depends on the bus that the pin is connected to. For additional information about the busses refer to Section 5-3. For additional information about pins with multiplexed signals, refer to Section 5.4.

[1] Indicates output only signal names.

[2] Indicates input only signal names.

[3] Indicates VDD and VSS supply pins.

Signal names not otherwise indicated are both input and output.

5.2 SIGNAL MNEMONIC TO PIN LOCATION

PIN - NAME	PIN - NAME	PIN - NAME	PIN - NAME
1 - BMD0	32 - BMA2[1]	63 - SLA17[2]	94 - SA13[2]
2 - BMD15	33 - BMA5[1]	64 - SLA18[2]	95 - SA14[2]
3 - BMD1	34 - BMA3[1]	65 - SLA19[2]	96 - SA15[2]
4 - BMD14	35 - BMA4[1]	66 - SLA20[2]	97 - SA16[2]
5 - VSS[3]	36 - VSS[3]	67 - SLA21[2]	98 - $\overline{IOR}$[2]ID/$\overline{C}$[2]
6 - BMD2	37 - PD29	68 - SLA22[2]	99 - $\overline{IOW}$[2]I$\overline{BE1}$[2]
7 - BMD13	38 - PD28	69 - SLA23[2]	100 - $\overline{MEMR}$[2]IM/$\overline{IO}$[2]
8 - BMD3	39 - PD27	70 - CLK486[2]	101 - $\overline{MEMW}$[2]IW/$\overline{R}$[2]
9 - BMD12	40 - PD26	71 - $\overline{IOCS16}$[1]I$\overline{BOFF}$[1]	102 - AVDD1[3]
10 - VDD[3]	41 - PD25	72 - $\overline{MEMCS16}$[1]IPD31	103 - XMCLK[2]
11 - BMD4	42 - PD24	73 - $\overline{SBHE}$[2]I CPURESET[2]	104 - MCAP[2]
12 - BMD11	43 - VDD[3]	74 - ALE[2]I$\overline{ADS}$[2]	105 - VCAP[2]
13 - BMD5	44 - PD23	75 - IRQ[1]IPD30	106 - VCLK2
14 - BMD10	45 - PD22	76 - $\overline{EIO}$[2]I$\overline{BE0}$[2]	107 - AVSS1[3]
15 - BMD6	46 - PD21	77 - $\overline{IOCHRDY}$[1]I $\overline{CPURDY}$[1]	108 - RVSS[3]
16 - BMD9	47 - PD20	78 - $\overline{ZWST}$[1]IVLBIBUSY	109 - SD0
17 - BMD7	48 - VSS[3]	79 - VSS[3]	110 - SD1
18 - BMD8	49 - PD19	80 - SA0[2]I$\overline{BE3}$[2]	111 - SD2
19 - MVDD[3]	50 - PD18	81 - SA1[2]I$\overline{BE2}$[2]	112 - SD3
20 - $\overline{BCASL}$[1]	51 - PD17	82 - SA2[2]	113 - BVDD[3]
21 - VSS[3]	52 - PD16	83 - SA3[2]	114 - SD4
22 - $\overline{BWE}$[1]	53 - SD15	84 - SA4[2]	115 - SD5
23 - $\overline{BCASH}$[1]	54 - SD14	85 - SA5[2]	116 - SD6
24 - $\overline{BRAS}$[1]	55 - SD13	86 - SA6[2]	117 - SD7
25 - $\overline{BOE}$[1]	56 - SD12	87 - SA7[2]	118 - VSS[3]
26 - VDD[3]	57 - BVDD[3]	88 - RVDD[3]	119 - XSCLK[1]IXSCLKL[1]I XSCLKU[1]IBD5[1]
27 - BMA8	58 - SD11	89 - SA8[2]	120 - $\overline{WPLT}$[1]IBD4[1]
28 - BMA0[1]	59 - SD10	90 - SA9[2]	121 - $\overline{RPLT}$[1]IBD3[1]I STN15[1] IUD7[1]
29 - BMA7[1]	60 - SD9	91 - SA10[2]	122 - STN14[1]IBD2[1]I UD6[1]
30 - BMA1[1]	61 - SD8	92 - SA11[2]	123 - STN13[1]IBD1[1]I IUD5[1]
31 - BMA6[1]	62 - VSS[3]	93 - SA12[2]	124 - STN12[1]IBD0[1]I IUD4[1]

NOTE: Refer to notes preceding this table.

TABLE 5-1. SIGNAL TO PIN LOCATION

PIN - NAME	PIN - NAME	PIN - NAME	PIN - NAME
125 - VDD[3]	146 - SA24[2]	167 - FPUSR0[1]	188 - AMD10
126 - STN11[1]|GD5[1]|UD3[1]	147 - SA25[2]	168 - VCLK1[1]| FPUSR1[1]	189 - AMD6
127 - STN10[1]|GD4[1]|UD2[1]	148 - SA26[2]	169 - PVDD[3]	190 - AMD9
128 - STN9[1]|RD5[1]|UD1[1]	149 - SA27[2]	170 - CKIN[2]|VCLK[2]	191 - AMD7
129 - STN8[1]|RD4[1]|UD0[1]	150 - SA28[2]	171 - $\overline{\text{EBROM}}$[1]| $\overline{\text{REFLCL}}$[2]	192 - AMD8
130 - FPVDD[3]	151 - SA29[2]	172 - $\overline{\text{VLBICS}}$[1]	193 - MVDD[3]
131 - VUD3[1]|D7[1]|RD3[1]|STN7[1]| STN0[1]|LD7[1]|VD7|P7[2]	152 - SA30[2]	173 - VSYNC[1]	194 - $\overline{\text{ACASL}}$[1]
132 - VUD2[1]|D6[1]|RD2[1]|STN6[1]| STN1[1]|LD6[1]|VD6|P6[2]	153 - SA31[2]	174 - HSYNC[1]	195 - VSS[3]
133 - VUD1[1]|D5[1]|RD1[1]|STN5[1]| STN2[1]|LD5[1]|VD5|P5[2]	154 - AVDD2[3]	175 - PCLK	196 - $\overline{\text{AWE}}$[1]
134 - VUD0[1]|D4[1]|RD0[1]| STN4[1]| STN3[1]|LD4[1]| VD4|P4[2]	155 - $\overline{\text{MDETECT}}$[2]|FSADJ[2]	176 - VSS[3]	197 - $\overline{\text{ACASH}}$[1]
135 - VLD3[1]|D3[1]|GD3[1]| STN3[1]| STN4[1]|LD3[1]| VD3|P3[2]	156 - VREF[2] (Analog)	177 - AMD0	198 - $\overline{\text{ARAS}}$[1]
136 - VLD2[1]|D2[1]|GD2[1]| STN2[1]| STN5[1]|LD2[1]| VD2|P2[2]	157 - BLUE[1] (Analog)	178 - AMD15	199 - $\overline{\text{AOE}}$[1]
137 - VLD1[1]|D1[1]|GD1[1]|STN1[1]| STN6[1]|LD1[1]| VD1|P1[2]	158 - GREEN[1] (Analog)	179 - AMD1	200 - AMA8[1]
138 - VLD0[1]| D0[1]|GD0[1]| STN0[1]| STN7[1]|LD0[1]| VD0|P0[2]	159 - RED[1] (Analog)	180 - AMD14	201 - AMA0[1]
139 - VSS[3]	160 - AVSS2[3]	181 - AMD2	202 - AMA7[1]
140 - XSCLK[1]|XSCLKL[1]| XSCLKU[1]	161 - EXCKEN[2]	182 - AMD13	203 - AMA1[1]
141 - RVDD[3]	162 - RESET[2]|SYSRES[2]	183 - AMD3	204 - AMA6[1]
142 - LP[1]	163 - $\overline{\text{PDOWN}}$[2]	184 - AMD12	205 - AMA2[1]
143 - FP[1]	164 - $\overline{\text{LCDENA}}$[1]	185 - AMD4	206 - AMA5[1]
144 - FR[1]|$\overline{\text{BLANK}}$[1]| ENDATA[1]	165 - PNLOFF[1]	186 - AMD11	207 - AMA3[1]
145 - RVSS[3]	166 - $\overline{\text{REFRESH}}$[2]| $\overline{\text{RDYIN}}$[2]	187 - AMD5	208 - AMA4[1]

NOTE: Refer to notes preceding this table.

TABLE 5-1 SIGNAL TO PIN LOCATIONS (Continued)

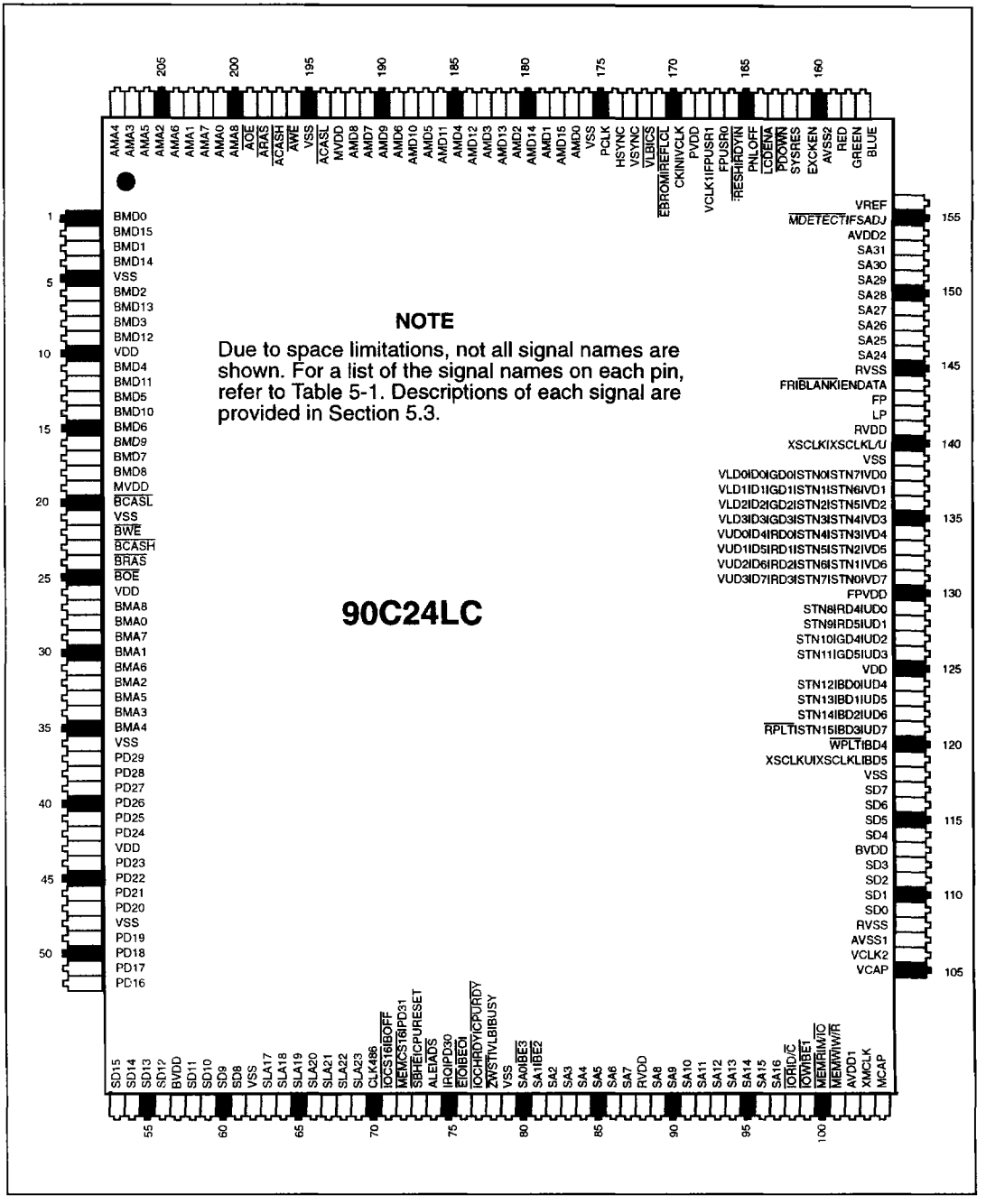

FIGURE 5-1. PIN CONFIGURATION