SSI 78P304A

Low-Power T1/E1 Integrated Short Haul Transceiver with Receive Jitter Attenuation

December 1993

DESCRIPTION

The SSI 78P304A is a fully integrated low-power transceiver for both North American 1.544 MHz (T1), and European 2.048 MHz (E1/CEPT) applications. It features a constant low output impedance transmitter allowing for high transmitter return loss in E1 applications. Transmit pulse shapes (DSX-1 or E1/CEPT) are selectable for various line lengths and cable types.

The SSI 78P304A provides receive jitter attenuation starting at 3 Hz, and is microprocessor controllable through a serial interface.

The SSI 78P304A offers a variety of diagnostic features including transmit and receive monitoring. The device incorporates an on-chip crystal oscillator, and also accepts digital clock inputs. It uses an advanced double-poly, double-metal CMOS process and requires only a single 5-volt power supply.

APPLICATIONS

- PCM / Voice Channel Banks
- Data Channel Bank / Concentrator
- T1 / E1 multiplexer
- Digital Access and Cross-connect Systems (DACS)
- Computer to PBX interface (CPI & DMI)
- High speed data transmission lines
- Interfacing Customer Premises Equipment to a CSU
- Digital Loop Carrier (DLC) terminals

FEATURES

- **Low power consumption (400 mW maximum) 40% less than the SSI 78P300**
- **Constant low output impedance transmitter regardless of data pattern**
- **High transmit and receive return loss**
- **Meets or exceeds all industry specifications including CCITT G.703, ANSI T1.403 and ATT Pub 62411**
- **Compatible with most popular PCM framers including the 2180A (T1) and 2181/2181A (E1)**
- **Line driver, data recovery and clock recovery functions**
- **Minimum receive signal of 500 mV**
- **Selectable slicer levels (CEPT/DSX-1) improve SNR**
- **Programmable transmit equalizer shapes pulses to meet DSX-1 pulse template from 0 to 655 ft**
- **Local and remote loopback functions Transmit / Receive performance monitors with DPM and LOS outputs**
- **Receiver jitter tolerance 0.4 UI from 40 kHz to 100 kHz**
- **Receive jitter attenuation starting at 6 Hz**
- **Microprocessor controllable**
- **Available in 28 pin DIP or PLCC**

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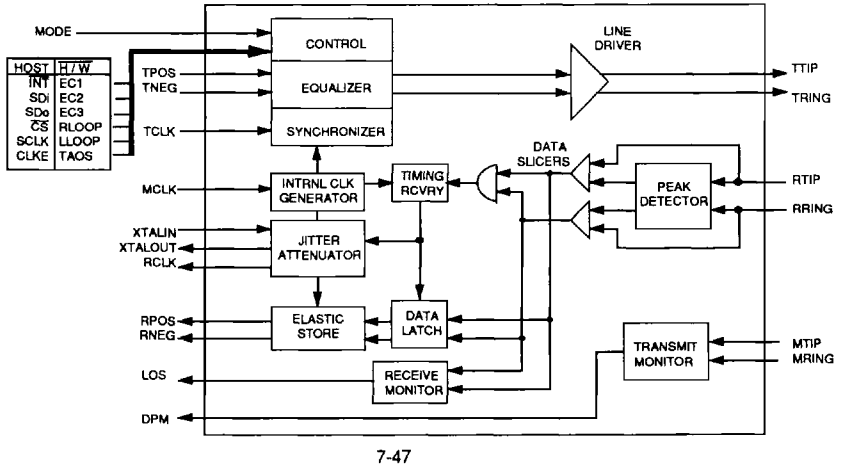
FIGURE 1: BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The SSI 78P304A is a fully integrated PCM transceiver for both 1.544 MHz (DSX-1) and 2.048 MHz (E1) applications. It allows transmission of digital data over existing twisted-pair installations. The SSI 78P304A transceiver interfaces with two twisted-pair lines, one twisted-pair for transmit, one twisted-pair for receive.

TRANSMITTER

Data received for transmission onto the line is clocked serially into the device at TPOS and TNEG. Input synchronization is supplied by the transmit clock (TCLK). The transmitted pulse shape is determined by Equalizer Control signals EC1 through EC3 as shown in Table 1. Refer to Table 2 and Figure 2 for master and transmit clock timing characteristics. Shaped pulses are applied to the AMI line driver for transmission onto the line at TTIP and TRING. Equalizer Control signals may be hardwired in the Hardware mode, or input as part of the serial data stream (SDI) in the Host mode.

Pulses can be shaped for either 1.544 or 2.048 MHz applications. 1.544 MHz pulses for DSX-1 applications can be programmed to match line lengths from 0 to 655 feet of ABAM cable. The SSI 78P304A also matches FCC and ECSA specifications for CSU applications. A 1:1.15 transmit transformer is used for all 1.544 MHz systems.

2.048 MHz pulses can drive coaxial or shielded twisted-pair lines. For E1 systems, a 1:2 transmit transformer and series resistors are recommended. This design meets or exceeds all CCITT and European PTT specifications for transmit and receive return loss. A 1:1 or 1:1.26 transformer may be used without series resistors.

DRIVER PERFORMANCE MONITOR

The transceiver incorporates a Driver Performance Monitor (DPM) in parallel with TTIP and TRING at the output transformer. The DPM output goes high upon detection of 63 consecutive zeros. It is reset when a one is detected on the transmit line, or when a reset command is received.

LINE CODE

The SSI 78P304A transmits data as a 50% AMI line code as shown in Figure 3. The output driver maintains a constant low output impedance regardless of whether it is driving marks or spaces.

RECEIVER

The SSI 78P304A receives the signal input from one twisted-pair line on each side of a center-grounded transformer. Positive pulses are received at RTIP and negative pulses are received at RRING. Recovered data is output at RPOS and RNEG, and the recovered clock is output at RCLK. Refer to Table 3 and Figure 4 for SSI 78P304A receiver timing.

The signal received at RPOS and RNEG is processed through the peak detector and data slicers. The peak detector samples the inputs and determines the maximum value of the received signal. A percentage of the peak value is provided to the data slicers as a threshold level to ensure optimum signal-to-noise ratio. For DSX-1 applications (determined by Equalizer Control inputs EC1 - EC3 $\neq$ 000) the threshold is set to 70% of the peak value. This threshold is maintained above 65% for up to 15 successive zeros over the range of specified operating conditions. For E1 applications (EC inputs = 000 or 001) the threshold is 50%.

The receiver is capable of accurately recovering signals with up to -13.6 dB of attenuation (from 2.4V), corresponding to a received signal level of approximately 500 mV. Maximum line length is 1500 feet of ABAM cable (approximately 6 dB of attenuation). Regardless of received signal level, the peak detectors are held above a minimum level of .3V to provide immunity from impulsive noise.

After processing through the data slicers, the received signal is routed to the data and clock recovery sections, and to the receive monitor. The receive monitor generates a Loss of Signal (LOS) output upon receipt of 175 consecutive zeros (spaces). The receiver monitor loads a digital counter at the RCLK frequency. The count is incremented each time a zero is received, and reset to zero each time a one (mark) is received. Upon receipt of 175 consecutive zeros the LOS pin goes high, and a smooth transition replaces the RCLK output with the MCLK. (If MCLK is not supplied the RCLK output will be replaced with the centered crystal clock.) The LOS pin is reset immediately upon receipt of a one.

Recovered clock signals are supplied to the jitter attenuator and the data latch. The recovered data is passed to the elastic store where it is buffered and synchronized with the dejittered recovered clock (RCLK).

JITTER ATTENUATION

Jitter attenuation of the SSI 78P304A clock and data outputs is provided by a Jitter Attenuation Loop (JAL) and an Elastic Store (ES). An external crystal oscillating at 4 times the bit rate provides clock stabilization. Refer to Table 4 for crystal specifications. The ES is a 32 x 2-bit register. Recovered data is clocked into the ES with the recovered clock signal, and clocked out of the ES with the dejittered clock from the JAL. When the bit count in the ES is within two bits of overflowing or underflowing, the ES adjusts the output clock by 1/8 of a bit period. The ES produces an average delay of 16 bits in the receive path.

OPERATING MODES

The SSI 78P304A transceiver can be controlled through hard-wired pins (Hardware mode) or by a microprocessor through a serial interface (Host mode). The mode of operation is set by the MODE pin logic level. The SSI 78P304A can also be commanded to operate in one of several diagnostic modes.

HOST MODE OPERATION

To allow a host microprocessor to access and control the SSI 78P304A through the serial interface, MODE is set to 1. The serial interface (SDI/SDO) uses a 16-bit word consisting of an 8-bit Command/Address byte and an 8-bit Data byte. Figure 5 shows the serial interface data structure and timing.

The Host mode provides a latched Interrupt output ($\overline{INT}$) which is triggered by a change in the Loss of Signal (LOS) and/or Driver Performance Monitor (DPM) bits. The Interrupt is cleared when the interrupt condition no longer exists, and the host processor enables the respective bit in the serial input data byte. Host mode also allows control of the serial data and receive data output timing. The Clock Edge (CLKE) signal determines when these outputs are valid, relative to the Serial Clock (SCLK) or RCLK as follows:

CLKE	Output	Clock	Valid Edge
LOW	RPOS	RCLK	Rising
	RNEG	RCLK	Rising
	SDO	SCLK	Falling
HIGH	RPOS	RCLK	Falling
	RNEG	RCLK	Falling
	SDO	SCLK	Rising

The SSI 78P304A serial port is addressed by setting bit A4 in the Address/Command byte, corresponding to address 16. The SSI 78P304A contains only a single output data register so no complex chip addressing scheme is required. The register is accessed by causing the Chip Select (CS) input to make a transition from high to low. Bit 1 of the serial Address/Command byte provides Read/Write control when the chip is accessed. A logic 1 indicates a read operation, and a logic 0 indicates a write operation. Table 6 lists serial data output bit combinations for each status. Serial data I/O timing characteristics are shown in Table 6, and Figures 6 and 7.

HARDWARE MODE OPERATION

In Hardware mode the transceiver is accessed and controlled through individual pins. With the exception of the $\overline{INT}$ and CLKE functions, Hardware mode provides all the functions provided in the Host mode. In the Hardware mode RPOS and RNEG outputs are valid on the rising edge of RCLK. To operate in Hardware mode, MODE must be set to 0. Equalizer Control signals (EC1 through EC3) are input on the Interrupt, Serial Data In and Serial Data Out pins. Diagnostic control for Remote Loopback (RLOOP), Local Loopback (LLOOP), and Transmit All Ones (TAOS) modes is provided through the individual pins used to control serial interface timing in the Host mode.

RESET OPERATION

Upon power up, the transceiver is held static until the power supply reaches approximately 3V. Upon crossing this threshold, the device begins a 32 ms reset cycle to calibrate the transmit and receive delay lines and lock the Phase Lock Loop to the receive line. A reference clock is required to calibrate the delay lines. The transmitter reference is provided by TCLK. The crystal oscillator provides the receiver reference. If the 78P304A crystal oscillator is grounded, MCLK is used as the receiver reference clock.

The transceiver can also be reset from the Host or Hardware mode. In Host mode, reset is commanded by simultaneously writing RLOOP and LLOOP to the register. In Hardware mode, reset is commanded by holding RLOOP and LLOOP high simultaneously for 200 ns. Reset is initiated on the falling edge of the reset request. In either mode, reset clears and sets all registers to 0 and centers the oscillator, then calibration begins.

DIAGNOSTIC MODE OPERATION

In Transmit All Ones (TAOS) mode the TPOS and TNEG inputs to the transceiver are ignored. The transceiver transmits a continuous stream of 1's when the TAOS mode is activated. TAOS can be commanded simultaneously with Local Loopback, but is inhibited during Remote Loopback.

In Remote Loopback (RLOOP) mode, the transmit data and clock inputs (TPOS, TNEG and TCLK) are ignored. The RPOS and RNEG outputs are looped back through the transmit circuits and output on TTIP and TRING at the RCLK frequency. Receiver circuits are unaffected by the RLOOP command and continue to output the RPOS, RNEG and RCLK signals received from the twisted-pair line.

In Local Loopback (LLOOP) mode, the receiver circuits are inhibited. The transmit data and clock inputs (TPOS, TNEG and TCLK) are looped back onto the receive data and clock outputs (RPOS, RNEG and RCLK.) The transmitter circuits are unaffected by the LLOOP command. The TPOS and TNEG inputs (or a stream of 1's if the TAOS command is active) will be transmitted normally. When used in this mode with a crystal, the transceiver can be used as a stand-alone jitter attenuator.

POWER REQUIREMENTS

The SSI 78P304A is a low-power CMOS device. It operates from a single +5 V power supply which can be connected externally to both the transmitter and receiver. However, the two inputs must be within ± .3V of each other, and decoupled to their respective grounds separately, as shown in Figure 8. Isolation between the transmit and receive circuits is provided internally.

PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
MCLK	I	Master Clock: A 1.544 or 2.048 MHz clock input used to generate internal clocks. Upon Loss of Signal (LOS), RCLK is derived from MCLK. If MCLK is not applied, this pin should be grounded.
TCLK	I	Transmit Clock: Transmit clock input. TPOS and TNEG are sampled on the falling edge of TCLK.
TPOS	I	Transmit Positive Data: Input for positive pulse to be transmitted on the twisted-pair or coaxial cable.
TNEG	I	Transmit Negative Data: Input for negative pulse to be transmitted on the twisted-pair or coaxial cable.
MODE	I	Mode Select: Setting MODE to logic 1 puts the SSI 78P304A in the Host mode. In the Host mode, the serial interface is used to control the SSI 78Q904A and determine its status. Setting MODE to logic 0 puts the SSI 78P304A in the Hardware (H/W) mode. In the Hardware mode the serial interface is disabled and hard-wired pins are used to control configuration and report status.
RNEG / RPOS	O	Receive Negative/Positive Data: Received data outputs. A signal on RNEG corresponds to receipt of a negative pulse on RTIP and RRING. A signal on RPOS corresponds to receipt of a positive pulse on RTIP and RRING. RNEG and RPOS outputs are Non-Return-to-Zero (NRZ). In the Host mode, CLKE determines the clock edge at which these outputs are stable and valid. In the Hardware mode both outputs are stable and valid on the rising edge of RCLK.
RCLK	O	Recovered Clock: This is the clock recovered from the signal received at RTIP and RRING.

PIN DESCRIPTION (continued)

NAME	TYPE	DESCRIPTION
XTALIN / XTALOUT	I	Crystal Input / Crystal Output: An external crystal operating at four times the bit rate (6.176 MHz for DSX-1, 8.192 MHz for E1 applications with an 18.7 pF load) is required to enable the jitter attenuation function of the SSI 78P304A. These pins may also be used to disable the jitter attenuator by connecting the XTALIN pin to the positive supply through a resistor, and tying the XTALOUT pin to ground.
DPM	O	Driver Performance Monitor: DPM goes to a logic 1 when the transmit monitor loop (MTIP and MRING) does not detect a signal for 63 ±2 clock periods. DPM remains at logic 1 until a signal is detected.
LOS	O	Loss of Signal: LOS goes to a logic 1 when 175 consecutive spaces have been detected. LOS returns to a logic 0 when a mark is received.
TTIP / TTRING	O	Transmit Tip / Transmit Ring: Differential Driver Outputs. These low impedance outputs achieve maximum power savings through a 1:1.15 transformer (T1), or a 1:1 or 1:1.26 transformer (E1) without additional components. To provide higher return loss for E1 systems, resistors may be used in series with a 1:2 transformer (use 15Ω resistors for 120Ω terminations, and 9.3Ω resistors for 75Ω terminations.)
TGND	-	Transmit Ground: Ground return for the transmit drivers power supply TV+.
TV+	I	Transmit Power Supply: +5 VDC power supply input for the transmit drivers. TV+ must not vary from RV+ by more than ±0.3V.
MTIP / MRING	I	Monitor Tip / Monitor RIng: These pins are used to monitor the tip and ring transmit outputs. The transceiver can be connected to monitor its own output or the output of another 78P304A on the board. To prevent false interrupts in the host mode if the monitor is not used, apply a clock signal to one of the monitor pins and tie the other monitor pin to approximately the clock's mid-level voltage. The monitor clock can range from 100kHz to the TCLK frequency.
RTIP / RRING	O	Receive Tip / Receive Ring: The AMI signal received from the line is applied at these pins. A center-tapped, center-grounded, 2:1 step-up transformer is required on these pins. Data and clock from the signal applied at these pins are recovered and output on the RPOS/RNEG, and RCLK pins.
RV+	I	Received Power Supply: +5 VDC power supply for all circuits except the transmit drivers. (Transmit drivers are supplied by TV+.)
RGND	-	Receive Ground: Ground return for power supply RV+.
$\overline{INT}$	O	Interrupt (Host Mode): This SSI 78P304A Host mode output goes low to flag the host processor when LOS or DPM go active. $\overline{INT}$ is an open-drain output and should be tied to power supply RV+ through a resistor. $\overline{INT}$ is reset by clearing the respective register bit (LOS and/or DPM.)
EC1	I	Equalizer Control 1 (H/W Mode): The signal applied at this pin in the SSI 78P304A Hardware mode is used in conjunction with EC2 and EC3 inputs to determine shape and amplitude of AMI output transmit pulses.

PIN DESCRIPTION (continued)

NAME	TYPE	DESCRIPTION
SDI	I	Serial Data In (Host Mode): The serial data input stream is applied to this pin when the SSI 78P304A operates in the Host mode. SDI is sampled on the rising edge of SCLK.
EC2	I	Equalizer Control 2 (H/W Mode): The signal applied at this pin in the SSI 78P304A Hardware mode is used in conjunction with EC1 and EC3 inputs to determine shape and amplitude of AMI output transmit pulses.
SDO	O	Serial Data Out (Host Mode): The serial data from the on-chip register is output on this pin in the SSI 78P304A Host mode. If CLKE is high, SDO is valid on the rising edge of SCLK. If CLKE is low SDO is valid on the falling edge of SCLK. This pin goes to a high-impedance state when the serial port is being written to and when $\overline{CS}$ is high.
EC3	I	Equalizer Control 3 (H/W Mode): The signal applied at this pin in the SSI 78P304A Hardware mode is used in conjunction with EC1 and EC2 inputs to determine shape and amplitude of AMI output transmit pulses.
$\overline{CS}$	I	Chip Select (Host Mode): This input is used to access the serial interface in the SSI 78P304A Host mode. For each read or write operation, $\overline{CS}$ must remain low for the duration of operation.
RLOOP	I	Remote Loopback (H/W Mode): This input controls loopback functions in the SSI 78P304A Hardware mode. Setting RLOOP to a logic 1 enables the Remote Loopback mode. Setting both RLOOP and LLOOP causes a Reset.
SCLK	I	Serial Clock (Host Mode): This clock is used in the SSI 78P304A Host mode to write data to or read data from the serial interface registers.
LLOOP	I	Local Loopback (H/W Mode): This input controls loopback functions in the SSI 78P304A Hardware mode. Setting LLOOP to a logic 1 enables the Local Loopback Mode.
CLKE	I	Clock Edge (Host Mode): Setting CLKE to logic 1 causes RPOS and RNEG to be valid on the falling edge of RCLK, and SDO to be valid on the rising edge of SCLK. When CLKE is a logic 0, RPOS and RNEG are valid on the rising edge of RCLK, and SDO is valid on the falling edge of SCLK.
TAOS	I	Transmit All Ones (H/W Mode): When set to a logic 1, TAOS causes the SSI 78P304A (Hardware mode) to transmit a continuous stream of marks at the TCLK frequency. Activating TAOS causes TPOS and TNEG inputs to be ignored. TAOS is inhibited during Remote Loopback.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation above maximum ratings may damage the device. Normal operation not guaranteed at these extremes.

PARAMETER		RATING	UNIT
DC supply (referenced to GND)	RV+, TV+	-0 to 6.0	V
Input voltage, any pin (see note 1)	V_{IN}	RGND -0.3 to RV+ + 0.3	V
Input current, any pin (see note 2)	I_{IN}	-10 to +10	mA
Ambient operating temperature	T_A	-40 to 85	°C
Storage temperature	T_{STG}	-65 to 150	°C

[1] Excluding RTIP and RRING which must stay within -6V to RV+ + 0.3V.
[2] Transient currents of up to 100 mA will not cause SCR latch-up. TTIP, TRING, TV+ and TGND can withstand a continuous current of 100 mA.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	NOM	MAX	UNIT
DC supply (see note 1)	RV+, TV+	4.75	5.0	5.25	V
Ambient Operating Temperature	T_A	-40	25	85	°C
Total power dissipation P_D (see note 2)	100% ones density & max line length @ 5.25V	-	-	400	mW

[1] TV+ must not exceed RV+ by more than ±0.3 V.
[2] Power dissipation while driving 25Ω load over operating temperature range. Includes device and load. Digital input levels are within 10% of the supply rails and digital outputs are driving a 50 pF capacitive load.

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DIGITAL CHARACTERISTICS (T_A = -40° to 85 °C, V+ = 5.0V ±5%, GND = 0V)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
High level input voltage V_{IH} (see notes 1 & 2)		2.0	-	-	V
Low level input voltage V_{IL} (see notes 1 & 2)		-	-	0.8	V
High level output voltage V_{OH} (see notes 1 & 2)	I_{OUT} = -400 µA	2.4	-	-	V
Low level output voltage V_{OL} (see notes 1 & 2)	I_{OUT} = 1.6 mA	-	-	0.4	V
Input leakage current I_{LL} (see note 3)		0	-	±10	µA
Three-state leakage current (see note 2) I_{3L}		0	-	±10	µA

[1] Functionality of pins 23 and 25 depends on mode. See Host / Hardware Mode descriptions.
[2] Output drivers will output CMOS logic levels into CMOS loads.
[3] Except MTIP and MRING I_{LL} = ± 50 µA.

ELECTRICAL SPECIFICATIONS (continued)

ANALOG SPECIFICATIONS (T_A = -40 to 85 °C, V+ = 5.0V ±5%, GND = 0V)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
AMI Output	DSX-1	measured at the DSX	2.4	3.0	3.6	V
Pulse Amplitudes	CEPT	measured at line side	2.7	3.0	3.3	V
Load presented to transmitter output			-	75	-	Ω
Jitter added by	10 Hz - 8 kHz		-	-	0.01	UI
the transmitter	8 kHz - 40 kHz		-	-	0.025	UI
(see note 1)	10 Hz - 40 kHz		-	-	0.025	UI
	Broad Band		-	-	0.05	UI
Sensitivity below DSX (0 dB = 2.4V)			13.6	-	-	dB
			500	-	-	mV
Loss of Signal threshold			-	0.3	-	V
Data decision	DSX-1		63	70	77	%peak
threshold	CEPT		43	50	57	%peak
Allowable consecutive zeros before LOS			160	175	190	-
Input jitter tolerance	10 kHz - 100 kHz		0.4	-	-	UI
Jitter attenuation curve corner frequency (see note 2)			-	6	-	Hz
Minimum Return Loss (see notes 3 & 4)			Transmit		Receive		
			Min	Typ	Min	Typ	
	51 kHz - 102 kHz		20	28	20	30	dB
	102 kHz - 2.048 MHz		20	28	20	30	dB
	2.048 MHz - 3.072 MHz		20	24	20	25	dB

[1] Input signal to TCLK is jitter-free.
[2] Circuit attenuates jitter at 20 dB/decade above the corner frequency.
[3] In accordance with CCITT G.703/RC6367A return loss specifications (CEPT), when wired as shown in Figure 9.
[4] Guaranteed by design.

TABLE 1: Equalizer Control Inputs for Transmitter

EC3	EC2	EC1	Line Length[1]	Cable Loss[2]	Application	Frequency
0	1	1	0 - 133 ft ABAM	0.6 dB	DSX-1	1.544 MHz
1	0	0	133 - 266 ft ABAM	1.2 dB		
1	0	1	266 - 399 ft ABAM	1.8 dB		
1	1	0	399 - 533 ft ABAM	2.4 dB		
1	1	1	533 - 655 ft ABAM	3.0 dB		
0	0	0	CCITT Recommendation G.703		E1 - Coax (75 Ω) E1 - Twisted-pair (120 Ω)	2.048 MHz
0	0	1				
0	1	0	FCC Part 68, Option A		CSU	1.544 MHz
0	1	1	ECSA T1C1.2			

[1] Line length from transceiver to DSX-1 cross-connect point.
[2] Maximum cable loss at 772 kHz.

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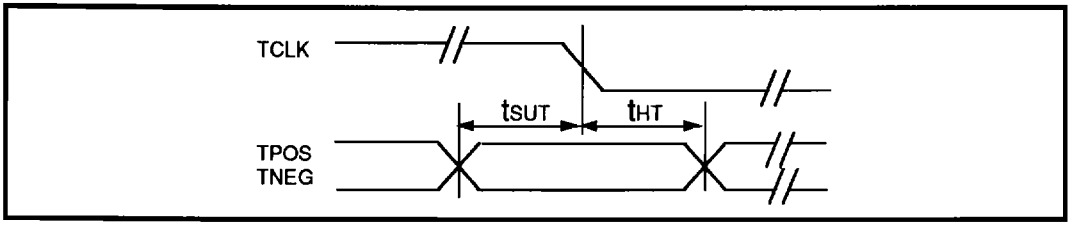

Figure 2: SSI 78P304A Transmit Clock Timing

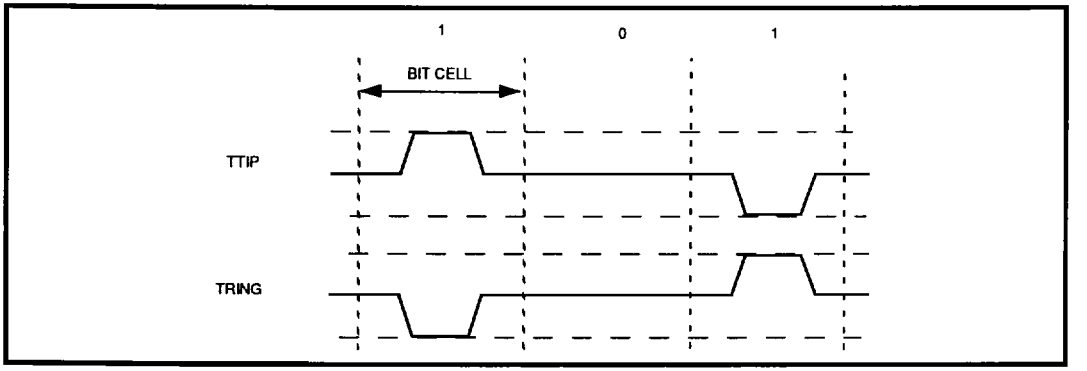

Figure 3: 50% AMI Coding

TABLE 2: SSI 78P304A Master Clock and Transmit Timing Characteristics (See Figure 2)

Parameter		Sym	Min	Typ[1]	Max	Units
Master clock frequency	DSX-1	MCLK	-	1.544	-	MHz
	E1	MCLK	-	2.048	-	MHz
Master clock tolerance		MCLKt	-	±100	-	ppm
Master clock duty cycle		MCLKd	40	-	60	%
Crystal frequency	DSX-1	fc	-	6.176	-	MHz
	E1	fc	-	8.192	-	MHz
Transmit clock frequency	DSX-1	TCLK	-	1.544	-	MHz
	E1	TCLK	-	2.048	-	MHz
Transmit clock tolerance		TCLKt	-	-	±50	ppm
Transmit clock duty cycle		TCLKd	40	-	60	%
TPOS/TNEG to TCLK setup time		t_{SUT}	25	-	-	ns
TCLK to TPOS/TNEG Hold time		t_{HT}	25	-	-	ns

[1] Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

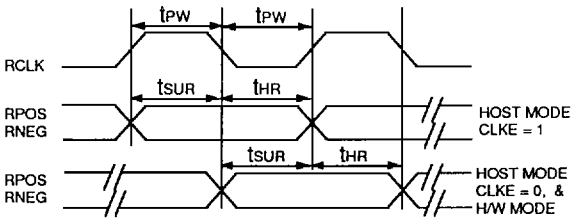

FIGURE 4: SSI 78P304A Receive Clock Timing

TABLE 3: SSI 78P304A Receive Timing Characteristics (See Figure 4)

Parameter		Sym	Min	Typ[1]	Max	Units
Receive clock duty cycle		RCLKd	40	-	60	%
Receive clock pulse width	DSX-1	tPW	-	324	-	ns
	CEPT	tPW	-	244	-	ns
RPOS / RNEG to RCLK	DSX-1	tSUR	-	274	-	ns
rising setup time	CEPT	tSUR	-	194	-	ns
RCLK rising to RPOS /	DSX-1	tHR	-	274	-	ns
RNEG hold time	CEPT	tHR	-	194	-	ns

[1] Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

TABLE 4: SSI 78P304A Crystal Specifications (External)

Parameter	T1	E1
Frequency	6.176 MHz	8.192 MHz
Frequency Stability	±20 ppm @ 25° C ±25 ppm from -40° C to + 85° C (Ref 25° C reading)	±20 ppm @ 25° C ±25 ppm from -40° C to + 85° C (Ref 25° C reading)
Pullability	CL = 11 pF to 18.7 pF, +ΔF = 175 to 195 ppm CL = 18.7 pF to 34 pF, -ΔF = 175 to 195 ppm	CL = 11 pF to 18.7 pF, +ΔF = 95 to 115 ppm CL = 18.7 pF to 34 pF, -ΔF = 95 to 115 ppm
Effective series resistance	40Ω Maximum	30Ω Maximum
Crystal cut	AT	AT
Resonance	Parallel	Parallel
Maximum drive level	2.0 mW	2.0 mW
Mode of operation	Fundamental	Fundamental
Crystal holder	HC49 (R3W), C_O = 7 pF maximum C_M = 17 pF typical	HC49 (R3W), C_O = 7 pF maximum C_M = 17 pF typical

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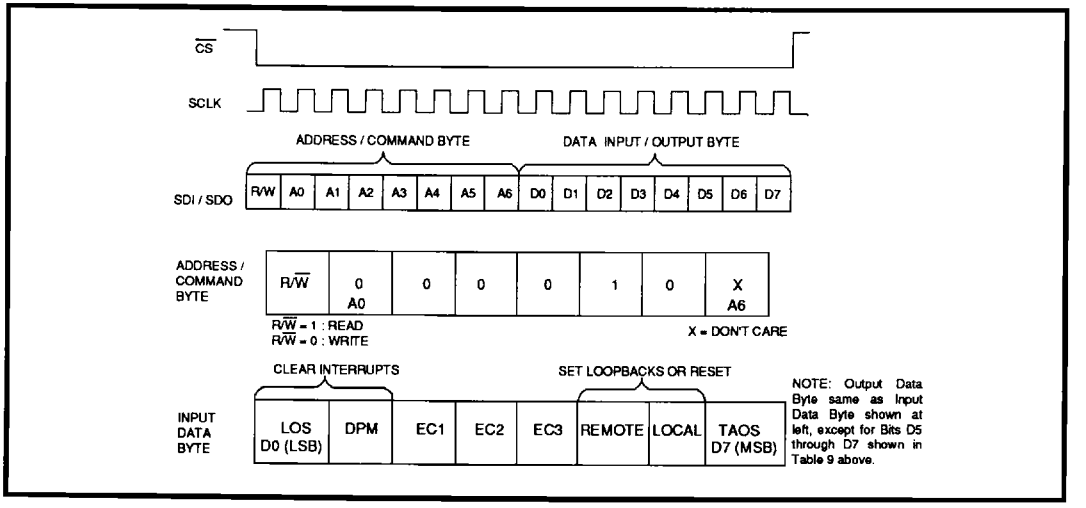

FIGURE 5: SSI 78P304A Serial Interface Data Structure

TABLE 5: SSI 78P304A Serial Data Output Bits (See Figure 5)

Bit D5	Bit D6	Bit D7	Status
0	0	0	Reset has occurred, or no program input.
0	0	1	TAOS active
0	1	0	Local Loopback active
0	1	1	TAOS and Local Loopback active
1	0	0	Remote Loopback active
1	0	1	DPM has changed state since last Clear DPM occurred
1	1	0	LOS has changed state since last Clear LOS occurred
1	1	1	LOS and DPM have both changed state since last Clear DPM and Clear LOS occurred

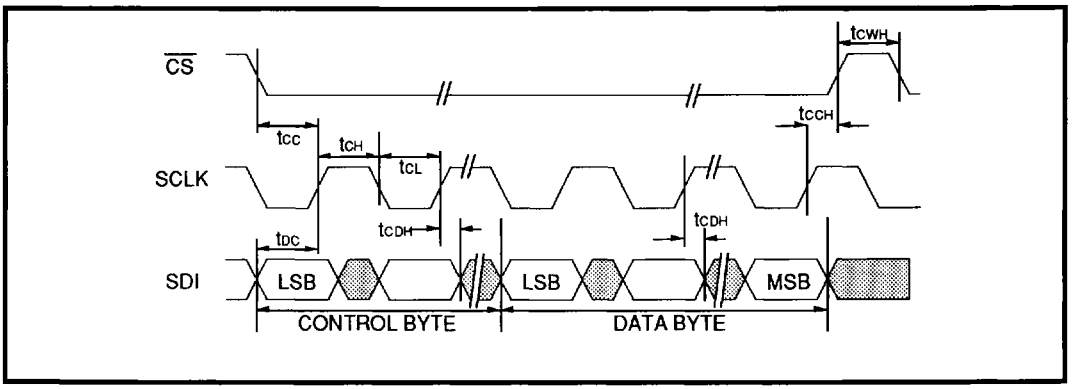

FIGURE 6: SSI 78P304A Serial Data Input Timing Diagram

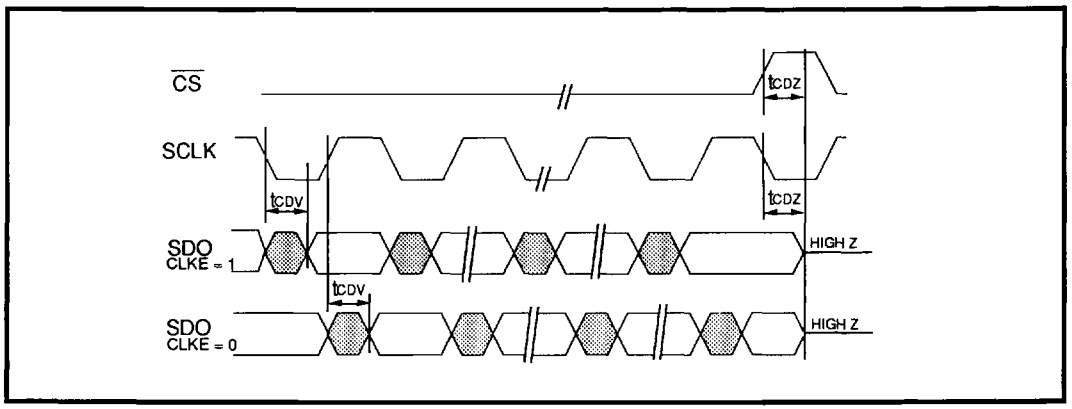

Figure 7: SSI 78P304A Serial Data Output Timing Diagram

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TABLE 6: SSI 78P304A Serial I/O Timing Characteristics (See Figures 6 and 7)

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Rise/Fall time - any digital output	t_{RF}	-	-	100	ns	Load 1.6 mA, 50pF
SDI to SCLK setup time	t_{DC}	50	-	-	ns	
SCLK to SDI hold time	t_{CDH}	50	-	-	ns	
SCLK low time	t_{CL}	240	-	-	ns	
SCLK high time	t_{CH}	240	-	-	ns	
SCLK rise and fall time	t_R , t_F	-	-	50	ns	
$\overline{CS}$ to SCLK setup time	t_{CC}	50	-	-	ns	
SCLK to $\overline{CS}$ hold time	t_{CCH}	50	-	-	ns	
$\overline{CS}$ inactive time	t_{CWH}	250	-	-	ns	
SCLK to SDO valid	t_{CDV}	-	-	200	ns	
SCLK falling edge or $\overline{CS}$ rising edge to SDO high Z	t_{CDZ}	-	100	-	ns	

[1] Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

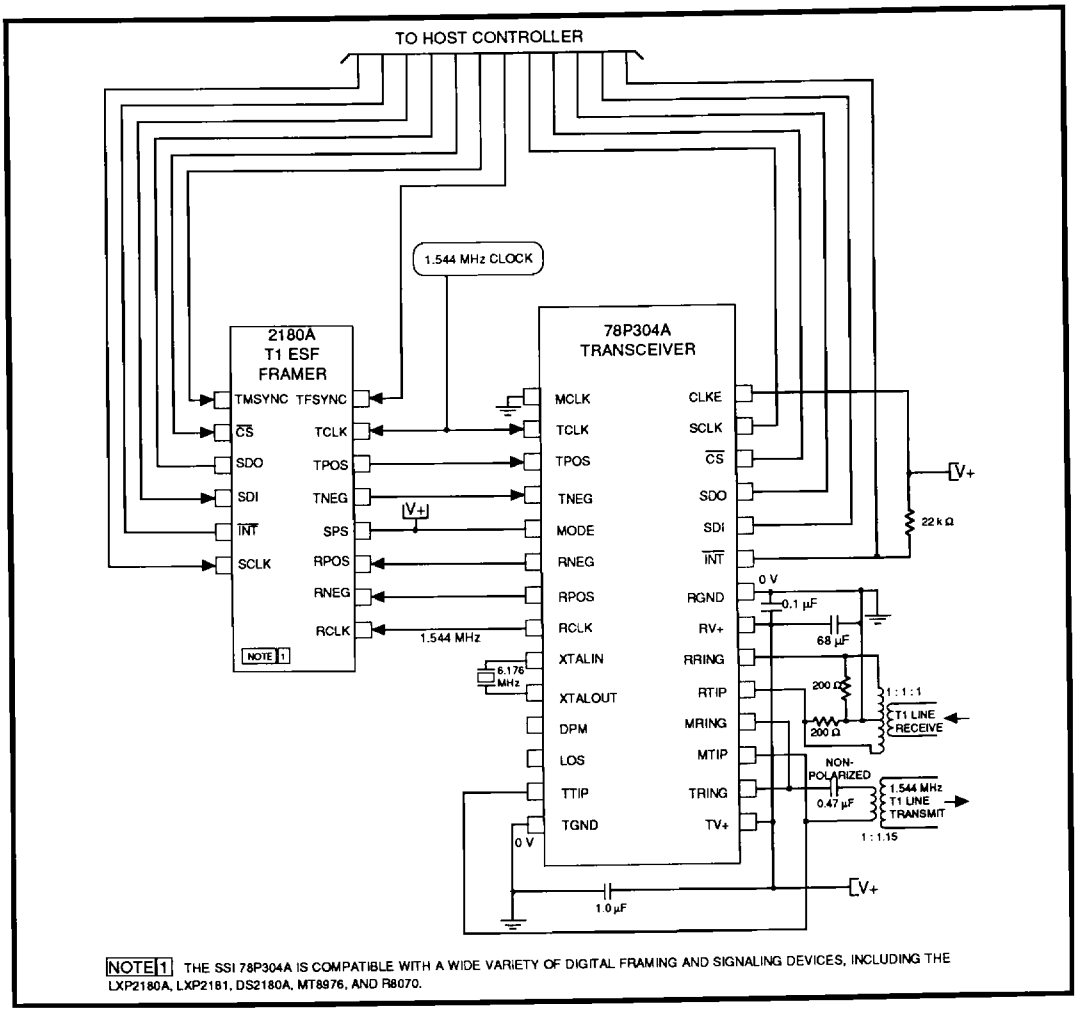
APPLICATION INFORMATION

1.544 MHz T1 INTERFACE APPLICATIONS

Figure 8 is a typical 1.544 MHz T1 application. The SSI 78P304A is shown in the Host mode with the 2180A T1/ESF Framer providing the digital interface with the host controller. Both devices are controlled through the serial interface. The power supply inputs are tied to a common bus with appropriate decoupling capacitors installed (1.0 µF on the transmit side, 68 µF and 0.1 µF on the receive side.)

TABLE 7: E1/CEPT Output Combinations

EC	75Ω Coax	120Ω TWP
0 0 1	1:1, Rt = 10Ω	1:1, Rt = 0Ω
0 0 1	1:2, Rt = 14.3Ω	1:2, Rt = 15Ω
0 0 0	1:1, Rt = 0Ω	1:1.26, Rt = 0Ω
0 0 0	1:2, Rt = 9.37Ω	1:2, Rt = 8.7Ω



NOTE 1 THE SSI 78P304A IS COMPATIBLE WITH A WIDE VARIETY OF DIGITAL FRAMING AND SIGNALING DEVICES, INCLUDING THE LXP2180A, LXP2181, DS2180A, MT8976, AND R8070.

FIGURE 8: Typical SSI 78P304A 1.544 MHz T1 Application (Host Mode)

2.048 MHZ E1/CEPT INTERFACE APPLICATIONS

Figure 9 is a 2.048 MHz E1/CEPT coax application using EC code 000 and 15Ω Rt resistors in line with the transmit transformer to provide high return loss. When high return loss is not a critical factor, a 1:1 or 1:1.26 transformer without in-line resistors provides maximum power savings. Table 7 lists transformer ratios and Rt values with associated 2.048 MHz EC codes for both 75Ω coax and 120Ω TWP. The SSI 78P304A is shown in Hardware mode with the 2181A E1/CRC4 Framer. The hard-wired control lines for TAOS, LLOOP and RLOOP are individually controllable, and the LLOOP and RLOOP lines are also tied to a single control for the Reset function. As in the T1 application Figure 8, this configuration is illustrated with a crystal in place to enable the SSI 78P304A Jitter Attenuation Loop, and a single power supply bus.

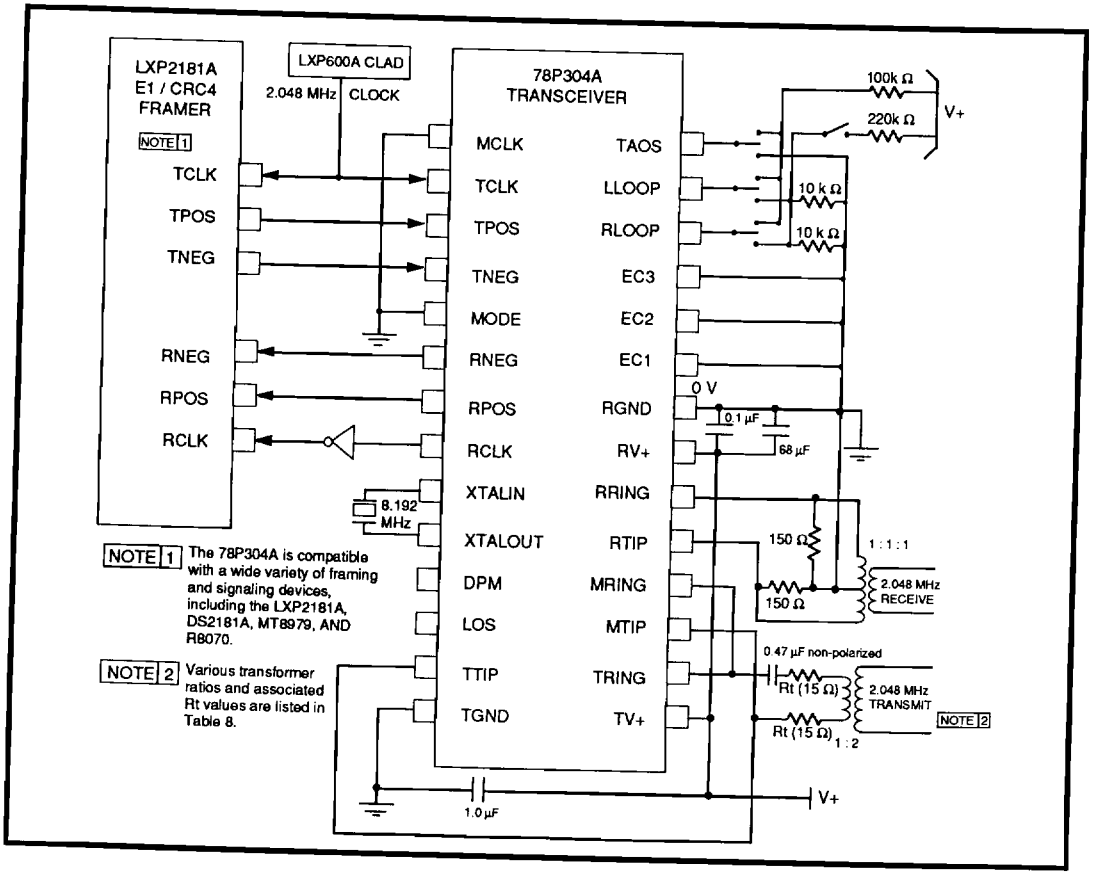
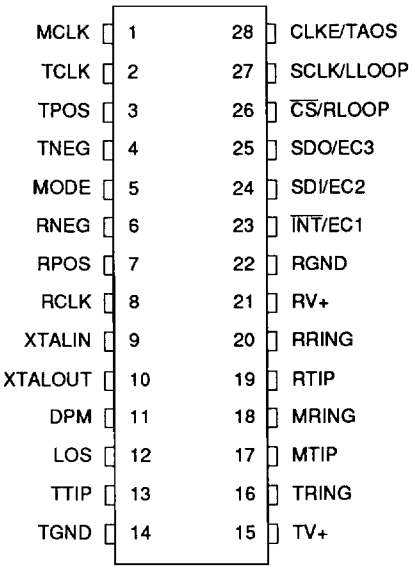


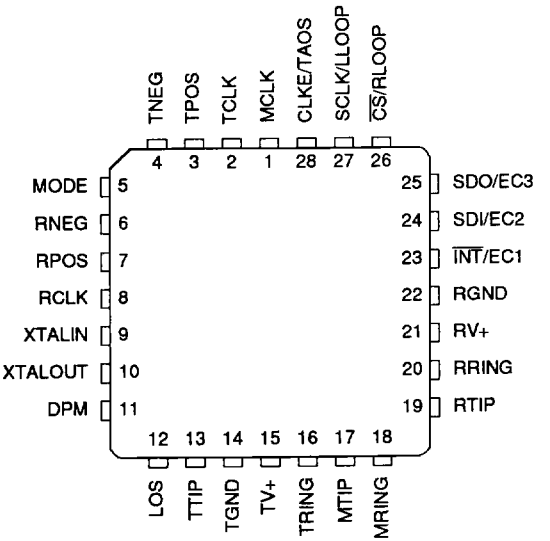
FIGURE 9: SSI 78P304A 2.048 MHz E1 Application (Hardware Mode)

PACKAGE PIN DESIGNATIONS
(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.



28-Pin DIP



28-Pin PLCC

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ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 78P304A 28-Pin DIP	78P304A-IP	78P304A-IP
SSI 78P304A 28-Pin PLCC	78P304A-IH	78P304A-IH

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Notes: