010508

Am9340

Four-Bit Arithmetic Logic Unit

Distinctive Characteristics

- Provides addition and subtraction and two logic functions.
- Typical add time of only 20ns and subtract time of only 25ns for 4 bits.
- Provision made for full look-ahead arithmetic over 16-bit words without additional carry package.
- Can be operated in ripple-block mode to give typical addition time of only 47ns for 28-bit words without additional carry packages.
- 100% reliability assurance testing in compliance with MIL-STD-883
- Electrically tested and optically inspected die for the assemblers of hybrid products
- Mixing privileges for obtaining price discounts. Refer to price list

FUNCTIONAL DESCRIPTION

The Am9340 is a high speed Arithmetic Logic Unit which can perform two arithmetic operations and two logic functions on two binary 4-bit words. The arithmetic operations are add and subtract and the logic functions are AND and EXCLUSIVE OR for active LOW data inputs and OR and EQUIVALENCE for active HIGH data inputs. The operation performed by the Arithmetic Logic Unit is determined by two select inputs S_0 and S_1. The Am9340 can perform arithmetic operations in 1's or 2's complement arithmetic and incorporates full internal look-ahead for high-speed operations.

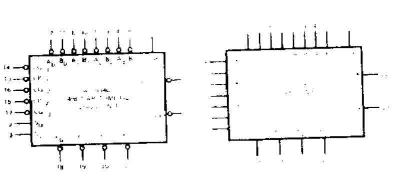
Provision is made for external look-ahead by using the ($\overline{CP}$) carry propagate and ($\overline{CO}/\overline{CG}$) carry out/carry generate functions. An input carry network on the Arithmetic Logic Unit allows full look-ahead over the first sixteen bits of a word and ripple-block carry between subsequent word increments of 12 bits. This ripple-block carry method of cascading units is accomplished by having the (COE) carry out enable input HIGH at the most significant unit in each block so as to give a carry-out signal from the carry out/carry generate output. This carry-out signal is then used as the carry-in signal to the next block. The COE inputs for all other units are tied to ground as shown in Figure 3. This ripple-block method of addition and subtraction gives high-speed operation 60ns typical addition time for 40-bit words, without additional carry packages.

The Am9340 can be used with either active LOW or active HIGH data inputs. In the active HIGH case although the look-ahead carry inputs and outputs are not carry generate and carry propagate, but are labelled C_X and C_Y respectively they are still connected in the same manner as the active LOW case.

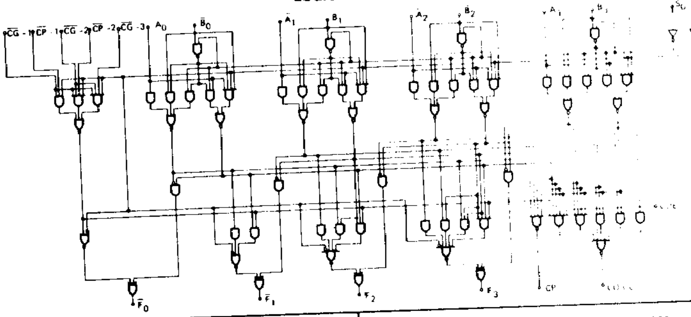
LOGIC SYMBOL

Active LOW

Active HIGH



LOGIC DIAGRAM



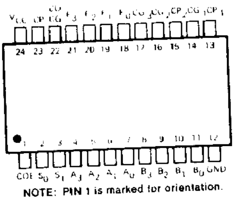
Am9340 ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0°C to +75°C	AM934059C
Hermetic DIP	0°C to +75°C	U6N934059X
Hermetic DIP	−55°C to +125°C	U6N934051X
Hermetic Flat Pak	−55°C to +125°C	U4M934051X
Dice	Note	UXX9340XXD

Note: The dice supplied will contain units which meet both 0°C to +75°C and −55°C to +125°C temperature range.

CONNECTION DIAGRAM

Top View



NOTE: PIN 1 is marked for orientation.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 24 to Pin 12) Continuous	−0.5 V to +7 V
DC Voltage Applied to Outputs for High Output State	−0.5 V to $+V_{CC}$ max
DC Input Voltage	−0.5 V to +5.5 V
Output Current, Into Outputs	30 mA
DC Input Current	−30 mA to +5.0 mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am934059X $T_A = 0°C$ to $+75°C$ $V_{CC} = 5.0\ V \pm 5\%$
Am934051X $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0\ V \pm 10\%$

Parameters	Description	Test Conditions		Min	Typ (Note 1)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., $I_{OH} = -0.8$ mA $V_{IN} = V_{IH}$ or V_{IL}		2.4	3.6		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., $I_{OL} = 16.0$ mA $V_{IN} = V_{IH}$ or V_{IL}			0.2	0.4	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
I_{IL} (Note 2)	Unit Load Input LOW Current	V_{CC} = MAX., $V_{IN} = 0.4$ V			−1.0	−1.6	mA
I_{IH} (Note 2)	Unit Load Input HIGH Current	V_{CC} = MAX., $V_{IN} = 2.4$ V			6.0	40	μA
	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 5.5$ V				1.0	mA
I_{SC}	Output Short Circuit Current	V_{CC} = MAX., $V_{OUT} = 0.0$ V	Am934051X	−30		−100	mA
			Am934059X	−30		−100	
I_{CC}	Power Supply Current	$S_O = B_{0-3} = 0$ V All other inputs = 4.5 V V_{CC} = MAX.	Am934051X		85	127	mA
			Am934059X		85	128	

Notes: 1) Typical limits are at $V_{CC} = 5.0$ V, 25°C ambient and maximum loading.

2) Actual input currents are obtained by multiplying unit load current by input load factor (See Loading Rules).

Switching Characteristics ($T_A = 25°C$)

		Test Conditions	Min	Typ	Max	Units
t_{pd+}	Turn Off Delay ($\overline{B}_0$ to $\overline{F}_3$) Add Mode	$V_{CC} = 5.0$ V, $C_L = 15$ pF Refer to test Table and Figure 1	10	20	30	ns
t_{pd-}	Turn On Delay ($\overline{B}_0$ to $\overline{F}_3$) Add Mode		10	20	30	ns
t_{pd+}	Turn Off Delay ($\overline{B}_0$ to $\overline{F}_3$) Subtract Mode		12	25	38	ns
t_{pd-}	Turn On Delay ($\overline{B}_0$ to $\overline{F}_3$) Subtract Mode		12	24	36	ns
t_{pd+}	Turn Off Delay ($\overline{B}_0$ to $\overline{CO}/\overline{CG}$) Add Mode		7	13	19	ns
t_{pd-}	Turn On Delay ($\overline{B}_0$ to $\overline{CO}/\overline{CG}$) Add Mode		7	13	19	ns
t_{pd+}	Turn Off Delay ($\overline{B}_0$ to $\overline{CO}/\overline{CG}$) Subtract Mode		9	17	25	ns
t_{pd-}	Turn On Delay ($\overline{B}_0$ to $\overline{CO}/\overline{CG}$) Subtract Mode		9	17	25	ns
t_{pd+}	Turn Off Delay ($\overline{CG}_{-1}$ to $\overline{CO}/\overline{CG}$)		7	13	19	ns
t_{pd-}	Turn On Delay ($\overline{CG}_{-1}$ to $\overline{CO}/\overline{CG}$)		7	13	19	ns
t_{pd+}	Turn Off Delay ($\overline{CG}_{-1}$ to $\overline{F}_3$)		11	23	35	ns
t_{pd-}	Turn On Delay ($\overline{CG}_{-1}$ to $\overline{F}_3$)		10	19	29	ns

DEFINITION OF TERMS

SUBSCRIPT TERMS:

F Forward, applying to LOW inputs.

H HIGH, applying to a HIGH logic level or when used with V_{CC} to indicate high V_{CC} value.

I Input.

L LOW, applying to LOW logic level or when used with V_{CC} to indicate low V_{CC} value.

O Output.

R Reverse, applying to HIGH inputs.

FUNCTIONAL TERMS:

$\overline{A}_i$ Active LOW Data A Inputs i = 0, 1, 2, 3.

$\overline{B}_i$ Active LOW Data B Inputs i = 0, 1, 2, 3.

$\overline{CG}_{-i}$ Active LOW Carry Generate input from i'th previous ALU i = 1, 2, 3.

$\overline{CP}_{-i}$ Active LOW Carry Propagate input from i'th previous ALU i = 1, 2.

COE Carry Out Enable input. When this input is HIGH the $\overline{CO/CG}$ output is a carry out signal and can be used to form a block ripple carry ALU. When the COE input is LOW $\overline{CO/CG}$ output is the carry generate signal which is used for lookahead operation.

$\overline{CO/CG}$ Active LOW Carry Out/Carry Generate output. A HIGH logic level on COE input gives Carry Out, a LOW level Carry Generate.

$\overline{CP}$ Active LOW Carry Propagate output used in conjunction with other $\overline{CG}$ and $\overline{CP}$ signals for lookahead operation.

$\overline{F}_i$ Active LOW Data Outputs of ALU i = 0, 1, 2, 3.

Fan-Out The logic HIGH or LOW output drive capability in terms of Input Unit Loads.

S_i Control inputs determine the arithmetic or logic function obeyed i = 0, 1.

Unit Load One T^2L gate input load. In the HIGH state it is equal to 40 µA at 2.4 V and in the LOW state it is equal to 1.6 mA at 0.4 V.

OPERATIONAL TERMS:

I_{IL} Forward input load current.

I_{OH} Output HIGH current forced out of output in V_{OH} test.

I_{OL} Output LOW current forced into the output in V_{OL} test.

I_{IH} Reverse input load current.

I_{CC} The current drawn by the device under a +5.0 V power supply bias with inputs S_0, B_0, B_1, B_2, B_3 at 0 V and all other inputs and outputs open circuit.

Negative Current Current flowing out of the device.

Positive Current Current flowing into the device.

V_{IH} Minimum logic HIGH input voltage. Refer to Figure 2.

V_{IL} Maximum logic LOW input voltage. Refer to Figure 2.

V_{OH} Minimum logic HIGH output voltage with output HIGH current I_{OH} flowing out of output.

V_{OL} Maximum logic LOW output voltage with output LOW current I_{OL} into output.

SWITCHING TERMS: (All switching times are measured at the 1.5 V logic level.)

t_{pd+} ($\overline{B}_0$ $\overline{F}_1$) The propagation delay from the $\overline{B}_0$ input transition to the $\overline{F}_3$ output LOW to HIGH transition.

t_{pd-} ($\overline{B}_0$ $\overline{F}_1$) The propagation delay from the $\overline{B}_0$ input transition to the $\overline{F}_3$ output HIGH to LOW transition.

t_{pd+} ($\overline{B}_0$ $\overline{CO/CG}$) The propagation delay from the $\overline{B}_0$ input transition to the $\overline{CO/CG}$ output LOW to HIGH transition.

t_{pd-} ($\overline{B}_0$ $\overline{CO/CG}$) The propagation delay from the $\overline{B}_0$ input transition to the $\overline{CO/CG}$ output HIGH to LOW transition.

t_{pd+} ($\overline{CG}_{-3}$ $\overline{CO/CG}$) The propagation delay from the $\overline{CG}_{-3}$ input transition to the $\overline{CO/CG}$ LOW to HIGH transition.

t_{pd-} ($\overline{CG}_{-3}$ $\overline{CO/CG}$) The propagation delay from the $\overline{CG}_{-3}$ input transition to the $\overline{CO/CG}$ HIGH to LOW transition.

t_{pd+} ($\overline{CG}_{-3}$ $\overline{F}_3$) The propagation delay from the $\overline{CG}_{-3}$ input transition to the $\overline{F}_3$ output LOW to HIGH transition.

t_{pd-} ($\overline{CG}_{-3}$ $\overline{F}_3$) The propagation delay from the $\overline{CG}_{-3}$ input transition to the $\overline{F}_3$ output HIGH to LOW transition.

SWITCHING TEST TABLE

Parameter	Operation	Inputs at 4.5 V	Inputs at GND	Waveform
t_{pd+} ($\overline{B}_0$ $\overline{F}_3$) t_{pd-} ($\overline{B}_0$ $\overline{F}_3$)	Add	S_0, $\overline{CG}_{-1}$, $\overline{CP}_{-1}$, $\overline{B}_1$, $\overline{B}_2$	S_1, $\overline{A}_0$, $\overline{A}_1$, $\overline{A}_2$, $\overline{A}_3$, $\overline{B}_3$	1
t_{pd+} ($\overline{B}_0$ $\overline{F}_3$) t_{pd-} ($\overline{B}_0$ $\overline{F}_3$)	Subtract	$\overline{CG}_{-1}$, $\overline{CP}_{-1}$, $\overline{B}_3$	S_0, S_1, $\overline{A}_0$, $\overline{A}_1$, $\overline{A}_2$, $\overline{A}_3$ $\overline{B}_1$, $\overline{B}_2$	2
t_{pd+} ($\overline{B}_0$ $\overline{CO/CG}$) t_{pd-} ($\overline{B}_0$ $\overline{CO/CG}$)	Add	S_0, $\overline{CG}_{-1}$, $\overline{CP}_{-1}$, $\overline{B}_1$, $\overline{B}_2$, $\overline{B}_3$	S_1, COE, $\overline{A}_0$, $\overline{A}_1$, $\overline{A}_2$, $\overline{A}_3$	1
t_{pd+} ($\overline{B}_0$ $\overline{CO/CG}$) t_{pd-} ($\overline{B}_0$ $\overline{CO/CG}$)	Subtract	$\overline{CG}_{-1}$, $\overline{CP}_{-1}$	S_0, S_1, COE, $\overline{A}_0$, $\overline{A}_1$, $\overline{A}_2$, $\overline{A}_3$ $\overline{B}_1$, $\overline{B}_2$, $\overline{B}_3$	2
t_{pd+} ($\overline{CG}_{-3}$ $\overline{CO/CG}$) t_{pd-} ($\overline{CG}_{-3}$ $\overline{CO/CG}$)	Add	S_0, $\overline{CG}_{-1}$, $\overline{CG}_{-2}$, COE, $\overline{A}_0$, $\overline{A}_1$, $\overline{A}_2$, $\overline{A}_3$	S_1, $\overline{B}_0$, $\overline{B}_1$, $\overline{B}_2$, $\overline{B}_3$ $\overline{CP}_{-1}$, $\overline{CP}_{-2}$	1
t_{pd+} ($\overline{CG}_{-3}$ $\overline{F}_3$) t_{pd-} ($\overline{CG}_{-3}$ $\overline{F}_3$)	Add	S_0, $\overline{CG}_{-1}$, $\overline{CG}_{-2}$, $\overline{B}_3$ $\overline{A}_0$, $\overline{A}_1$, $\overline{A}_2$, $\overline{A}_3$	S_1, $\overline{B}_0$, $\overline{B}_1$, $\overline{B}_2$, $\overline{CP}_{-1}$, $\overline{CP}_{-2}$	1

SWITCHING WAVEFORMS

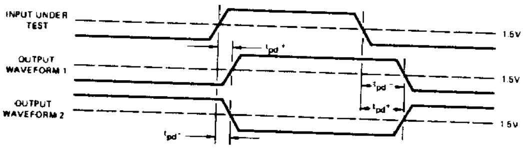
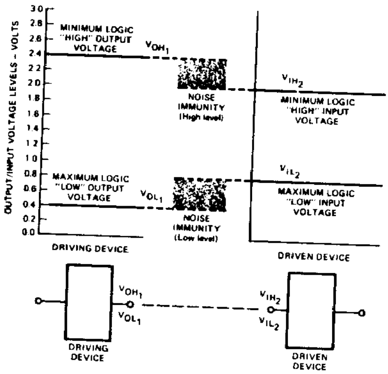


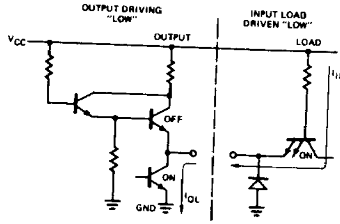
Figure 1

INPUT/OUTPUT INTERFACE CONDITIONS

Voltage Interface Conditions — LOW & HIGH



Current Interface Conditions — LOW



Current Interface Conditions — HIGH

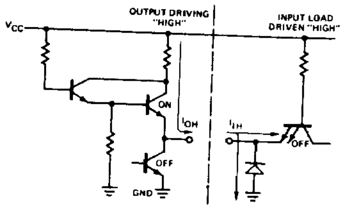


Figure 2

MSI INTERFACING RULES

Interfacing Digital Family	Equivalent Input Unit Load HIGH	LOW
Advanced Micro Devices 9300/2500 Series	1	1
FSC Series 9300	1	1
TI Series 54/7400	1	1
Signetics Series 8200	2	2
National Series DM 75/85	1	1
DTL Series 930	12	1

Table I

USER NOTES

1. Arithmetic operations are performed on a word basis.
2. Logic operations are performed on a bit basis.
3. Arithmetic in 1's complement requires an end-around carry. This is obtained by connecting the $\overline{CO/CG}$ output of the last ALU to the $\overline{CG}_{-1}$ input of the first ALU.
4. Subtraction in 2's complement requires a carry-in ($\overline{CG}_{-1}$ = LOW) active LOW case, (CX_{-1} = HIGH) active HIGH case. This is obtained by connecting S_0 to $\overline{CG}_{-1}$ for the active LOW case and S_0 through an inverter to CX_{-1} for the active HIGH case.

Am9340 LOADING RULES (in unit loads)

Input/Output	Pin No.'s	Input Unit Load	Output Drive HIGH	Output Drive LOW
COE	1	1.5	—	—
S_0	2	1	—	—
S_1	3	1	—	—
$\overline{A}_3$	4	3	—	—
$\overline{A}_2$	5	3	—	—
$\overline{A}_1$	6	3	—	—
$\overline{A}_0$	7	3	—	—
$\overline{B}_3$	8	3	—	—
$\overline{B}_2$	9	3	—	—
$\overline{B}_1$	10	3	—	—
$\overline{B}_0$	11	3	—	—
GND	12	—	—	—
$\overline{CP}_{-1}$	13	1	—	—
$\overline{CG}_{-1}$	14	3	—	—
$\overline{CP}_{-2}$	15	1	—	—
$\overline{CG}_{-2}$	16	2	—	—
$\overline{CG}_{-3}$	17	1	—	—
$\overline{F}_0$	18	—	20	10
$\overline{F}_1$	19	—	20	10
$\overline{F}_2$	20	—	20	10
$\overline{F}_3$	21	—	20	10
$\overline{CO/CG}$	22	—	20	10
$\overline{CP}$	23	—	20	10
V_{CC}	24	—	—	—

Table II

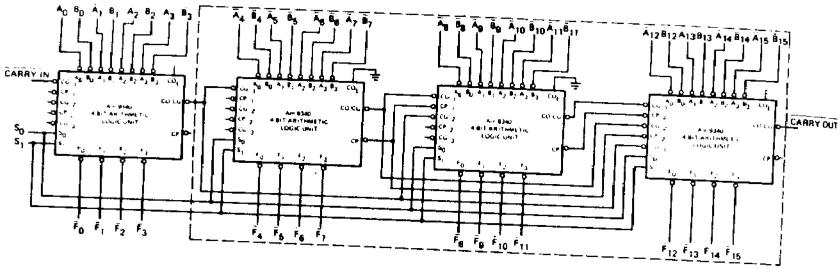
OPERATION TABLE

Control Inputs	Active LOW Inputs and Outputs	Active HIGH Inputs and Outputs
S_0 S_1	Function	Function
L L	A SUBTRACT B	A SUBTRACT B
H L	A ADD B	A ADD B
L H	A EXCLUSIVE OR B	A EQUIVALENCE B
H H	A AND B	A OR B

H = HIGH Voltage Level
L = LOW Voltage Level

Table III

Am9340 APPLICATION



16-Bit Full Look-ahead ALU

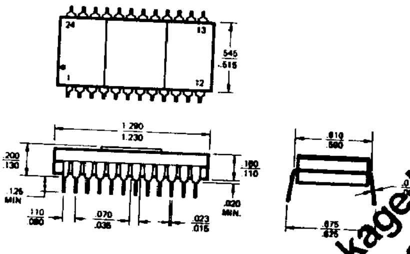
Four Am9340 ALU's can be connected together to form a 16-bit full look-ahead ALU. This ALU can work in 1's or 2's complement arithmetic representations and in the active LOW or active HIGH logic representations. If longer word lengths are required 12-bit ALU blocks connected as shown in the dashed portion of the diagram can be cascaded at the end of the 16-bit full look-ahead portion.

TYPICAL DELAY TABLE

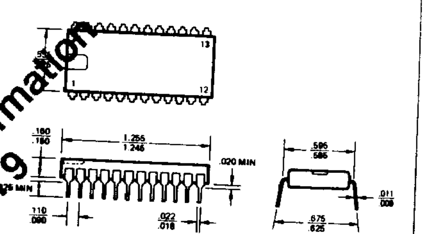
WORD LENGTH (in bits)	ADD (in ns)	SUBTRACT (in ns)
1-4	20	25
5-16	34	39
17-28	47	52
29-40	60	65
41-52	73	78
53-64	86	91
65-76	99	104
77-88	114	127
89-100	127	140

Figure 3

PHYSICAL DIMENSIONS
Hermetic Dual In-Line

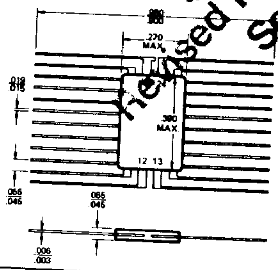


PHYSICAL DIMENSIONS
Molded Dual-In-Line

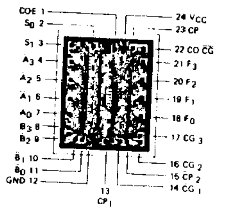


Revised Package Information
See Section 9

PHYSICAL DIMENSIONS
Flat Package



Metallization and Pad Layout



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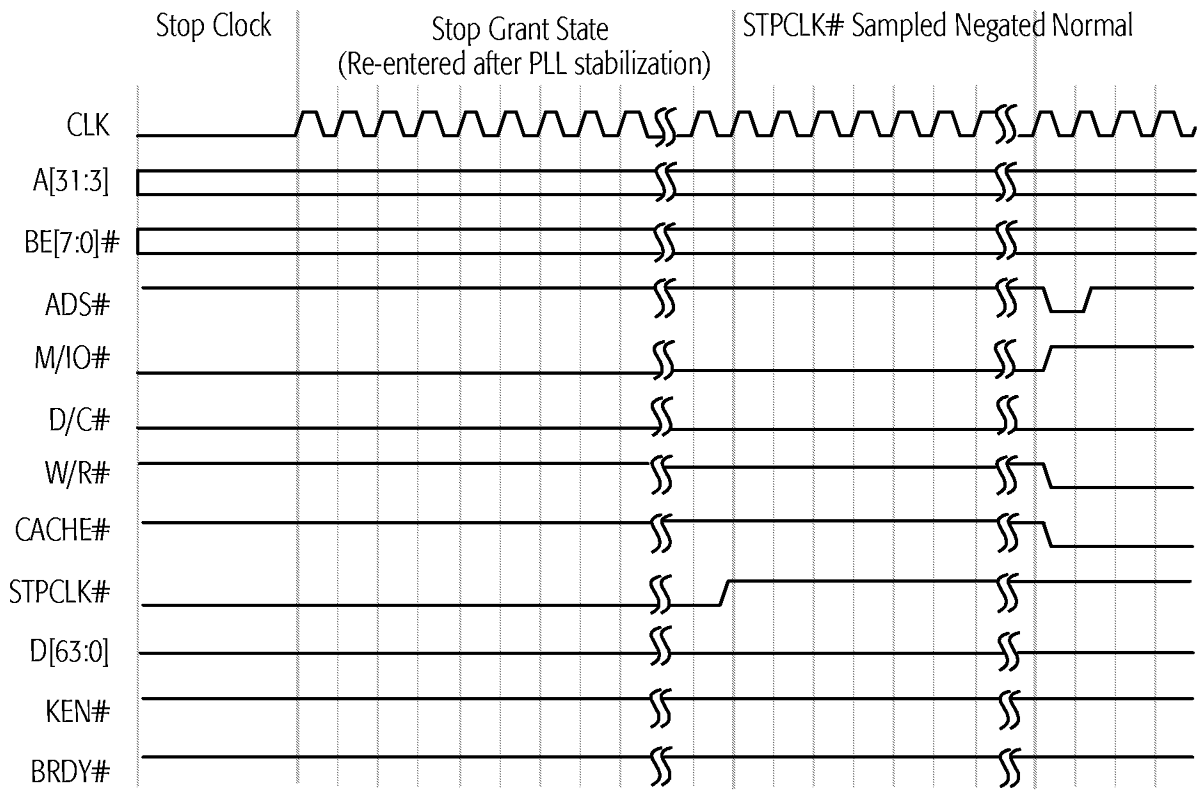

Figure 75. Stop Grant and Stop Clock Modes, Part 2

INIT-Initiated Transition from Protected Mode to Real Mode

INIT is typically asserted in response to a BIOS interrupt that writes to an I/O port. This interrupt is often in response to a Ctrl-Alt-Del keyboard input. The BIOS writes to a port (similar to port 64h in the keyboard controller) that asserts INIT. INIT is also used to support 80286 software that must return to Real mode after accessing extended memory in Protected mode.

The assertion of INIT causes the processor to empty its pipelines, initialize most of its internal state, and branch to address FFFF_FFF0h—the same instruction execution starting point used after RESET. Unlike RESET, the processor preserves the contents of its caches, the floating-point state, the MMX state, Model-Specific Registers (MSRs), the CD and NW bits of the CR0 register, the time stamp counter, and other specific internal resources.

Figure 76 shows an example in which the operating system writes to an I/O port, causing the system logic to assert INIT. The sampling of INIT asserted starts an extended microcode sequence that terminates with a code fetch from FFFF_FFF0h, the reset location. INIT is sampled on every clock edge but is not recognized until the next instruction boundary. During an I/O write cycle, it must be sampled asserted a minimum of three clock edges before BRDY# is sampled asserted if it is to be recognized on the boundary between the I/O write instruction and the following instruction. If INIT is asserted synchronously, it can be asserted for a minimum of one clock. If it is asserted asynchronously, it must have been negated for a minimum of two clocks, followed by an assertion of a minimum of two clocks.

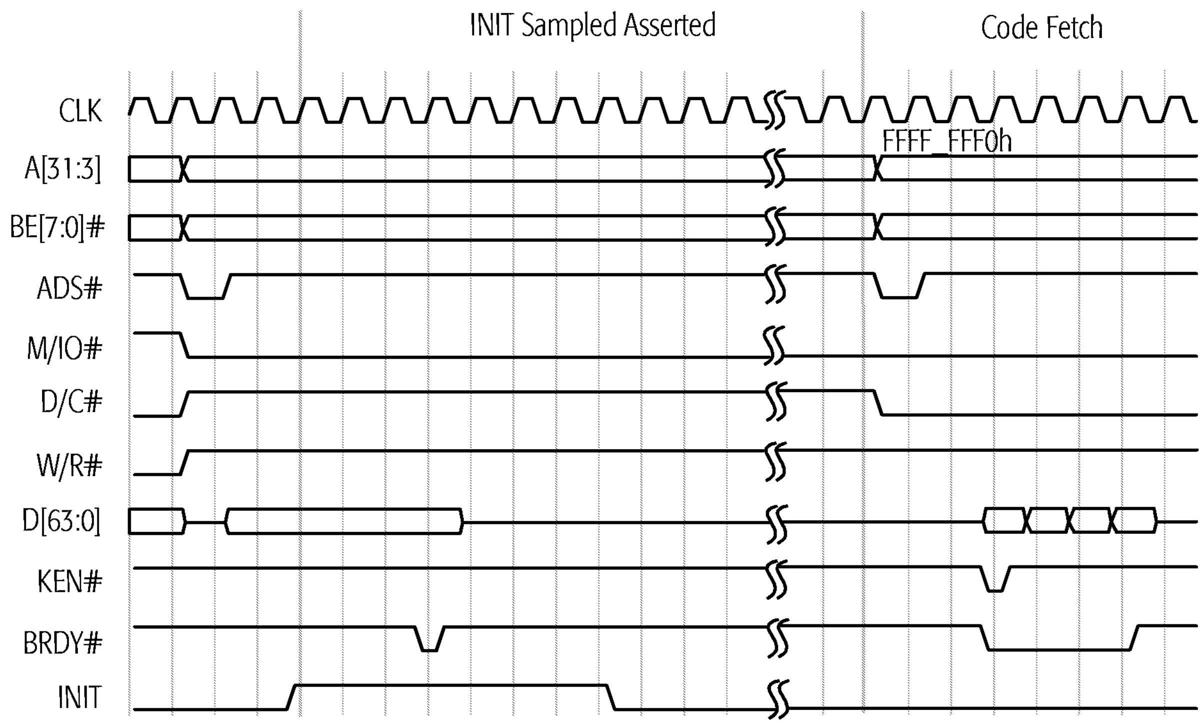

Figure 76. INIT-Initiated Transition from Protected Mode to Real Mode

6 Power-on Configuration and Initialization

On power-on the system logic must reset the AMD-K6-2 processor by asserting the RESET signal. When the processor samples RESET asserted, it immediately flushes and initializes all internal resources and its internal state, including its pipelines and caches, the floating-point state, the MMX and 3DNow! states, and all registers. Then the processor jumps to address FFFF_FFF0h to start instruction execution.

6.1 Signals Sampled During the Falling Transition of RESET

FLUSH# FLUSH# is sampled on the falling transition of RESET to determine if the processor begins normal instruction execution or enters Tri-State Test mode. If FLUSH# is High during the falling transition of RESET, the processor unconditionally runs its Built-In Self Test (BIST), performs the normal reset functions, then jumps to address FFFF_FFF0h to start instruction execution. (See "Built-In Self-Test (BIST)" on page 217 for more details.) If FLUSH# is Low during the falling transition of RESET, the processor enters Tri-State Test mode. (See "Tri-State Test Mode" on page 218 and "FLUSH# (Cache Flush)" on page 103 for more details.)

BF[2:0] The internal operating frequency of the processor is determined by the state of the bus frequency signals BF[2:0] when they are sampled during the falling transition of RESET. The frequency of the CLK input signal is multiplied internally by a ratio defined by BF[2:0]. (See "BF[2:0] (Bus Frequency)" on page 92 for the processor-clock to bus-clock ratios.)

BRDYC# BRDYC# is sampled on the falling transition of RESET to configure the drive strength of A[20:3], ADS#, HITM#, and W/R#. If BRDYC# is Low during the fall of RESET, these outputs are configured using higher drive strengths than the standard strength. If BRDYC# is High during the fall of RESET, the standard strength is selected. (See "BRDYC# (Burst Ready Copy)" on page 95 for more details.)

6.2 RESET Requirements

During the initial power-on reset of the processor, RESET must remain asserted for a minimum of 1.0 ms after CLK and V_{CC} reach specification. (See “CLK Switching Characteristics” on page 255 for clock specifications. See “Electrical Data” on page 247 for V_{CC} specifications.)

During a warm reset while CLK and V_{CC} are within specification, RESET must remain asserted for a minimum of 15 clocks prior to its negation.

6.3 State of Processor After RESET

Output Signals

Table 31 shows the state of all processor outputs and bidirectional signals immediately after RESET is sampled asserted.

Table 31. Output Signal State After RESET

Signal	State	Signal	State
A[31:3], AP	Floating	LOCK#	High
ADS#, ADSC#	High	M/IO#	Low
APCHK#	High	PCD	Low
BE[7:0]#	Floating	PCHK#	High
BREQ	Low	PWT	Low
CACHE#	High	SCYC	Low
D/C#	Low	SMIACT#	High
D[63:0], DP[7:0]	Floating	TDO	Floating
FERR#	High	VCC2DET	Low
HIT#	High	VCC2H/L#	Low
HITM#	High	W/R#	Low
HLDA	Low	–	–

Registers

Table 32 on page 175 shows the state of all architecture registers and Model-Specific Registers (MSRs) after the processor has completed its initialization due to the recognition of the assertion of RESET.