

• • • • • V363EPC Local Bus to PCI Bridge for Embedded Processors

Device Highlights

- Direct interface to these processors:
 - AMD® AM29030/40™
 - IBM® PowerPC 401™ Gx
 - Intel® i960® Cx/Hx/Jx/Sx
- Fully compliant with *PCI Local Bus Specification*, Revision 2.1
- Configurable for system master, PCI bus master, or PCI target operation
- Type 0 and Type 1 PCI configuration cycles
- Up to 1 KB burst access on the PCI or the local bus
- 640 bytes of programmable FIFO storage with Dynamic Bandwidth Allocation™ architecture
- 64-byte read FIFO in each direction
- Enhanced support for 8-bit/16-bit local bus devices with programmable region sizes
- Dual bi-directional address space remapping
- 10-bit bus watch timer
- On-the-fly byte order (endian) conversion
- I₂O-Ready™ ATU and messaging unit, including hardware controlled circular queues
- Two-channel DMA, multiprocessor DMA chaining, and demand mode DMA
- Hot Swap Capable™ according to the *PICMG® Hot Swap Specification*, version 2.1
- Sixteen 8-bit bi-directional mailbox registers with doorbell interrupts
- Support for real-mode MS-DOS® holes
- Flexible PCI and local interrupt management
- Optional power-on serial EEPROM initialization

- Up to 50 MHz on both PCI and local bus clocks
- 3.3 V operation; 5 V tolerant input
- Industrial temperature range (
 - –40°C to +85°C)
- Low-cost 160-pin EIAJ PQFP package (Electronic Industries Association of Japan Plastic Quad Flat Pack)

Overview

The V363EPC offers the highest performance, most flexible, and most economical solution for interfacing either 32-bit or 16-bit local bus applications to the PCI bus. It is also an ideal candidate for a variety of high-performance applications based on Motorola, IBM, DEC, Hitachi, and other popular embedded processors where only a minimal amount of glue logic is needed.

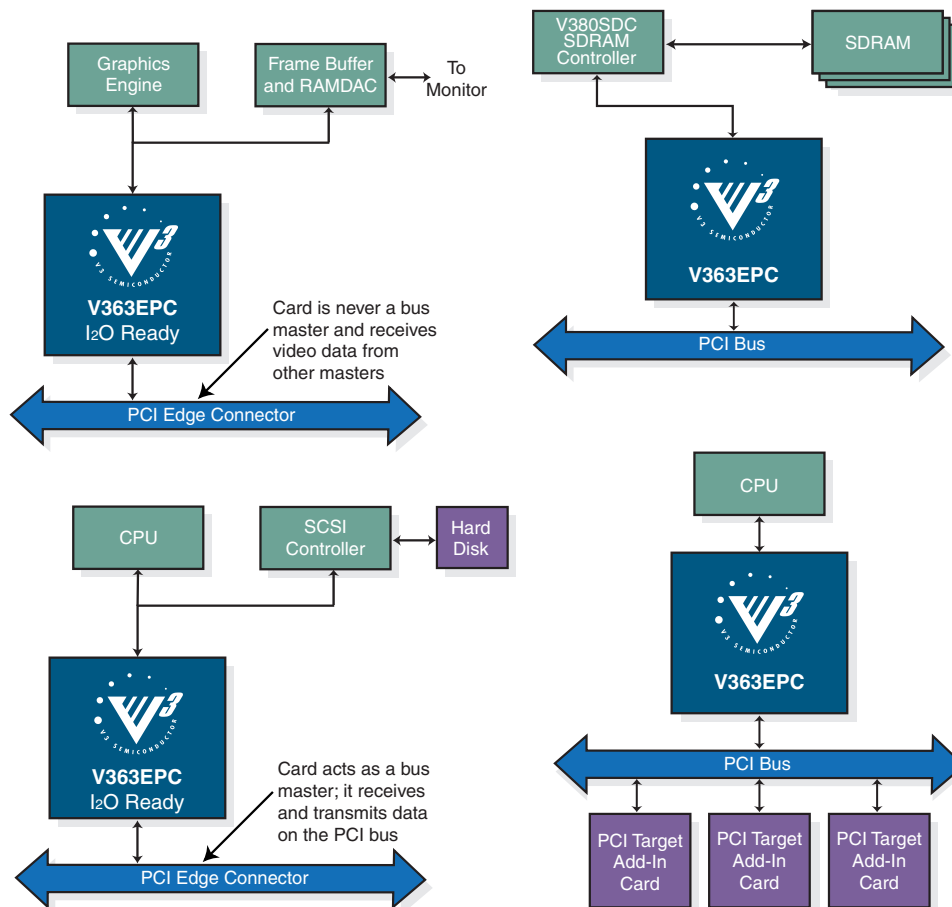
V363EPC is the 3.3 V enhanced version of the V350EPC and V360EPC Rev A1 devices and supports powerful features like Hot Swap and DMA chaining. The PCI bus operates at up to 50 MHz, independent of local bus clock frequency. The overall throughput of the system is dramatically improved by using our unique Dynamic Bandwidth Allocation architecture.

Access to the PCI bus can be performed through two programmable address apertures. Two more apertures are provided for PCI-to-local bus accesses. There are 64 bytes of read FIFOs in each direction, 32 bytes dedicated for each aperture.

Two high-performance DMA channels with chaining and demand mode capabilities provide a powerful data transfer engine for bulk data transfers. Mailbox registers and flexible PCI interrupt controllers also provide a simple mechanism to emulate PCI device control ports. The part is available in a 160-pin, low-cost PQFP package.

This document contains the product codes, electrical specifications, pinout, and package mechanical information for the V363EPC. Detailed functional information is contained in the *V363EPC User's Manual*.

Figure 1: Example Applications



Product Codes

Table 1: Product Codes

Product Code	Package	Frequency
V363EPC-50LP REV A0	160-pin EIAJ PQFP	50 MHz
V363EPC-50LPN ^a REV A0	PB-Free 160-pin EIAJ PQFP	50 MHz

a. Lead free.

Electrical Specifications

DC Characteristics

The DC characteristics for the PCI bus signals reference those given in the *PCI Local Bus Specification*, Revision 2.1, Section 4.2.2.1. For more information on the PCI DC specifications, see the *PCI Local Bus Specification*.

Table 2: Absolute Maximum Ratings

Symbol	Parameter	Value	Units
V_{CC}	Supply voltage	–0.3 to 3.8	V
V_{IN}	DC input voltage	–0.3 to 5.75	V
T_{STG}	Storage temperature range	–55 to 125	°C

Table 3: Guaranteed Operating Conditions

Symbol	Parameter	Value	Units
V_{CC}	Supply voltage 3.3 V	3.0 to 3.6	V
J_{max}	Maximum Junction temperature	125	°C
θ_{JA}	Junction-to-ambient thermal resistance	50	°C/w
θ_{JC}	Junction-to-case thermal resistance	11	°C/w
T_A	Ambient temperature range	–40 to 85	°C

PCI Bus DC Specifications

Table 4: PCI Bus Signals DC Operating Specifications

Symbol	Parameter	Condition	Min.	Max.	Units
V_{IH}	Input high voltage ^a		$0.5 V_{CC}$	5.75	V
V_{IL}	Input low voltage		-0.5	$0.3 V_{CC}$	V
I_{IL}	Input leakage current ^b	$0 < V_{IN} < V_{CC}$		± 10	μA
V_{OH}	Output high voltage	$I_{OUT} = -500 \mu A$	$0.9 V_{CC}$		V
V_{OL}	Output low voltage	$I_{OUT} = 1500 \mu A$		$0.1 V_{CC}$	V
C_{IN}	Input pin capacitance ^c			10	pF
C_{CLK}	PCLK pin capacitance		5	12	pF
C_{IDSEL}	IDSEL pin capacitance ^d			8	pF

a. Custom 5 V tolerant PCI buffers are used in the design.

b. Input leakage currents include hi-Z output leakage for all bi-directional buffers with tri-state outputs.

c. Absolute maximum pin capacitance for a PCI unit is 10 pF (except for CLK).

d. Lower capacitance on this input-only pin allows for non-resistive coupling to AD[xx].

Local Bus DC Specifications

Table 5: Local Bus Signals DC Operating Specifications

Symbol	Description	Conditions	Min.	Max.	Units
V_{IL}	Low level input voltage			0.8	V
V_{IH}	High level input voltage		2.0		V
I_{IL}	Low level input current	$V_{IN} = GND$	-10		μA
I_{IH}	High level input current	$V_{IN} = V_{CC}$		10	μA
V_{OL4}	Low level output voltage for 4 mA outputs and I/O pins	$I_{OL} = 4 \text{ mA}$		0.4	V
V_{OH4}	High level output voltage for 4 mA outputs and I/O pins	$I_{OH} = -4 \text{ mA}$	2.4		V
I_{OZL}	Low level float input leakage	$V_{IN} = GND$	-10		μA
I_{OZH}	High level float input leakage	$V_{IN} = V_{CC}$		10	μA
I_{CC} (max.)	Maximum supply current	$V_{CC} = 3.6 \text{ V}$ $PCLK = LCLK = 33 \text{ MHz}$		55	mA
I_{CC} (typ.)	Typical supply current	$V_{CC} = 3.3 \text{ V}$ $PCLK = LCLK = 33 \text{ MHz}$		44	mA
C_{IO}	Input and output capacitance			10	pF

AC Characteristics

The AC characteristics for the PCI bus signals match those given in the *PCI Local Bus Specification*, Revision 2.1, Section 4.2.2.2. For more information on the PCI AC specifications, including the V/I curves for 3.3 V signalling, see the *PCI Local Bus Specification*.

PCI Bus Timings

Table 6: PCI Bus Signals AC Operating Specifications

Symbol	Parameter	Condition	Min.	Max.	Units
$I_{OH(AC)}$	Switching current high	$0 < V_{OUT} \leq 0.3 V_{CC}$	$-12 V_{CC}$		mA
		$0.3 V_{CC} < V_{OUT} < 0.9 V_{CC}$	$-17.1 (V_{CC} - V_{OUT})$		mA
		$0.7 V_{CC} < V_{OUT} < V_{CC}$		Equation C	
	(Test point)	$V_{OUT} = 0.7 V_{CC}$		$-32 V_{CC}$	mA
$I_{OL(AC)}$	Switching current low	$V_{CC} > V_{OUT} \geq 0.6 V_{CC}$	$16 V_{CC}$		mA
		$0.6 V_{CC} > V_{OUT} > 0.1 V_{CC}$	$26.7 V_{OUT}$		mA
		$0.18 V_{CC} > V_{OUT} > 0$		Equation D	
	(Test point)	$V_{OUT} = 0.18 V_{CC}$		$38 V_{CC}$	mA
I_{CL}	Low clamp current	$-3 < V_{IN} \leq -1$	$-25 + (V_{IN} + 1) / 0.015$		mA
I_{CH}	High clamp current	$V_{CC} + 4 > V_{IN} \geq V_{CC} + 1$	$25 + (V_{IN} - V_{CC} - 1) / 0.015$		mA
t_R	Unloaded output rise time	$0.2 V_{CC} - 0.6 V_{CC}$ load	1	4	V/ns
t_F	Unloaded output fall time	$0.6 V_{CC} - 0.2 V_{CC}$ load	1	4	V/ns

Local Bus Timings

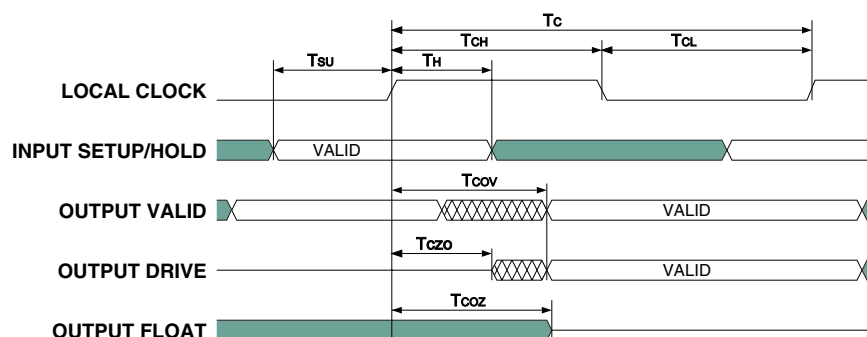
Table 7: Local Bus AC Test Conditions

Symbol	Parameter	Limits	Units
V_{CC}	Supply voltage, 3.3 V operation	3.0 to 3.60	V
V_{IN}	Input low and high voltages	0.4 and 2.0	V
C_{OUT}	Capacitive load on output and I/O pins	50	pF

Table 8: Capacitive Derating for Output and I/O Pins

Output Drive Limit	Supply Voltage	Derating
4 mA	3.3 V	+0.046 ns/pF for loads >50 pF

Figure 2: Clock and Synchronous Signals

Table 9: Local Bus Timing Parameters for $V_{CC} = 3.3\text{ V} \pm 10\%$

No.	Symbol	Description	Min.	Max.	Units
1	T_C	LCLK/MEMCLK period	20		ns
2	T_{CH}	LCLK/MEMCLK high time ^a	9		ns
3	T_{CL}	LCLK/MEMCLK low time ^b	9		ns
4	T_{SU}	Synchronous input setup ^c	6		ns
4a	T_{SU}	Synchronous input setup ($\overline{AS}/\overline{ADS}/\overline{LREQ}$)	4		ns
4b	T_{SU}	Synchronous input setup for HOLDA ($\overline{LBGRT}$)	3		ns
5	T_H	Synchronous input hold	2		ns
6	T_{COV}	LCLK/MEMCLK to output valid delay ^d	4	11	ns
6a	T_{COV}	LCLK/MEMCLK to output valid delay (address, data)	4	12	ns
7	T_{CZO}	LCLK/MEMCLK to output driving delay	4	11	ns
8	T_{COZ}	LCLK/MEMCLK to output float delay	4	11	ns
9	T_{RST}	Reset period when $\overline{LRST}$ used as input	16 T_C		ns

a. Measured at 1.5 V.

b. Measured at 1.5 V.

c. All local bus signals except those in 4a and 4b.

d. All local bus signals except those in 6a.

Table 10: PCI Bus Timing Parameters for $V_{CC} = 3.3\text{ V} \pm 10\%$

No.	Symbol	Description	Min.	Max.	Units
1	T_C	PCLK period	20		ns
2	T_{SU}	Synchronous input setup to PCLK ^a	7		ns
2a	T_{SU}	Synchronous input setup to PCLK ($\overline{GNT}$)	9		ns
3	T_H	Synchronous input hold from PCLK	0		ns
4	T_{COV}	PCLK to output valid delay ^b	3	11	ns
4a	T_{COV}	PCLK to output valid delay ($\overline{REQ}$)	3	12	ns
5	T_{CZO}	PCLK to output driving delay	3	11	ns
6	T_{COZ}	PCLK to output float delay	4	18	ns
7	T_{RST}	Reset period when PRST used as input	16 T_C		

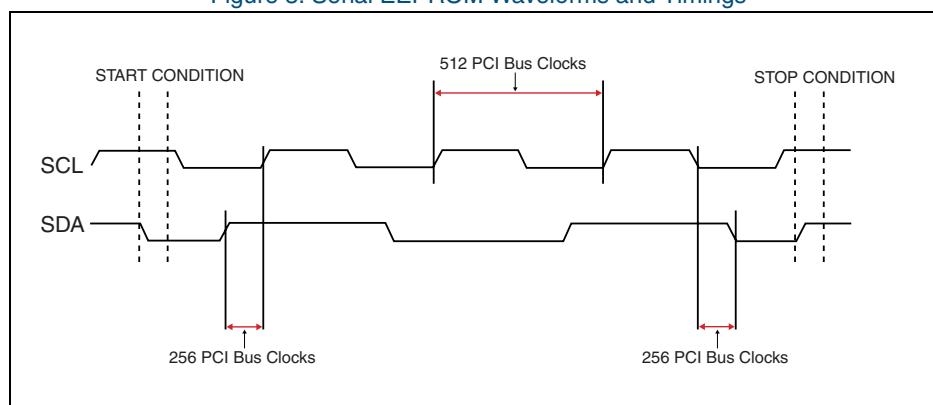
a. All PCI bus signals except those in 2a.

b. All PCI bus signals except those in 4a.

Serial EEPROM Port Timings

The clock for the serial EEPROM interface is derived by dividing the PCI bus clock. The waveforms generated are shown in **Figure 3**.

Figure 3: Serial EEPROM Waveforms and Timings



Pin Description

Table 11 lists the pin types found on the V363EPC. Together, **Table 12** and **Table 13** describe the function of each pin on the V363EPC. **Table 14** lists the RESET state for test mode pins.

Table 11: Pin Types

Pin Type	Description
PCI I	PCI input only pin.
PCI O	PCI output only pin.
PCI I/O	PCI tri-state I/O pin.
PCI I/O _D	PCI input with open drain output.
I/O ₄	TTL I/O pin with 4 mA output drive.
I	TTL input only pin.
O ₄	TTL output pin with 4 mA output drive.

Signal Description

Table 12: Signal Descriptions: Non-Processor Mode Dependent

Signal	Type	Reset State	Description
PCI Bus Interface Signals			
AD[31:0]	PCI I/O	Z	Address and Data multiplexed on the same pins.
C/ $\overline{\text{BE}}$ [3:0]	PCI I/O	Z	Bus Command and Byte Enables multiplexed on the same pins.
PAR	PCI I/O	Z	Parity represents even parity across AD[31:0] and C/ $\overline{\text{BE}}$ [3:0].
$\overline{\text{FRAME}}$	PCI I/O	Z	Cycle Frame indicates the beginning and burst length of an access.
$\overline{\text{IRDY}}$	PCI I/O	Z	Initiator Ready indicates the initiating agent's (bus master's) ability to complete the current data phase of the transaction.
$\overline{\text{TRDY}}$	PCI I/O	Z	Target Ready indicates the target agent's (selected device's) ability to complete the current data phase of the transaction.
$\overline{\text{STOP}}$	PCI I/O	Z	Stop indicates that the current target is requesting the master to stop the current transaction (retry or disconnect).
$\overline{\text{DEVSEL}}$	PCI I/O	Z	Device Select , when actively driven by a target, indicates the driving device has decoded its address as the target of the current access. As an input to the initiator, $\overline{\text{DEVSEL}}$ indicates whether any device on the bus has been selected.
IDSEL	PCI I		Initialization Device Select is used as a chip select during configuration read and write transactions. It must be driven high in order to access the chip's internal configuration space.
$\overline{\text{REQ}}$	PCI O	Z	Request indicates to the arbiter that this agent requests use of the bus.
$\overline{\text{GNT}}$	PCI I		Grant indicates to the agent that access to the bus has been granted.
PCLK	PCI I		PCI Clock provides timing for all transactions on the PCI bus.
$\overline{\text{PRST}}$	PCI I/O	Z/L	PCI Reset acts as an input when RDIR is high, an output when RDIR is low. As an input it is asserted low to bring all internal EPC operation to a reset state.
$\overline{\text{PERR}}$	PCI I/O	Z	Parity Error is used to report data parity errors during all PCI transactions except a Special Cycle.
$\overline{\text{SERR}}$	PCI I/OD	Z	System Error is used to report address parity errors, data parity errors on the Special Cycle command, or any other system error where the result will be catastrophic.
$\overline{\text{INT}}[\text{A:D}]$	PCI I/OD	Z	Interrupt is used to receive or generate level-sensitive interrupt requests.
Serial EEPROM Interface Signals			
SCL/ $\overline{\text{LPERR}}$	O ₄	X	EEPROM Clock, Local Parity Error.
SDA	I/O ₄	X	EEPROM Data.
Configuration Signal			
RDIR	I		Reset Direction: tie low to drive $\overline{\text{PRST}}$ out and $\overline{\text{LRST}}$ in; tie high to drive $\overline{\text{LRST}}$ out and $\overline{\text{PRST}}$ in.

Table 12: Signal Descriptions: Non-Processor Mode Dependent (Continued)

Signal	Type	Reset State	Description
Power and Ground Signals			
V _{CC}	—		Power leads for external connection to a 3.3 V V _{CC} board plane.
GND	—		Ground leads for external connection to a GND board plane.

Table 13: Signal Descriptions: Processor Mode Dependent

De-Multiplexed A/D		Multiplexed A/D		Type	Reset State	Description
AM29030/40	i960Cx/Hx	i960Jx	i960Sx			
ID[31:0]	LD[31:0]	LAD[31:0]	LAD[15:0]	I/O ₄	Z	De-multiplexed data bus. Multiplexed address and data bus.
LA[31:2]	LA[31:2]	LA[5:2]	LA[31:16] LA[5:2]	I/O ₄	Z	Address Bus LA[5:2] are output only in Multiplexed A/D mode.
$\overline{\text{BWE}}[3:0]$	$\overline{\text{BE}}[3:0]$	$\overline{\text{BE}}[3:0]$	$\overline{\text{BE}}[1:0]$	I/O ₄	Z	Byte Enables
R/ $\overline{\text{W}}$	W/ $\overline{\text{R}}$	W/ $\overline{\text{R}}$	W/ $\overline{\text{R}}$	I/O ₄	Z	Read-Write strobe.
—	—	ALE	ALE	I/O ₄	Z	Address Latch Enable
$\overline{\text{LREQ}}$	$\overline{\text{ADS}}$	$\overline{\text{ADS}}$	$\overline{\text{AS}}$	I/O ₄	Z	Address Strobe is asserted low to indicate the beginning of a bus cycle; interpreted as LREQ in AM29030/40 mode.
$\overline{\text{RDY}}$	$\overline{\text{READY}}$	$\overline{\text{RDYRCY}}$	$\overline{\text{READY}}$	I/O ₄	Z	Data Ready
$\overline{\text{LBREQ}}$	HOLD	HOLD	HOLD	O ₄	L ^a	Bus Mastership Request
$\overline{\text{LBGR}}\overline{\text{T}}$	HOLDA	HOLDA	HOLDA	I		Bus Mastership Grant
LPAR[3:0]	LPAR[3:0]	LPAR[3:0]	LPAR[1:0]	I/O ₄	Z	Data Parity
$\overline{\text{BURST}}$	$\overline{\text{BLAST}}$	$\overline{\text{BLAST}}$	$\overline{\text{BLAST}}$	I/O ₄	Z	$\overline{\text{BURST}}$: Burst Request $\overline{\text{BLAST}}$: Burst Last
$\overline{\text{ERR}}$	$\overline{\text{BTERM}}$	$\overline{\text{BTERM}}$	—	I/O ₄	Z	$\overline{\text{ERR}}$: Bus Time-out $\overline{\text{BTERM}}$: Burst Terminate
$\overline{\text{LINT}}$	$\overline{\text{LINT}}$	$\overline{\text{LINT}}$	$\overline{\text{LINT}}$	O ₄	H	Local Interrupt Request
$\overline{\text{LRST}}$	$\overline{\text{LRST}}$	$\overline{\text{LRST}}$	$\overline{\text{LRST}}$	I/O ₄	L/Z	Local Bus RESET
MEMCLK	LCLK	LCLK	LCLK	I		Local Bus Clock

a. The reset state is 'H' in AM29030/40 mode.

Test Mode Pins

Several device pins are used during the manufacturing test to put the V363EPC device into various test modes.

NOTE: These pins must be maintained at proper levels during reset to insure proper operation.

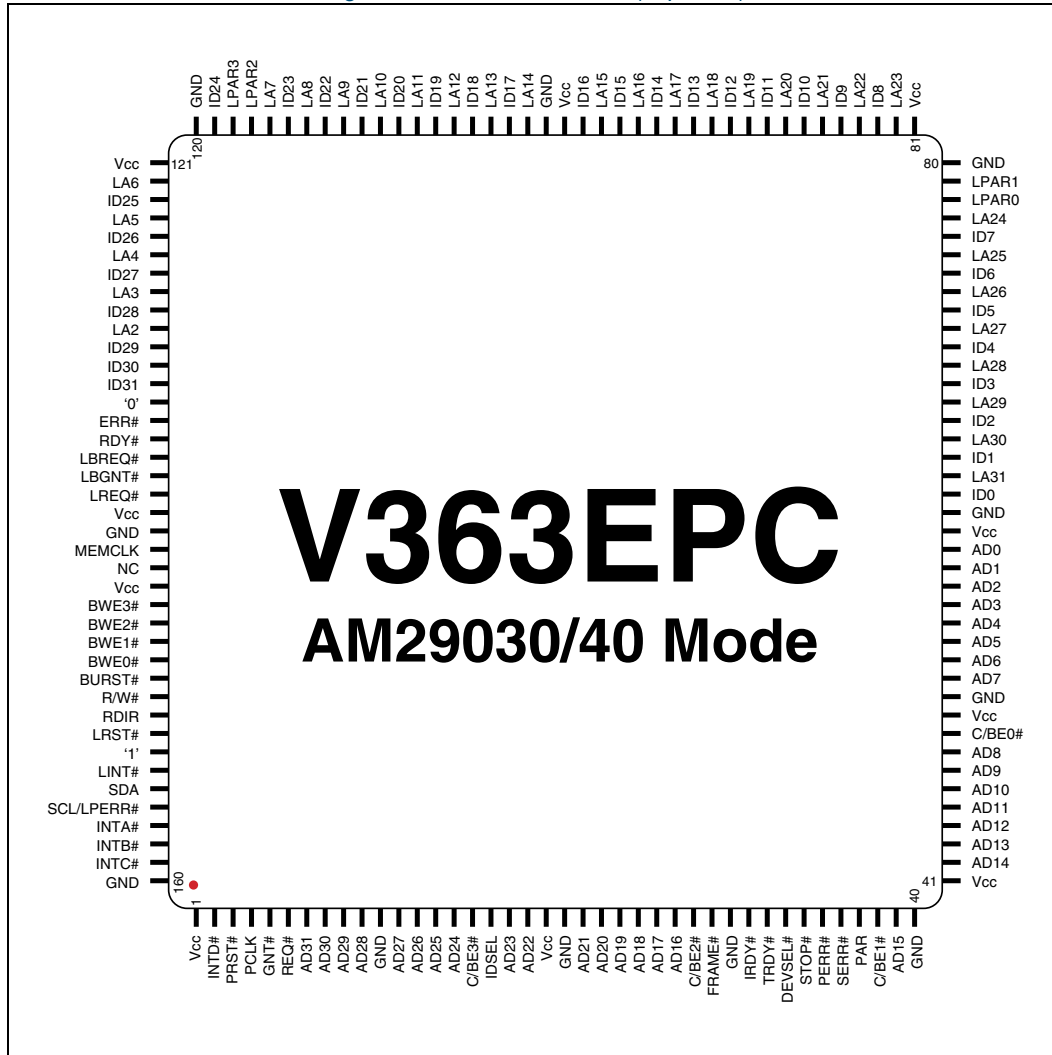
This is typically handled through pull-up or pull-down resistors (typically 1–10 k Ω) on the signal pins if they are not guaranteed to be at the proper level during reset. Table 5 shows the reset states for test mode pins.

Table 14: RESET State for Test Mode Pins

Mode	Pin 134	Pin 135	Pin 153
i960 Cx/Hx	Pull up	Pull up	Pull up
AMD 2930/40	Pull down	Pull up	Pull up
i960 Jx	Pull down	Pull up	Pull down
i960 Sx	Pull down	Pull down	Pull down

AM29030/40 Mode Pinout Diagram

Figure 4: AM29030/40 Mode (Top View)



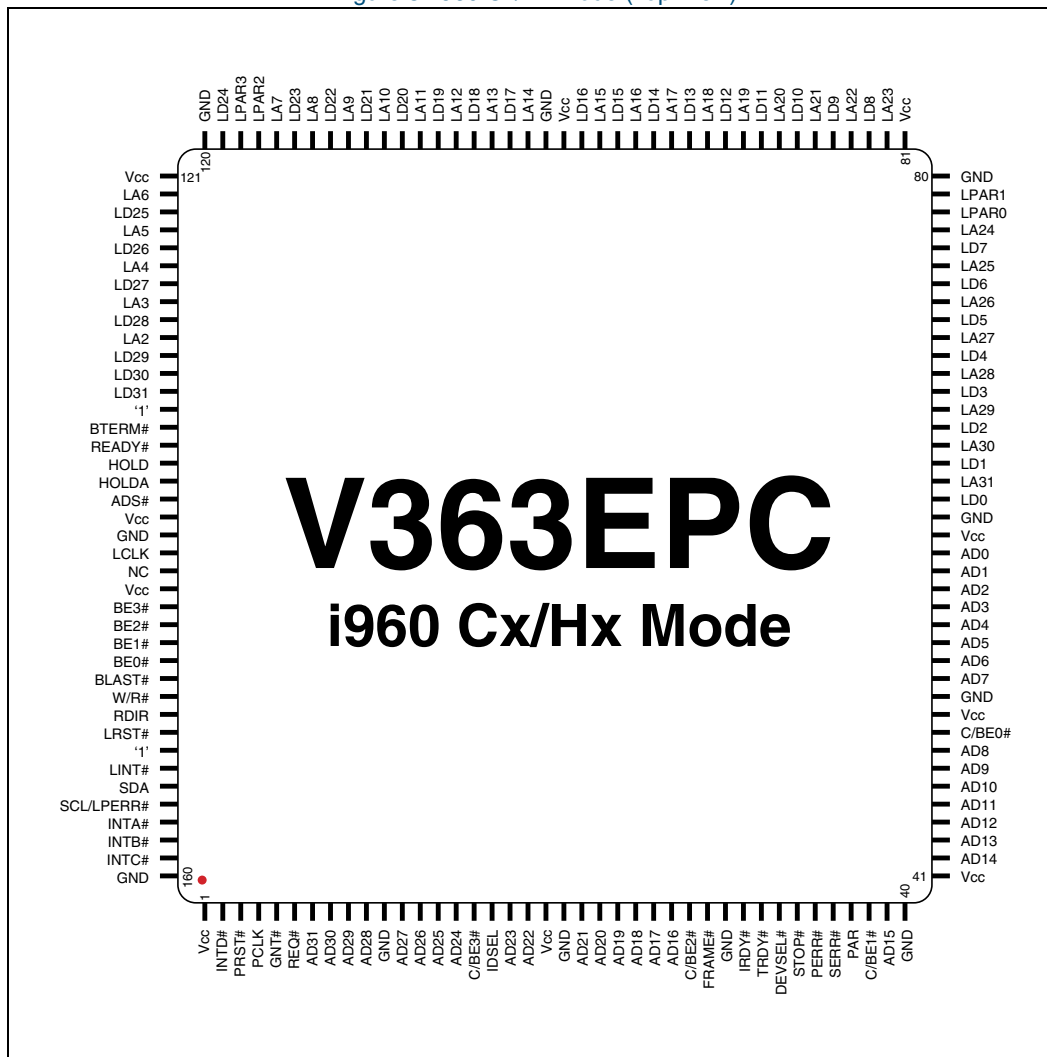
AM29030/40 Mode Pinout Table

Table 15: AM29030/40 Mode Pinout

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	VCC	41	VCC	81	VCC	121	VCC
2	INTD	42	AD14	82	LA23	122	LA6
3	PRST	43	AD13	83	ID8	123	ID25
4	PCLK	44	AD12	84	LA22	124	LA5
5	GNT	45	AD11	85	ID9	125	ID26
6	REQ	46	AD10	86	LA21	126	LA4
7	AD31	47	AD9	87	ID10	127	ID27
8	AD30	48	AD8	88	LA20	128	LA3
9	AD29	49	C/BE0	89	ID11	129	ID28
10	AD28	50	VCC	90	LA19	130	LA2
11	GND	51	GND	91	ID12	131	ID29
12	AD27	52	AD7	92	LA18	132	ID30
13	AD26	53	AD6	93	ID13	133	ID31
14	AD25	54	AD5	94	LA17	134	'0'
15	AD24	55	AD4	95	ID14	135	ERR
16	C/BE3	56	AD3	96	LA16	136	RDY
17	IDSEL	57	AD2	97	ID15	137	LBREQ
18	AD23	58	AD1	98	LA15	138	LBGNT
19	AD22	59	AD0	99	ID16	139	LREQ
20	VCC	60	VCC	100	VCC	140	VCC
21	GND	61	GND	101	GND	141	GND
22	AD21	62	ID0	102	LA14	142	MEMCLK
23	AD20	63	LA31	103	ID17	143	NC
24	AD19	64	ID1	104	LA13	144	VCC
25	AD18	65	LA30	105	ID18	145	BWE3
26	AD17	66	ID2	106	LA12	146	BWE2
27	AD16	67	LA29	107	ID19	147	BWE1
28	C/BE2	68	ID3	108	LA11	148	BWE0
29	FRAME	69	LA28	109	ID20	149	BURST
30	GND	70	ID4	110	LA10	150	R/W
31	IRDY	71	LA27	111	ID21	151	RDIR
32	TRDY	72	ID5	112	LA9	152	LRST
33	DEVSEL	73	LA26	113	ID22	153	'1'
34	STOP	74	ID6	114	LA8	154	LINT
35	PERR	75	LA25	115	ID23	155	SDA
36	SERR	76	ID7	116	LA7	156	SCL/LPERR
37	PAR	77	LA24	117	LPAR2	157	INTA
38	C/BE1	78	LPAR0	118	LPAR3	158	INTB
39	AD15	79	LPAR1	119	ID24	159	INTC
40	GND	80	GND	120	GND	160	GND

i960 Cx/Hx Mode Pinout Diagram

Figure 5: i960 Cx/Hx Mode (Top View)



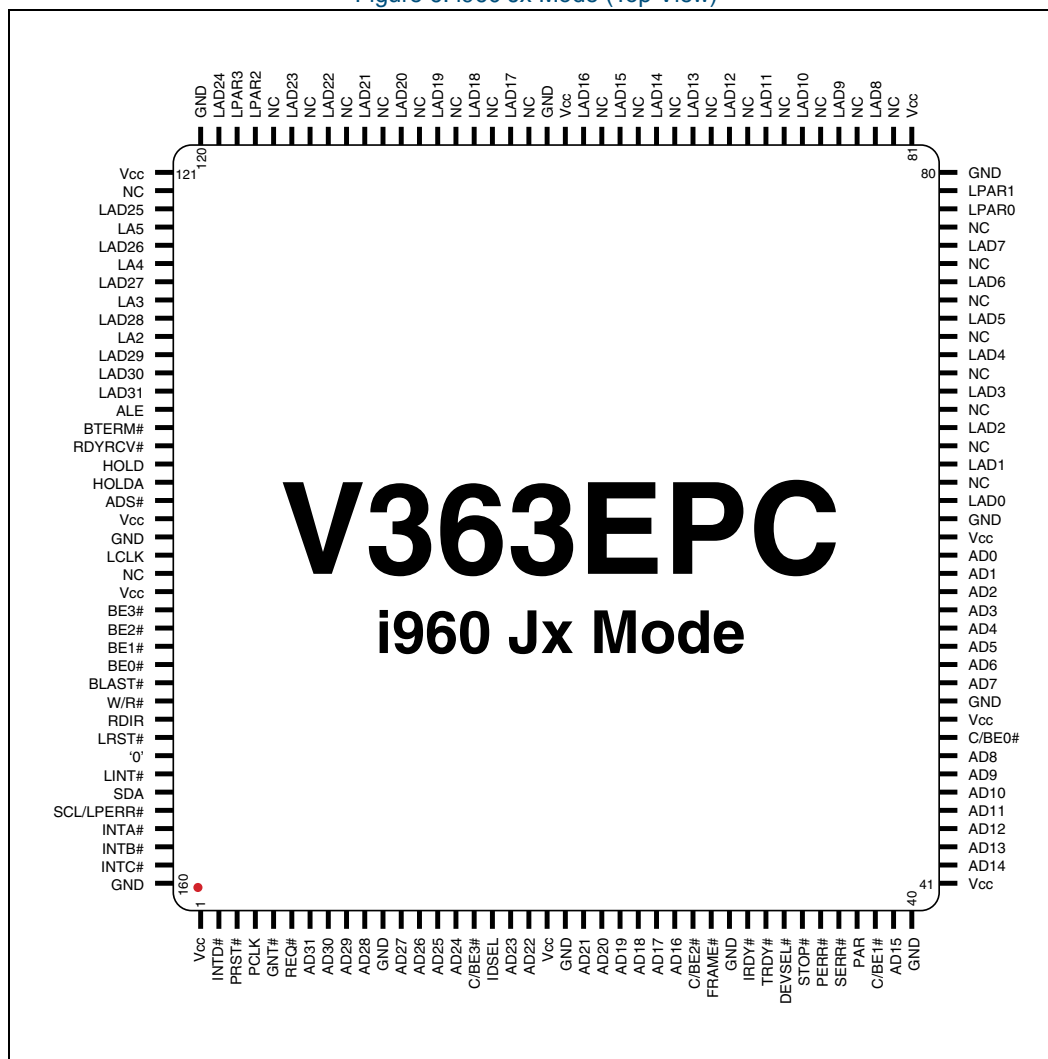
i960 Cx/Hx Mode Pinout Table

Table 16: i960 Cx/Hx Mode Pinout

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	VCC	41	VCC	81	VCC	121	VCC
2	INTD	42	AD14	82	LA23	122	LA6
3	PRST	43	AD13	83	LD8	123	LD25
4	PCLK	44	AD12	84	LA22	124	LA5
5	GNT	45	AD11	85	LD9	125	LD26
6	REQ	46	AD10	86	LA21	126	LA4
7	AD31	47	AD9	87	LD10	127	LD27
8	AD30	48	AD8	88	LA20	128	LA3
9	AD29	49	C/BE $\overline{0}$	89	LD11	129	LD28
10	AD28	50	V _{CC}	90	LA19	130	LA2
11	GND	51	GND	91	LD12	131	LD29
12	AD27	52	AD7	92	LA18	132	LD30
13	AD26	53	AD6	93	LD13	133	LD31
14	AD25	54	AD5	94	LA17	134	'1'
15	AD24	55	AD4	95	LD14	135	BTERM
16	C/BE $\overline{3}$	56	AD3	96	LA16	136	READY
17	IDSEL	57	AD2	97	LD15	137	HOLD
18	AD23	58	AD1	98	LA15	138	HOLDA
19	AD22	59	AD0	99	LD16	139	ADS
20	VCC	60	VCC	100	VCC	140	VCC
21	GND	61	GND	101	GND	141	GND
22	AD21	62	LD0	102	LA14	142	LCLK
23	AD20	63	LA31	103	LD17	143	NC
24	AD19	64	LD1	104	LA13	144	VCC
25	AD18	65	LA30	105	LD18	145	BE $\overline{3}$
26	AD17	66	LD2	106	LA12	146	BE $\overline{2}$
27	AD16	67	LA29	107	LD19	147	BE $\overline{1}$
28	C/BE $\overline{2}$	68	LD3	108	LA11	148	BE $\overline{0}$
29	FRAME	69	LA28	109	LD20	149	BLAST
30	GND	70	LD4	110	LA10	150	W/R
31	IRDY	71	LA27	111	LD21	151	RDIR
32	TRDY	72	LD5	112	LA9	152	LRST
33	DEVSEL	73	LA26	113	LD22	153	'1'
34	STOP	74	LD6	114	LA8	154	LINT
35	PERR	75	LA25	115	LD23	155	SDA
36	SERR	76	LD7	116	LA7	156	SCL/LPERR
37	PAR	77	LA24	117	LPAR2	157	INTA
38	C/BE $\overline{1}$	78	LPAR0	118	LPAR3	158	INTB
39	AD15	79	LPAR1	119	LD24	159	INTC
40	GND	80	GND	120	GND	160	GND

i960 Jx Mode Pinout Diagram

Figure 6: i960 Jx Mode (Top View)



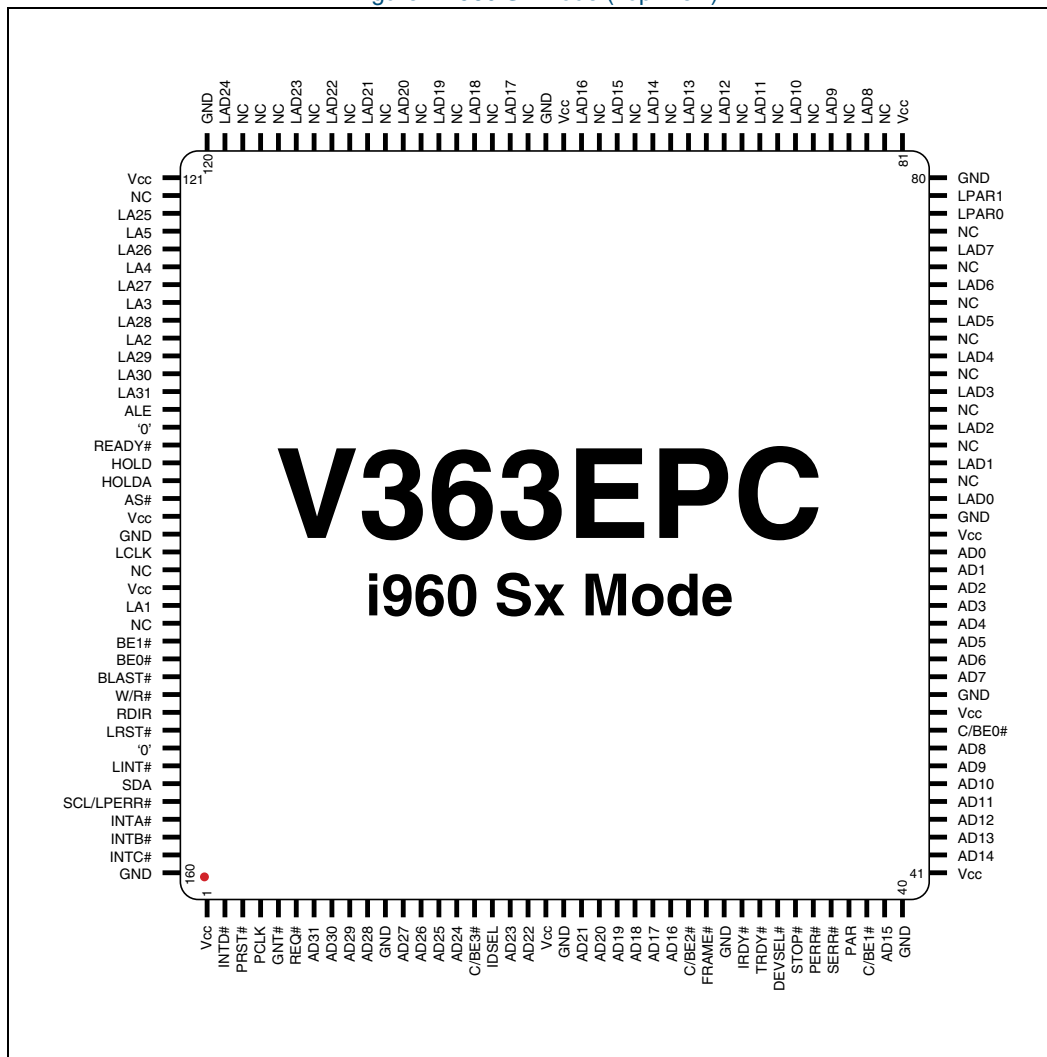
i960 Jx Mode Pinout Table

Table 17: i960 Jx Mode Pinout

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	VCC	41	VCC	81	VCC	121	VCC
2	INTD	42	AD14	82	NC	122	NC
3	PRST	43	AD13	83	LAD8	123	LAD25
4	PCLK	44	AD12	84	NC	124	LA5
5	GNT	45	AD11	85	LAD9	125	LAD26
6	REQ	46	AD10	86	NC	126	LA4
7	AD31	47	AD9	87	LAD10	127	LAD27
8	AD30	48	AD8	88	NC	128	LA3
9	AD29	49	C/BE0	89	LAD11	129	LAD28
10	AD28	50	VCC	90	NC	130	LA2
11	GND	51	GND	91	LAD12	131	LAD29
12	AD27	52	AD7	92	NC	132	LAD30
13	AD26	53	AD6	93	LAD13	133	LAD31
14	AD25	54	AD5	94	NC	134	ALE
15	AD24	55	AD4	95	LAD14	135	BTERM
16	C/BE3	56	AD3	96	NC	136	RDYRCV
17	IDSEL	57	AD2	97	LAD15	137	HOLD
18	AD23	58	AD1	98	NC	138	HOLDA
19	AD22	59	AD0	99	LAD16	139	ADS
20	VCC	60	VCC	100	VCC	140	VCC
21	GND	61	GND	101	GND	141	GND
22	AD21	62	LAD0	102	NC	142	LCLK
23	AD20	63	NC	103	LAD17	143	NC
24	AD19	64	LAD1	104	NC	144	VCC
25	AD18	65	NC	105	LAD18	145	BE3
26	AD17	66	LAD2	106	NC	146	BE2
27	AD16	67	NC	107	LAD19	147	BE1
28	C/BE2	68	LAD3	108	NC	148	BE0
29	FRAME	69	NC	109	LAD20	149	BLAST
30	GND	70	LAD4	110	NC	150	W/R
31	IRDY	71	NC	111	LAD21	151	RDIR
32	TRDY	72	LAD5	112	NC	152	LRST
33	DEVSEL	73	NC	113	LAD22	153	'0'
34	STOP	74	LAD6	114	NC	154	LINT
35	PERR	75	NC	115	LAD23	155	SDA
36	SERR	76	LAD7	116	NC	156	SCL/LPERR
37	PAR	77	NC	117	LPAR2	157	INTA
38	C/BE1	78	LPAR0	118	LPAR3	158	INTB
39	AD15	79	LPAR1	119	LAD24	159	INTC
40	GND	80	GND	120	GND	160	GND

i960 Sx Mode Pinout Diagram

Figure 7: i960 Sx Mode (Top View)



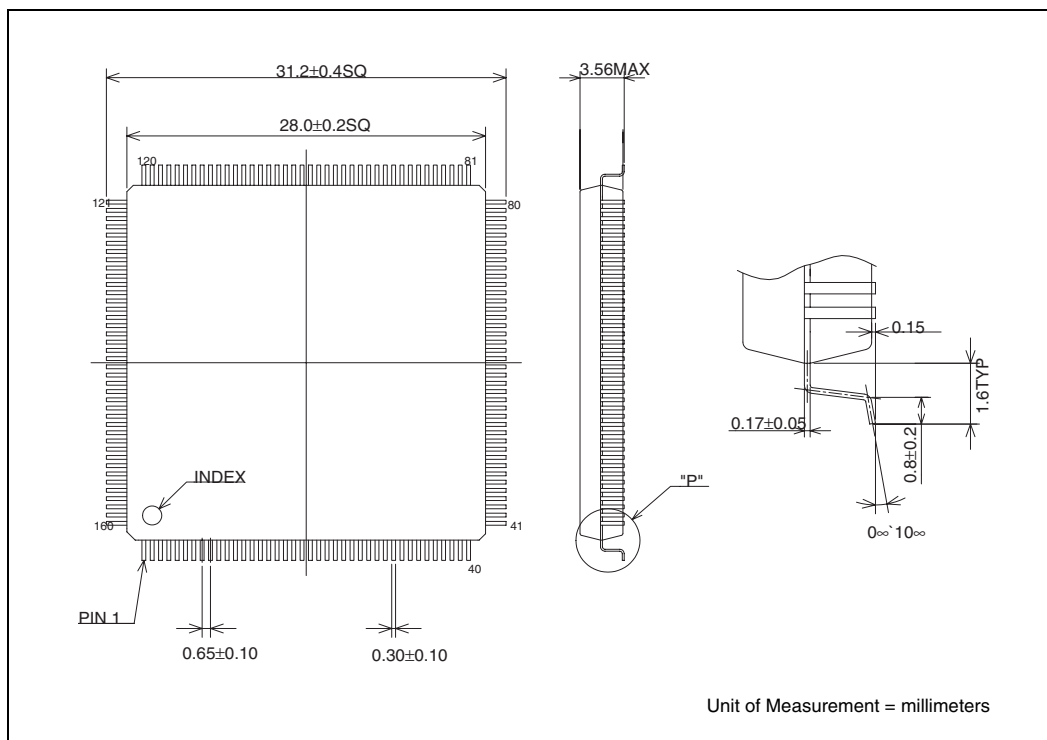
i960 Sx Mode Pinout Table

Table 18: i960 Sx Mode Pinout

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	VCC	41	VCC	81	VCC	121	VCC
2	INTD	42	AD14	82	NC	122	NC
3	PRST	43	AD13	83	LAD8	123	LA25
4	PCLK	44	AD12	84	NC	124	LA5
5	GNT	45	AD11	85	LAD9	125	LA26
6	REQ	46	AD10	86	NC	126	LA4
7	AD31	47	AD9	87	LAD10	127	LA27
8	AD30	48	AD8	88	NC	128	LA3
9	AD29	49	C/BE0	89	LAD11	129	LA28
10	AD28	50	VCC	90	NC	130	LA2
11	GND	51	GND	91	LAD12	131	LA29
12	AD27	52	AD7	92	NC	132	LA30
13	AD26	53	AD6	93	LAD13	133	LA31
14	AD25	54	AD5	94	NC	134	ALE
15	AD24	55	AD4	95	LAD14	135	'0'
16	C/BE3	56	AD3	96	NC	136	READY
17	IDSEL	57	AD2	97	LAD15	137	HOLD
18	AD23	58	AD1	98	NC	138	HOLDA
19	AD22	59	AD0	99	LA16	139	AS
20	VCC	60	VCC	100	VCC	140	VCC
21	GND	61	GND	101	GND	141	GND
22	AD21	62	LAD0	102	NC	142	LCLK
23	AD20	63	NC	103	LA17	143	NC
24	AD19	64	LAD1	104	NC	144	VCC
25	AD18	65	NC	105	LA18	145	LA1
26	AD17	66	LAD2	106	NC	146	NC
27	AD16	67	NC	107	LA19	147	BE1
28	C/BE2	68	LAD3	108	NC	148	BE0
29	FRAME	69	NC	109	LA20	149	BLAST
30	GND	70	LAD4	110	NC	150	W/R
31	IRDY	71	NC	111	LA21	151	RDIR
32	TRDY	72	LAD5	112	NC	152	LRST
33	DEVSEL	73	NC	113	LA22	153	'0'
34	STOP	74	LAD6	114	NC	154	LINT
35	PERR	75	NC	115	LA23	155	SDA
36	SERR	76	LAD7	116	NC	156	SCL/LPERR
37	PAR	77	NC	117	NC	157	INTA
38	C/BE1	78	LPAR0	118	NC	158	INTB
39	AD15	79	LPAR1	119	LA24	159	INTC
40	GND	80	GND	120	GND	160	GND

Package Mechanical Drawing

160-pin EIAJ PQFP Packaging Drawing



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Revision History

Revision	Date	Originator and Comments
1.01	10/00	Updated power consumption & θ_{JC} .
1.00	07/00	Preliminary presilicon revision of data sheet.
C	October 2005	Mehul Kochar and Kathleen Murchek Updated Product Code table to include item V363EPC-50LPN REV A0. General Edit and reformat.
D	November 2005	Mehul Kochar and Kathleen Murchek Added footnote that product code item V363EPC-50LPN REV A0 is lead-free.

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