

MN65752H

Low Power 8-Bit, 2-Channel CMOS A/D Converter for Image Processing

Overview

The MN65752H is an 8-bit, 2-channel CMOS analog-to-digital converter for image processing applications.

It uses a half flash structure based on chopper comparators and achieves both high speed and low power consumption with multiplexing.

It provides separate power supply pins for the circuits driving the low-voltage digital output pins.

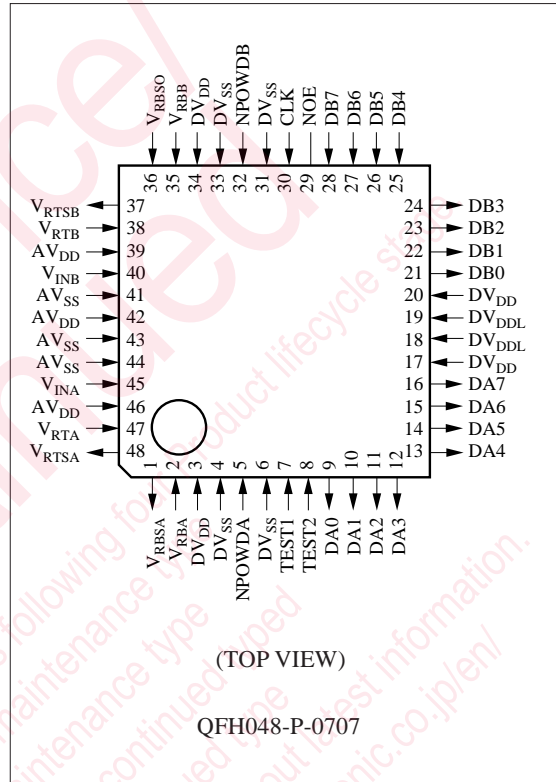
Features

- Maximum conversion rate: 20 MSPS (min.)
- Linearity error: ± 0.9 LSB (typ.)
- Differential linearity error: ± 0.5 LSB (typ.)
- Power supply voltage: 3.6 V or 2.6 V
- Power consumption: 50 mW (typ.) ($f_{CLK}=16$ MHz)

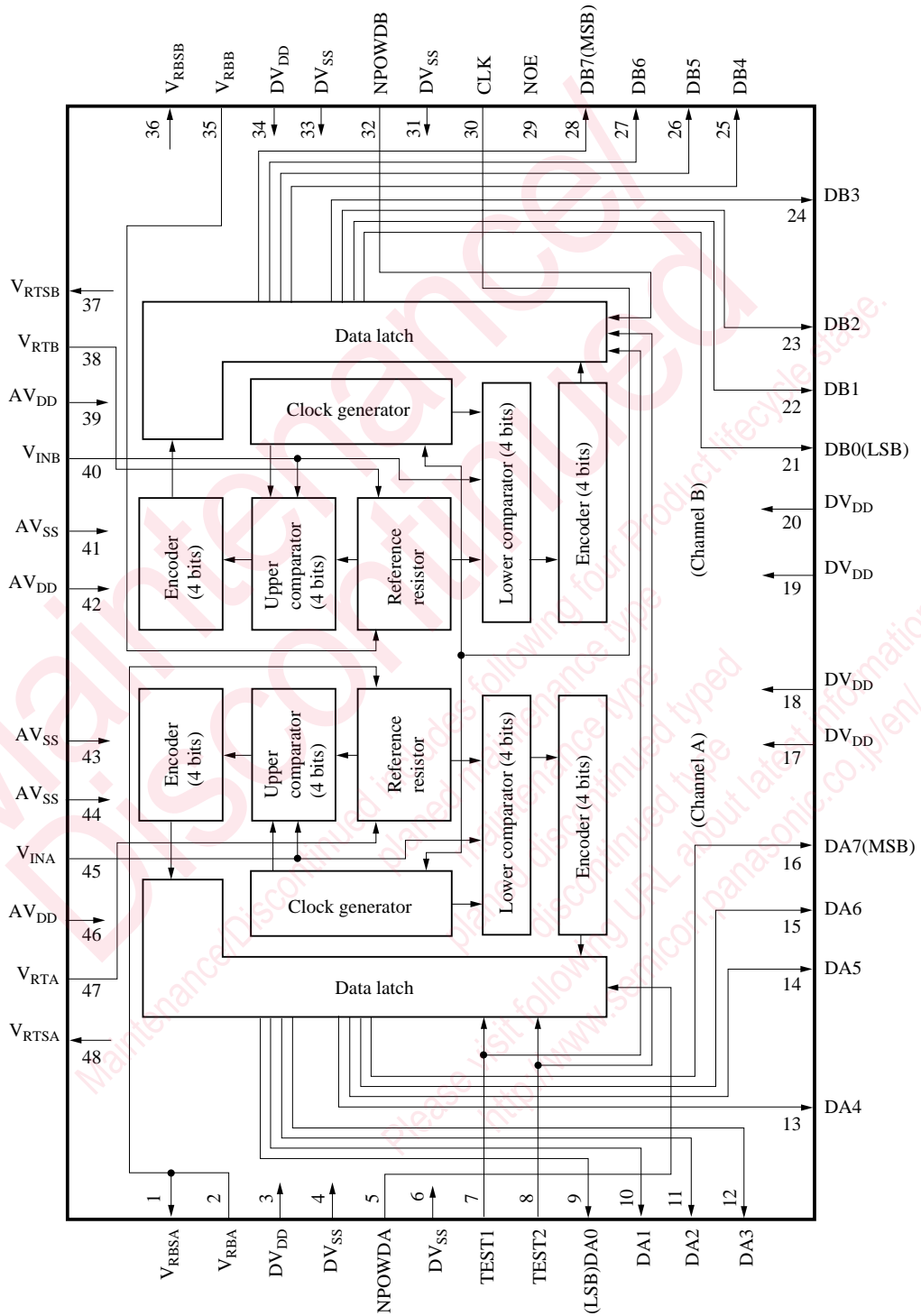
Applications

- Digital television receivers
- Digital video equipment
- Digital image processing equipment

Pin Assignment



■ Block Diagram



■ Pin Descriptions

Pin No.	Symbol	Function Description
1	V _{RBSA}	Reference voltage power supply (BOTTOM)
2	V _{RBA}	Reference voltage input (BOTTOM)
3	DV _{DD}	Power supply for digital circuits
4	DV _{SS}	Ground for digital circuits
5	NPOWDA	Power down mode selection
6	DV _{SS}	Ground for digital circuits
7	TEST1	Test mode selection
8	TEST2	Test mode selection
9	DA0	Digital code output (LSB)
10	DA1	Digital code output
11	DA2	Digital code output
12	DA3	Digital code output
13	DA4	Digital code output
14	DA5	Digital code output
15	DA6	Digital code output
16	DA7	Digital code output (MSB)
17	DV _{DD}	Power supply for digital circuits
18	DV _{DDL}	Power supply for low-voltage digital outputs
19	DV _{DDL}	Power supply for low-voltage digital outputs
20	DV _{DD}	Power supply for digital circuits
21	DB0	Digital code output (LSB)
22	DB1	Digital code output
23	DB2	Digital code output
24	DB3	Digital code output
25	DB4	Digital code output
26	DB5	Digital code output
27	DB6	Digital code output
28	DB7	Digital code output (MSB)
29	NOE	Digital output enable
30	CLK	Sampling clock
31	DV _{SS}	Ground for digital circuits
32	NPOWDB	Power down mode selection
33	DV _{SS}	Ground for digital circuits
34	DV _{DD}	Power supply for digital circuits
35	V _{RBB}	Reference voltage input (BOTTOM)
36	V _{RBSB}	Reference voltage power supply (BOTTOM)
37	V _{RTSB}	Reference voltage power supply (TOP)
38	V _{RTB}	Reference voltage input (TOP)
39	AV _{DD}	Power supply for analog circuits
40	V _{INB}	Ground for analog circuits

■ Pin Descriptions (continued)

Pin No.	Symbol	Function Description
41	AV _{SS}	Ground for analog circuits
42	AV _{DD}	Power supply for analog circuits
43	AV _{SS}	Ground for analog circuits
44	AV _{SS}	Ground for analog circuits
45	V _{INA}	Analog signal input
46	AV _{DD}	Power supply for analog circuits
47	V _{RTA}	Reference voltage input (TOP)
48	V _{RTSA}	Reference voltage power supply (TOP)

■ Absolute Maximum Ratings $T_a=25^\circ\text{C}$

Parameter	Symbol	Rating	Unit
Power supply voltage	V _{DD}	-0.3 to +7.0	V
Power supply voltage for digital output circuits	DV _{DDL}	-0.3 to V _{DD} +0.3	V
Input voltage	V _I	-0.3 to V _{DD} +0.3	V
Output voltage	V _O	-0.3 to V _{DD} +0.3	V
Operating ambient temperature	T _{opr}	-20 to +70	°C
Storage temperature	T _{stg}	-55 to +125	°C

■ Recommended Operating Conditions $V_{DD}=AV_{DD}=DV_{DD}=3.6\text{V}$, $DV_{DDL}=2.6\text{V}$, $V_{SS}=AV_{SS}=DV_{SS}=0\text{V}$, $T_a=25^\circ\text{C}$

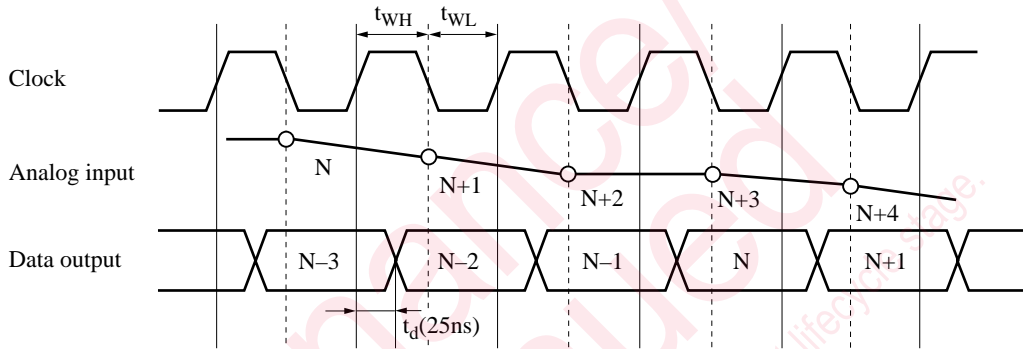
Parameter	Symbol	min	typ	max	Unit
Power supply voltage	V _{DD}	3.30	3.60	5.25	V
Power supply voltage for digital output circuits	DV _{DDL}	2.50	2.60	5.25	V
Digital input voltage	"H" level	V _{IH}	V _{DD} × 0.55	V _{DD}	V
	"L" level	V _{IL}	V _{SS}	V _{DD} × 0.2	V
Reference voltage	"H" level	V _{RT}	2.80	V _{DD}	V
	"L" level	V _{RB}	V _{SS}	1.30	V
Clock	"H" level pulse width	t _{WH}	20		ns
	"L" level pulse width	t _{WL}	20		ns
Analog input voltage	V _{AIN}	V _{SS}		V _{DD}	V

■ Electrical Characteristics $V_{DD}=AV_{DD}=DV_{DD}=3.6\text{V}$, $DV_{DDL}=2.6\text{V}$, $AV_{SS}=DV_{SS}=0\text{V}$, $T_a=25^\circ\text{C}$

Parameter	Symbol	Conditions	min	typ	max	Unit
Power consumption	P _C	f _{CLK} = 16 MSPS (not including reference current)		50	90	mW
Resolution	RES			8		bit
Linearity error	E _L	f _{CLK} =20MSPS		±0.9	±1.8	LSB
Differential linearity error	E _D	V _{RT} =2.8V, V _{RB} =1.3V		±0.5	±1.0	LSB
Maximum conversion rate	F _{C(max.)}		20			MSPS
Clock frequency	f _{CLK}		1		20	MHz
Analog input dynamic range	D _R		1.5		V _{RT} -V _{RB}	V
Output current	"H" level	I _{OH}	V _{OH} =DV _{DDL} -0.8V		-1.5	mA
	"L" level	I _{OL}	V _{OL} =0.4V	1.5		mA
Output delay time	t _d	C _L =20pF	10	25	40	ns
Analog input capacitance	C _I			15		pF

■ Timing Chart

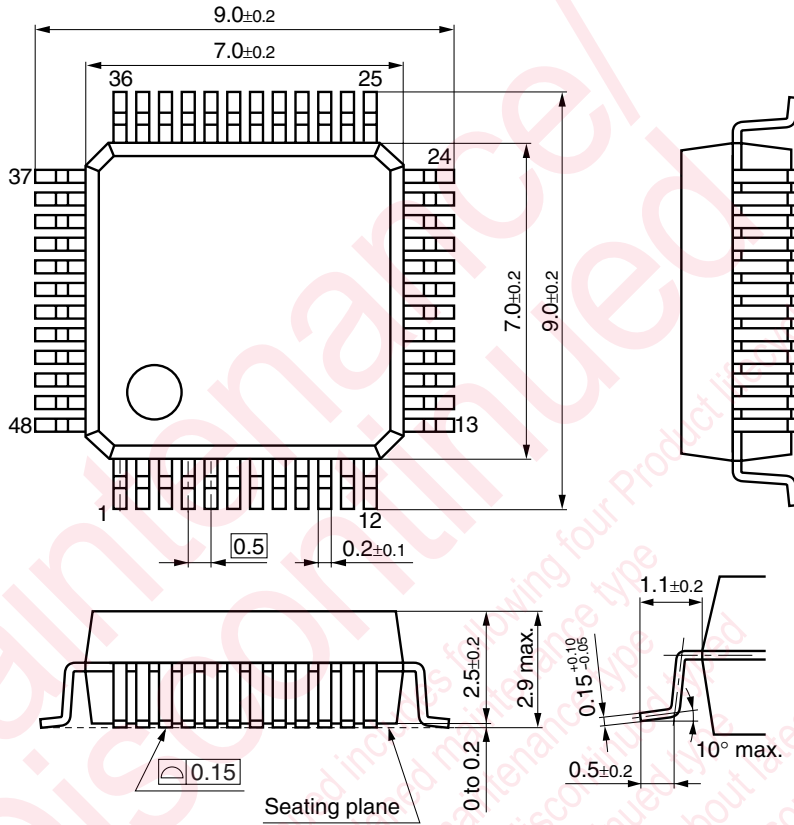
The chip samples the analog input at the falling edge of the clock signal and provides the corresponding digital output 2.5 clock cycles later at the rising edge of the clock signal.



Note: The circles indicate analog signal sampling points.

■ Package Dimensions (Unit:mm)

QFH048-P-0707



Note) The package of this product will be changed to the following lead-free type (QFH048-P-0707B).

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