NEC
ELECTRON DEVICE

MOS INTEGRATED CIRCUIT
μPD6131

MSK REMOTE CONTROL TRANSMITTING/RECEIVING IC
CMOS IC

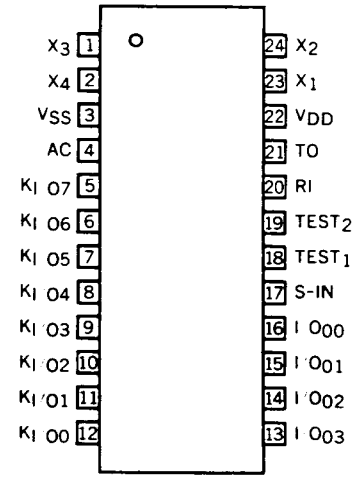
The μPD6131 is a remote control IC which transmits and receives by using MSK (minimum shift keying) signals.

It consists of a 1k-step (10 bits/step) ROM, 32-word RAM (5 bits/word), 4-bit parallel processing ALU, MSK signal generation circuit, receiving circuit, key I/O port, transmission output port, and receiving input port. Each function can be extended by programming.

FEATURES

- MSK system bi-directional remote control IC
- 19 kinds of instructions
- Instruction cycle
  17.4 μs/460.8 kHz (ceramic oscillator)
- Program memory capacity (ROM)
  1 024 x 10 bits
- Data memory capacity (RAM)
  32 x 5 bits
- MSK signal generation circuit/built-in receiving circuit
- I/O: 12 lines
  Serial input pin: 1
- Transmit data output format (MSK signal)
  9 level D/A output
- Built-in SCF circuit (low-pass filter)
- Stand-by operation (HALT)
- Built-in system clock ceramic oscillation circuit
- CMOS
- Low power consumption
- Low voltage operation assurance (2.2 to 6.0 V)

PIN CONFIGURATION (Top View)

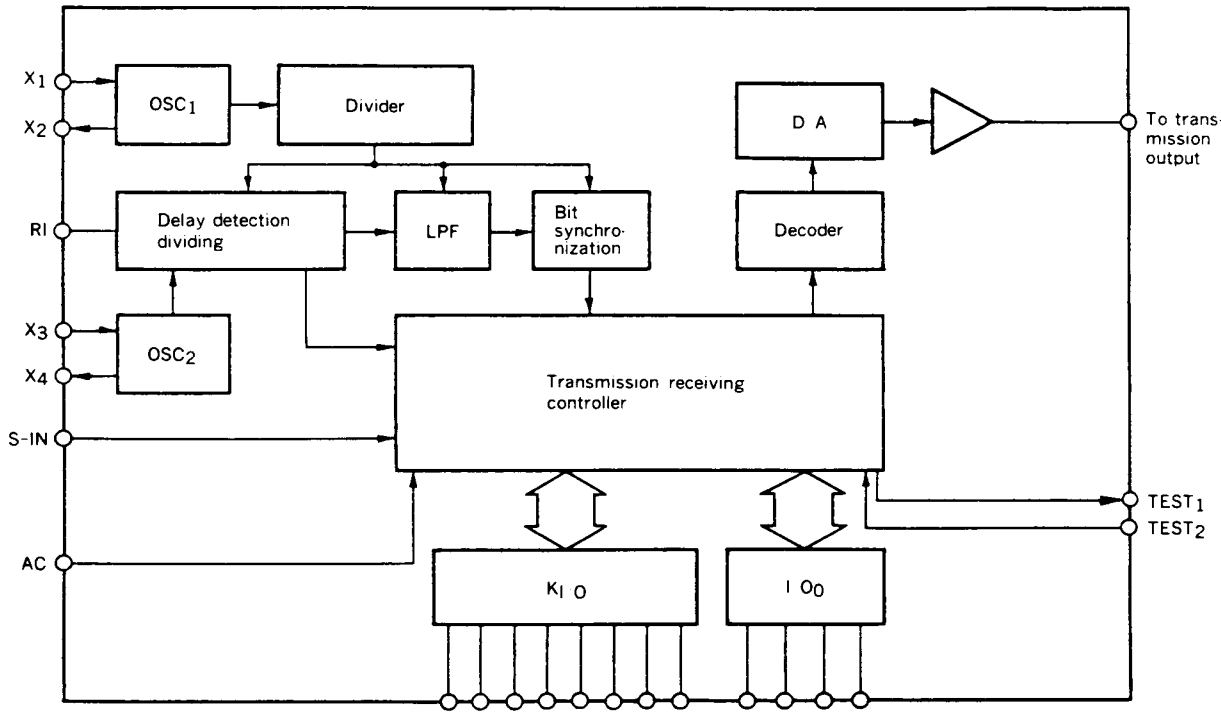


ORDERING INFORMATION

Order Code	Package
μPD6131GT	24-pin plastic SOP (375 mil)
μPD6131CS	24-pin shrink (300 mil)

Document No. IC-2516
(O. D. No. ID-7690)
Date Published September 1989 M
Printed in Japan

BLOCK DIAGRAM



1. INTERNAL BLOCK FUNCTION

1.1 Program Counter (PC): 10 Bits

The program counter is a 10-bit binary counter for holding 10-bit address information in the program memory.

Fig. 1-1 Program Counter Configuration

PC_9	PC_8	PC_7	PC_6	PC_5	PC_4	PC_3	PC_2	PC_1	PC_0	PC

When an instruction is executed, the program counter is normally incremented automatically according to the number of bytes in that instruction.

When jump instructions (JMP0, JC, and JF) are executed, a destination is indicated.

Immediate data and contents of the data memory are loaded to all or part of the PCs.

When a call instruction (CALL0) is executed, the content of the PCs used at that time is incremented, saved in the stack memory, and the values needed for each jump instruction are loaded.

When a return instruction (RET) is executed, the content of the stack memory is incremented by two and loaded in the PCs. When All Clear is input, all PCs are initialized to "000".

1.2 Stack Pointer (SP): 2 Bits

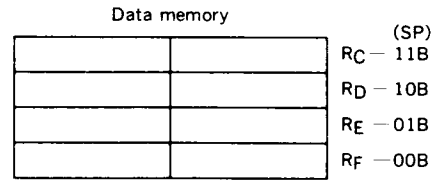
When the data memory is used as a stack memory, a 2-bit register called the stack pointer (SP) is used to hold the start address of the stack area.

The SP is incremented during execution of a call instruction (CALL0) and decremented for execution of a return instruction (RET).

The stack pointer is initialized to "00B" after ALL Clear is input, and specifies the highest order address "FH" as a stack area.

The figure below shows the relationship between the stack pointer and data memory area.

Data memory:



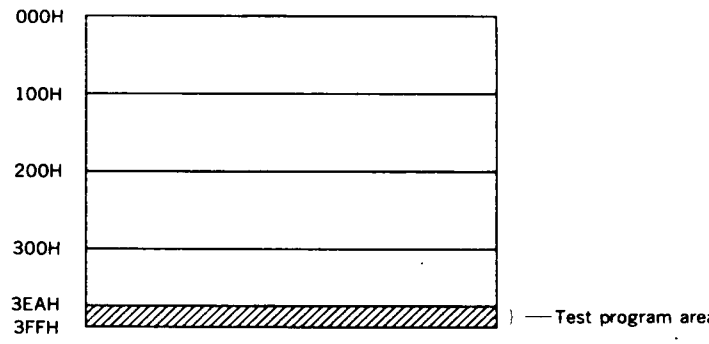
When the stack pointer overflows, the CPU has overrun, so the PC is initialized to "000".

1.3 Program Memory (POM): 1 024 Steps x 10 Bits

The program memory consists of 1 024 steps x 10 bits of mask programmable ROM. It is addressed by the program counter.

The program memory stores programs and table data.

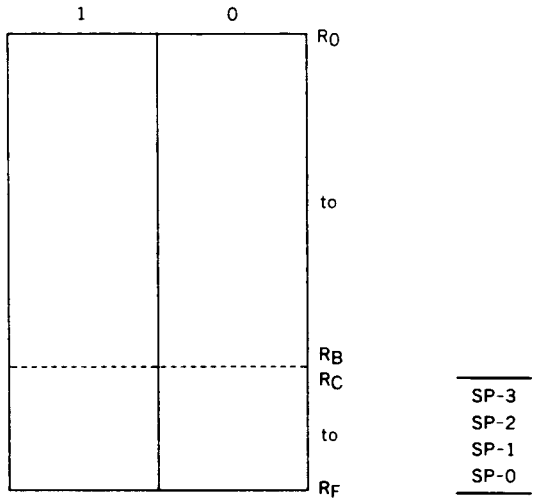
Fig. 1-2 Program Memory Map



1.4 Data Memory (RAM): 32 Words x 5 Bits

The data memory consists of 32 words x 5 bits of static RAM used for storing processing data. The data memory may be processed every eight bits. R_0 is available as a ROM data pointer.

Fig. 1-3 Data Memory Configuration



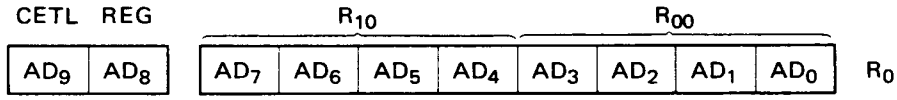
1.5 Data Pointer (R_0)

The data memory R_0 (R_{10}, R_{00}) serves as a ROM data pointer.

The R_0 specifies eight low order bits of ROM address and the control register specifies two high order bits.

Setting the ROM address in the data pointer and calling the contents of ROM allows the ROM data table to be easily referenced.

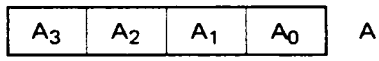
Fig. 1-4 Data Pointer Configuration



1.6 Accumulator (A): 4 Bits

The accumulator is 4-bit register. It serves as the heart of each arithmetic function.

Fig. 1-5 Accumulator Configuration



1.7 Arithmetic Logical Unit (ALU): 4 Bits

The arithmetic logical unit is a 4-bit arithmetic circuit which executes simple processing, mainly logical operation.

1.8 Flag

(1) Status flag

When each port status is checked by the STTS command and that status matches the conditions specified in the STTS command, the status flag (F) is set.

(2) Carry flag

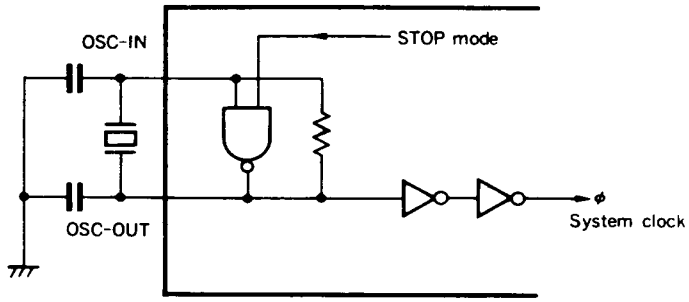
When the INC (increment) instruction or RL (rotate left) instruction is executed and a carry is generated at MSB of the accumulator, the carry flag (C) is set.

When the SCAF command is executed and the content of the accumulator is "FH", the carry flag (C) is set.

1.9 System Clock Generation Circuit

The system clock generation circuit is the oscillation circuit for the ceramic oscillator (400 to 500 kHz).

Fig. 1-6 System Clock Generation Circuit

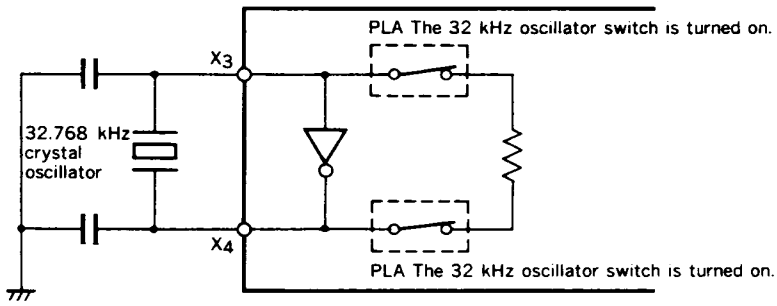


In the system clock generation circuit, the oscillation circuit and system clock ϕ stop in STOP mode (HALT under the condition of oscillation stop).

1.10 Subclock Generation Circuit

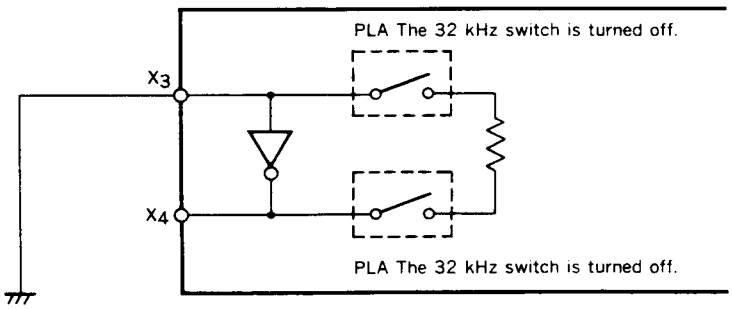
The subclock generation circuit consists of the 32.768 kHz crystal oscillation circuit.

Fig. 1-7 Subclock Generation Circuit



In the subclock generation circuit, whether the 32.768 kHz oscillator is set or not can be selected with the PLA data. When the 32.768 kHz oscillator is not set, set the pin X_3 (OSC-IN) to V_{DD} or V_{SS}.

Fig. 1-8 Subclock Generation Circuit



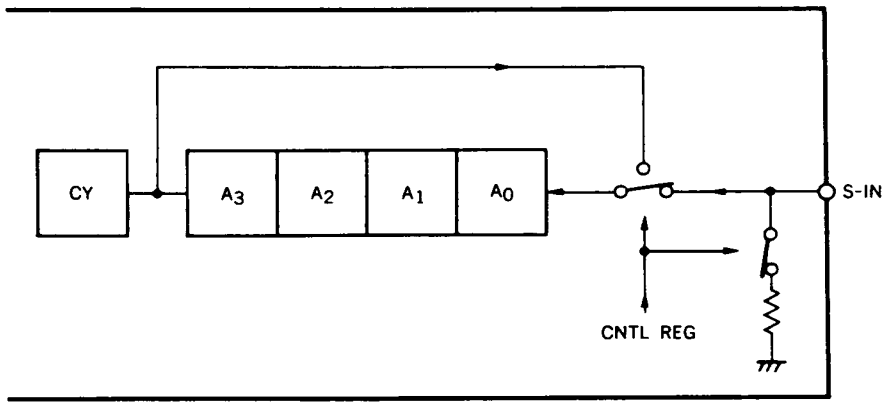
1.11 Serial Input Port

Use the serial input port to input serial data. When the control register (P1) is set to serial input mode, the serial input port is connected as the accumulator LSB input and is pulled down to the V_{SS} level inside the LSI. If the left shift command of the accumulator is executed under such a condition, the serial input port data is obtained by the accumulator LSB.

When the control register setting is released from serial input mode, the impedance of the serial input pin becomes high.

When the left shift command of the accumulator is executed, MSB data is input to the LSB.

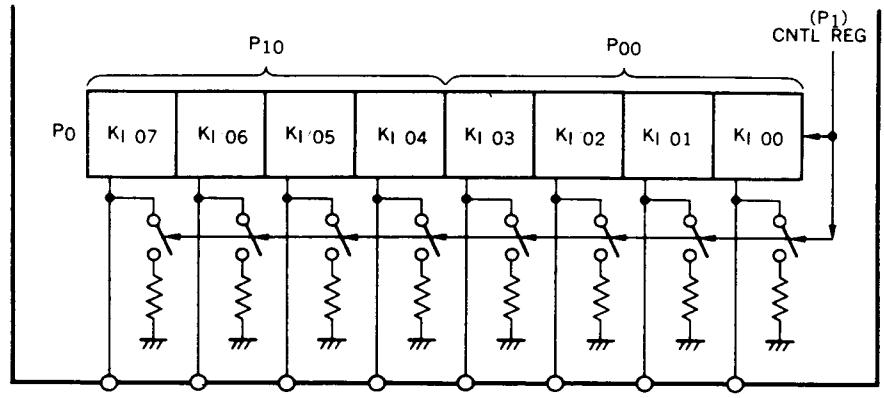
Fig. 1-9 Serial Input Port Configuration Diagram



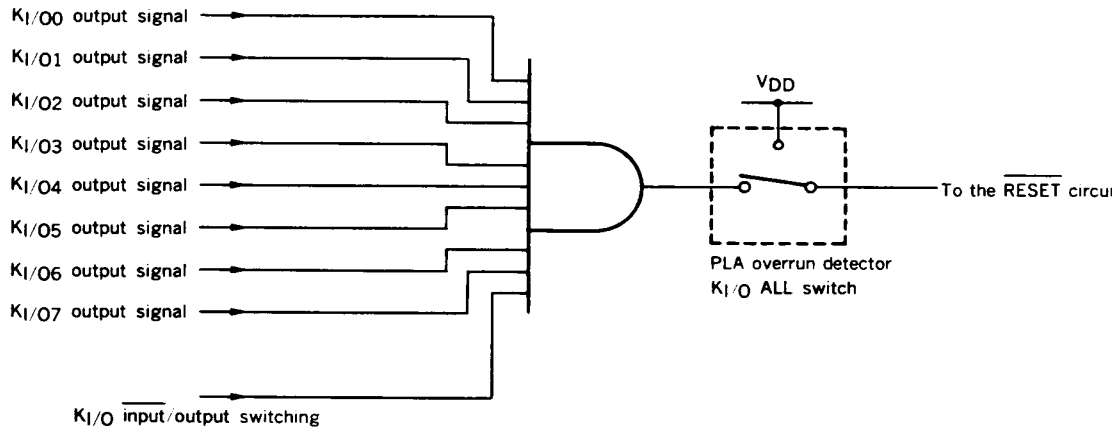
1.12 $K_{I/O}$ Port (P_0)

This is an 8-bit port for key scan output. Use it as an 8-bit input port by setting the control register (P_1) to input mode. When the control register is set to input mode, all the pins are pulled down to the V_{SS} level in the LSI.

Fig. 1-10 $K_{I/O}$ Port Configuration



1.13 Overrun Detection $K_{I/O}$ All Configuration Diagram



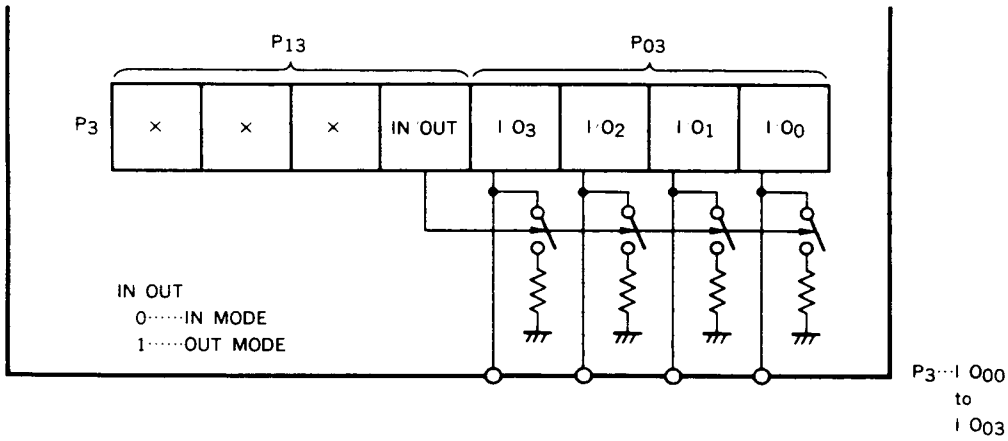
When the overrun detection $K_{I/O}$ ALL switch is turned on ("1" is set) with the PLA data, and the $K_{I/O}$ pin is set to input mode in oscillation stop HALT mode, or either $K_{I/O}$ pin goes low level, the switch is reset.

When using this pin as a source of the switch, turn on the switch with the PLA data.

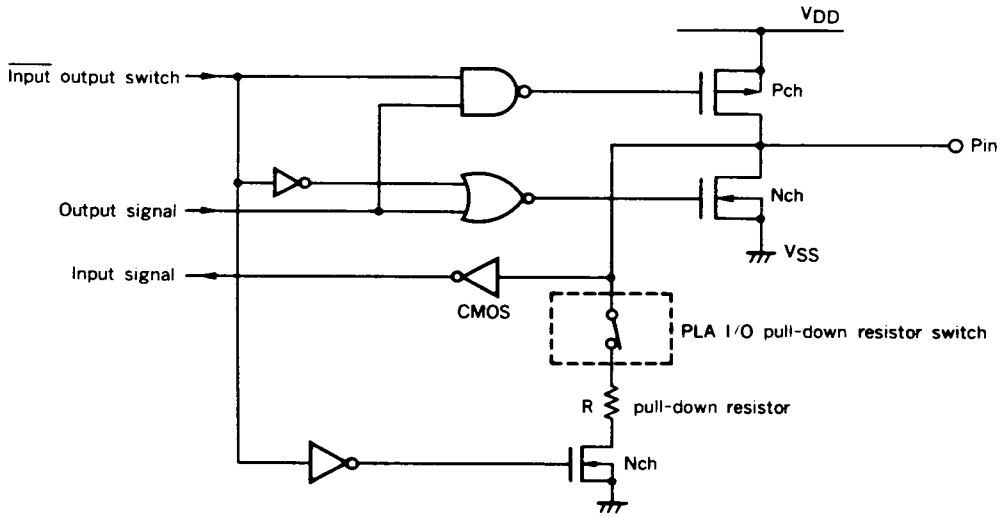
1.14 I/O Port (P_3)

This is an I/O port for key matrix expansion. Input mode and output mode are switched with the LSB of P_{13}.
The pull-down resistor of the LSI is disconnected for output mode.

Fig. 1-11 I/O Port Configuration



1.15 $K_{I/O}$ I/O Pull Down Resistance Configuration Diagram



The I/O port allows the pull-down resistance to be set or not set using the PLA data.

The pull-down resistor R is set only in input mode when the pull-down resistor switch is turned on ("1" is set) with the PLA data.

Turn on the pull-down resistor switch with the PLA data to use the pin as a switch.

The $K_{I/O}$ cannot use PLA data, to select whether the pull-down resistor is set or not.

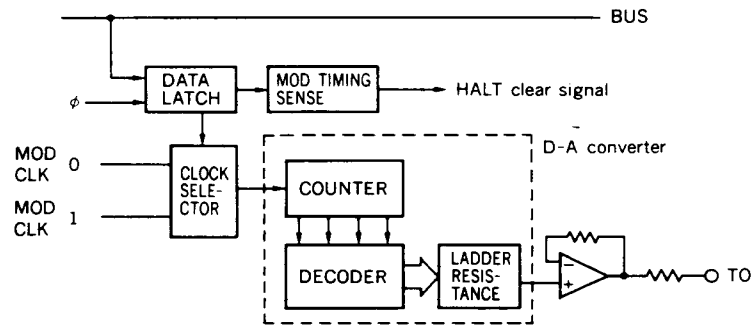
If the $K_{I/O}$ is set to input mode, all pins are pulled down to the V_{SS} level.

1.16 TO Port (P_{16})

This port outputs MAK (minimum shift keying) signals. When the D_6 of the control registor P_1 is set to "1" and HALT mode is set, the analog circuit power down occurs. The port status during analog circuit power down can be selected as pull-up resistor/pull-down resistor/high impedance.

Fig. 1-12 shows the transmitter configuration.

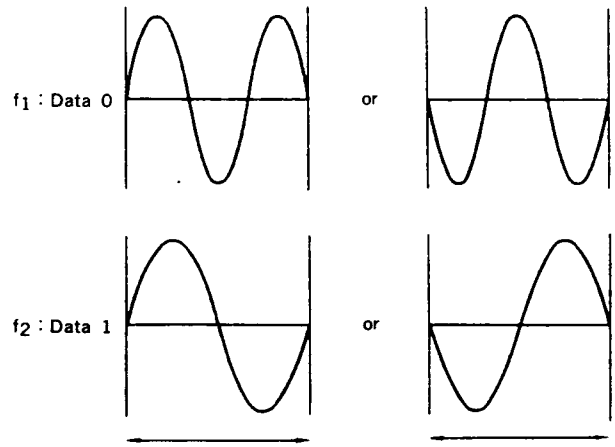
Fig. 1-12 Transmitter Block Diagram



Data is transmitted in units of a bit. Selection of a clock for the D/A converter depends on data stored in the data latch. On the circuit, selection of a clock for the D/A converter determines whether data 1 or data 0 is transmitted.

Fig. 1-13 shows transmission waveforms of data 0 and data 1.

Fig. 1-13 Transmission Waveforms of Data 0 and Data 1



Baud rate is selected with the PLA data.

The figure below shows the relationship between the baud rate and oscillator.

PLA data	Relationship of f_1, f_2, and f_{OSC}	f_1/f_2 (Hz) when f_{OSC} is 460.8 kHz
C_4	$f_1 = f_{OSC}/2^9 \times 3$ $f_2 = 1.5\, f_1$	300/450
C_3	$f_1 = f_{OSC}/2^8 \times 3$ $f_2 = 1.5\, f_1$	600/900
C_2	$f_1 = f_{OSC}/2^7 \times 3$ $f_2 = 1.5\, f_1$	1.2 k/1.8 k
C_1	$f_1 = f_{OSC}/2^6 \times 3$ $f_2 = 1.5\, f_1$	2.4 k/3.6 k
C_0	$f_1 = f_{OSC}/2^5 \times 3$ $f_2 = 1.5\, f_1$	4.8 k/7.2 k

When F_{OSC} is 460.8 kHz, f_1/f_2 becomes 300/450, 600/900, 1.2 k/1.8 k, 2.4 k/3.6 k, and 4.8 k/7.2 k.

The transmitter sends data determined by the D_3 and D_2 of the port P_{16} for each bit and the CPU waits for the completion of one bit data transmission in HALT mode.

The OUT P_{16}, A command resets the HALT release signal and transmit data to the P_{16}.

The HALT MOD command sets the HALT release signal.

When data is sent to the port P_{16} from the accumulator, the data is timed at the next HALT release signal setting.

Repeat the OUT P_{16}, A command and HALT MOD command to transmit data.

1.17 R1 Port (P_{06})

This is an input port (DEM port) to input the MSK signal. When the D_6 of the control register P_1 is set to "1" and the μPD6131 enters HALT mode, the analog circuit power down occurs. The port status during analog circuit power down can be selected as pull-up resistor/pull-down resistor/high impedance with the PLA data.

Fig. 1-14 shows the receiver configuration.

Input MSK signal delay is detected by the delay detection circuit consisting of a 48-stage shift register. Exclusive OR output of the input data and data delayed by one data unit is assumed to be detection output. Delay detection output includes a high frequency element. Eliminate it through the low-pass filter. This low-pass filter is a switched capacitor filter (SCF).

Output through the low-pass filter becomes detection output for the input data. This detection output is latched at the same time the output clock of the bit synchronizing circuit, then the received data becomes valid. The bit synchronizing circuit adjusts output clock synchronization by comparing a data changing point from "0" to "1" with an output clock timing of the bit synchronous circuit. To establish synchronization of the bit synchronizing circuit operation with the input signal timing, input twelve bits or more of "01" signals repeatedly as a bit synchronizing signal.

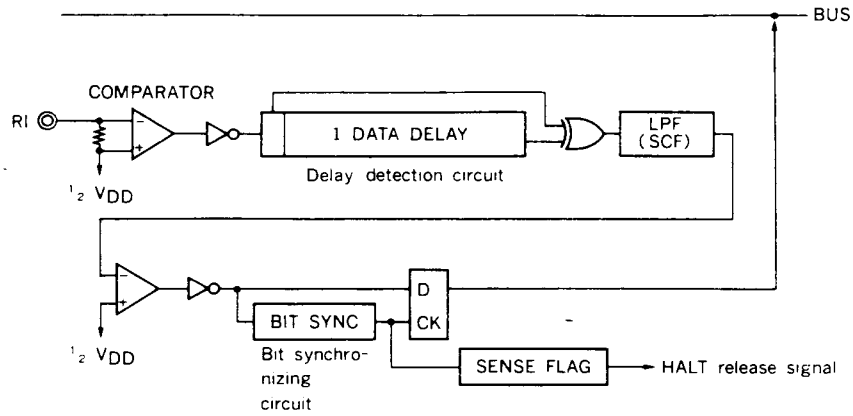
The CPU operation for receiving is the same as for transmission basically. The CPU waits for the receipt of one bit data in HALT mode. The HALT release signal is synchronized with bit synchronizing signal output. The CPU reads the receiving latch data in synchronism with the bit synchronizing signal output to determine whether the value is "0" or "1".

Data is input to the D_3 of the port P_{06}. The receiver receives data in units of a bit and the CPU waits for the receipt of data in HALT mode. The IN A, P_{06} command resets the HALT release signal to send data from P_{06} to the accumulator.

The HALT DEM command sets the HALT release signal.

When data is sent from the port P_{06} to the accumulator, data is received at the timing of the next HALT release signal setting. Data can be received by repeating the IN A, P_{06} command and HALT DEM command.

Fig. 1-14 Receiver Block Diagram



1.18 Control Register (P_1)

The control resister consists of eight bits. Table 1-1 lists details to be controlled.

Table 1-1

D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
TEST MODE		*	HALT	D.P. AD_9	D.P. AD_8			$K_{I/O}$	RL A_{CC} A_0←	
Setting always "0"		NOP	NOP	*	*	DEM	NOP	IN	A_3	0
		NOP	OSC STOP	*	*	Timer	NOP	OUT	S-IN	1

D_0 : Specifies data input to A0 when the left shift command of the accumulator is executed.
"0" = A_3, "1" = S-IN

D_1 : Specifies the $K_{I/O}$ status.
"0" = IN MODE, "1" = OUT MODE

D_3 : Specifies DEM/intermittent timer mode.
"0" = IN MODE, "1" = OUT MODE

D_4, D_5 : Specifies two high order bits of the ROM data pointer.

D_6 : Specifies the oscillation circuit during HALT command execution and when powering the analog circuit on or off.
"0" : Oscillation does not stop. The analog circuit is powered on.
"1" : Oscillation stops and the analog circuit is powered off. (STOP mode)

D_7 : NOP

D_8, D_9 : Register for setting test mode. Be sure to set D_8 and D_9 to "0".

2. STAND-BY FUNCTION (HALT)

The μPD6131 is provided with stand-by mode (HALT) for saving power while the program is waiting. The control register allows an oscillation stop to be executed during stand-by mode. (STOP mode)

The program execution stops when the μPD6131 enters stand-by mode. All contents of the register and data memory immediately before stand-by mode are held.

2.1 STOP Mode (Oscillation Stop HALT)

The system clock generation circuit (ceramic oscillator oscillation circuit) stops in STOP mode and the analog circuit is powered off. Consequently, an operation which requires a system clock stops.

2.2 HALT Mode (Oscillation Continuance HALT)

The CPU operation stops until the HALT release condition is generated.
The system clock generation circuit and analog circuit operate.

2.3 Stand-by Clear Condition

(1) S-IN input
(2) $K_{I/O}$ input
(3) MOD/DEM
(4) I/O input
(5) I/O, INTVL input
(6) S-IN, INTVL input

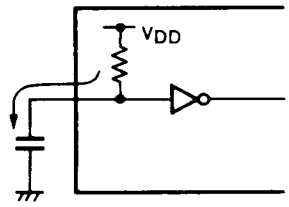
3. AC PIN

The program counter is reset by setting the AC pin to the V_{SS} level.

Watchdog Timer Function:

The CR watchdog timer applying the power on reset function and program control can be provided by adding an 0.1 μF capacitor between the AC pin and V_{SS}.

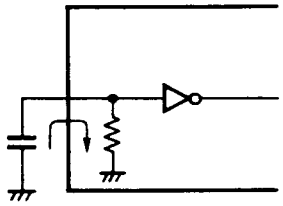
Charging mode



Charging start command:

Execute the HALT command immediately after executing the NOP command.

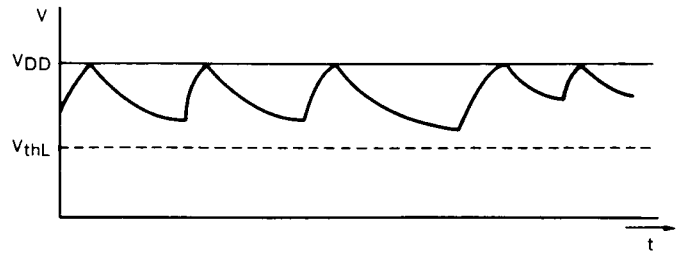
Discharging mode



Discharging start command:

Discharging starts immediately after the NOP command is executed.

Repeated pattern of discharging and charging



Control with the program so that the charging of C does not go lower than V_{thL}.

4. MASK OPTION

The following items can be selected by switching the mask option:

(1) Whether the pull-down resistor of the S-IN and I/O_0 ports is provided or not
(2) Specification of the pull-down resistor/pull-up resistor/high impedance of the RI and TO ports
(3) Specification of the 1/2 V_{DD}/floating of the TO port
(4) Whether the 32.768 kHz crystal oscillator is provided or not
(5) Baud rate specification
(6) Specification of the timer on the time during intermittent receiving
(7) Specification of overrun detection

PLA data is registered at the end of the object code.

Switching Bit Assignment

Address	Correspondence	MSB 7	6	5	4	3	2	1	LSB 0
0	S-IN	0	0	0	0	0	0	S-IN pull-down resistor	0
1	Overrun detection	$K_{I/O}$ ALL	HALT S-IN	HALT $K_{I/O}$	HALT INTVL	HALT I/O_0	0	HALT MOD	HALT DEM
2	Baud rate	0	0	0	C_4	C_3	C_2	C_1	C_0
3	OSC, RI, TO	0	32 K OSC	RI pull-up resistor	RI pull-down resistor	0	TO 1/2 V_{DD}/ floating	TO pull-up resistor	TO pull-down resistor
4	Timer	0	0	0	T_{20}	T_{16}	T_{12}	T_{10}	T_2
5	I/O_0	I/O_0 pull-down resistor				0	0	0	0

Switching for data

① Pull-down resistor (S-IN, I/O_0)
- 0: Not provided
- 1: Provided

② Pull-up resistor/pull-down resistor/high impedance (RI, TO)
- 0: Not provided
- 1: Provided

Only the following values can be selected:

PULL UP	PULL DOWN	Status
0	0	High impedance
0	1	Pull-down resistor provided
1	0	Pull-up resistor provided

③ TO 1/2 V_{DD} floating
- 0: 1/2 V_{DD} output
- 1: Floating

④ 32.768 kHz OSC
- 0: Not provided
- 1: Provided: The 32.768 kHz crystal oscillator is used for X_3 and X_4.

⑤ Baud rate specification
- 0: Not selected
- 1: Selected

LSB

C_4	C_3	C_2	C_1	C_0	Baud rate (when f_{OSC} is 460.8 kHz)
1	0	0	0	0	300/450
0	1	0	0	0	600/900
0	0	1	0	0	1.2 k/1.8 k
0	0	0	1	0	2.4 k/3.6 k
0	0	0	0	1	4.8 k/7.2 k

⑥ Timer specification

0: Not selected

1: Selected

LSB

T_{20}	T_{16}	T_{12}	T_{10}	T_2	Setting time
1	0	0	0	0	20 s
0	1	0	0	0	16 s
0	0	1	0	0	12 s
0	0	0	1	0	10 s
0	0	0	0	1	2 s

⑦ Overrun detection

(1) $K_{I/O}$ ALL

If the $K_{I/O}$ pin is in input mode or if the level of either $K_{I/O}$ pin goes low during oscillation stop HALT mode, system reset occurs.

0: Reset function not provided

1: Reset function provided

(2) HALT release condition specification

System reset occurs if "not used" is specified in the PLA during HALT mode.

0: Used

1: Not used

HALT #00EH command (I/O_0, INTVL)
#006H

or

HALT #00F command (S-IN, INTVL)
#007

is used, HALT S-IN and HALT I/O_0 are all specified as "not used".

Data setting format

(HEX)

Address	μPD6131	
0	0	0 or 2
1	0 to F	0, 1, 2, 3, 8, 9, A, B
2	0 or 1	1, 1, 2, 4, 8
3	0, 1, 2, 4, 5, 6	0, 1, 2, 4, 5, 6
4	0 or 1	0, 1, 2, 4, 8
5	0 to F	0

Reference of Mnemonic and Machine Language

Accumulator operation command

R_r	–	R_{10}	R_{11}	R_{12}		R_{1F}	R_{00}	R_{01}		R_{0F}
ANL A, R_r		D00	D01	D02		D0F	D20	D21		D2F
ANL A, @ R_0H	D10									
ANL A, @ R_0L	D30									
ANL A, #data	D31									
ORL A, R_r		E00	E01	E02		E0F	E20	E21		E2F
ORL A, @ R_0H	E10									
ORL A, @ R_0L	E30									
ORL A, #data	E31									
XRL A, R_r		A00	A01	A02		A0F	A20	A21		A2F
XRL A, @R_0H	A10									
XRL A, @R_0L	A30									
XRL A, #data	A31									
INC A	A13									
RL A	F13									

I/O command

P_P	P_{10}	P_{11}	P_{13}	P_{14}	P_{16}	P_{00}	P_{01}	P_{03}	P_{04}	P_{06}
IN A, P_P	F18	F19	F1B	F1C	F1E	F38	F39	F3B	F3C	F3E
OUT P_P, A	218	219	21B	21C	21E	238	239	23B	23C	23E
ANL A, P_P	D18	D19	D1B	D1C	D1E	D38	D39	D3B	D3C	D3E
ORL A, P_P	E18	E19	E1B	E1C	E1E	E38	E39	E3B	E3C	E3E
XRL A, P_P	A18	A19	A1B	A1C	A1E	A38	A39	A3B	A3C	A3E

P_P	P_0	P_1	P_3	P_4	P_6
OUT P_P, #data	318	319	31B	31C	31E

P_{1P} and P_{0P} operate as a pair.

Data transfer command

R_r		R_{10}	R_{11}	R_{12}		R_{1F}	R_{00}	R_{01}		R_{0F}

MOV A, R_r
MOV A, @ R_0H
MOV A, @ R_0L
MOV A, #data
	
	F10
	F30
	F31
		F00	F01	F02		F0F	F20	F21		F2F

MOV R_r, A		200	201	202		20F	220	221		22F

R_r		R_0	R_1	R_2		R_F
MOV R_r, #data		300	301	302		30F
MOV R_r, @ R_0		320	321	322		32F

P_{1r} and R_{0r} operate as a pair register.

Branch command

R_r	–	R_0	R_1	R_2		R_F	← Pair register
JMP0 addr	411						
JMP0 R_r	–	400	401	402		40F	
JC addr	611						
JC R_r	–	600	601	602		60F	
JNC addr	631						
JNC R_r	–	620	621	622		62F	
JF addr	711						
JF R_r	–	700	701	702		70F	
JNF addr	731						
JNF R_r	–	720	721	722		72F	

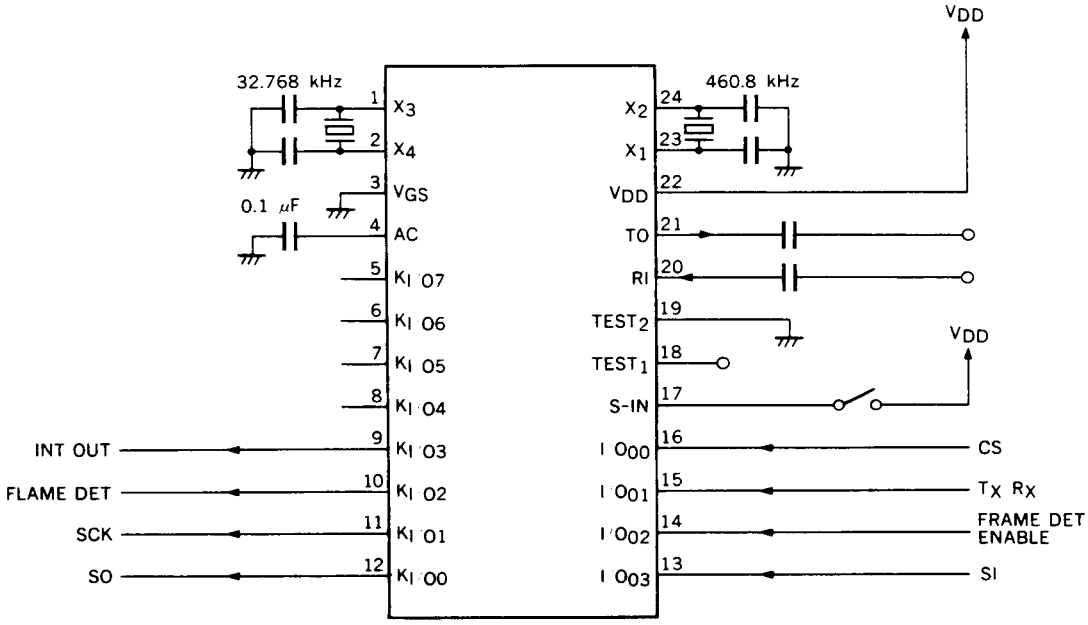
Subroutine command

CALL0 addr	312	411
RET	412	

Others

		R_{00}	R_{01}	R_{02}		R_{0F}
HALT #data	111					
STTS R_{0r} STTS #data	 131	120	121	122		12F
SCAF	D13					
NOP	000					

APPLICATION CIRCUIT DIAGRAM (Standard product μPD6131-011)



After the operation is started, SCK output and INT OUT output are started, T_X/R_X is read, and the subsequent operation is performed according to that setting.

T_X/R_X "H" level: Transmission mode
"L" level: Receiving mode

Transmission mode (S-IN: "H" level, CS: "H" level, T_X/R_X: "H" level)

Data is read at the timing of SCK clock from the SI input and that data is output from the TO pin as an MSK signal.

T_X/R_X goes low level or CS goes low level when transmission is completed.

Receiving mode (S-IN: "H" level, CS: "H" level, T_X/R_X: "L" level)

FRAME DET ENABLE (I/O_{02}) is read and the operation is performed according to that setting.

FRAME DET ENABLE:

"H" level: After the frame pattern is detected, the FRAME DET output ($K_{I/O2}$) is kept at the high level.

"L" level: FRAME DET output ($K_{I/O2}$) is set at low level.

When FRAME DET ENABLE input level goes high, the FRAME DET output ($K_{I/O2}$) level goes high after the frame pattern is detected, and receiving data is output from the SO output on the timing of the SCK clock.

When the FRAME DET ENABLE input level goes low, receiving data is output from the SO output on the timing of the SCK clock, and the FRAME DET output ($K_{I/O2}$) is set at low level.

Before using the μPD6131, consider the relationship between the operation frequency deviation of the transmitter and receiver and transmission bit pattern.

Figs. 1 and 2 show the relationship of bit patterns that can be transmitted and operation frequency fluctuation rate of the transmitter and receiver.

Frequency allowable fluctuation rate vs. Number of the same code continuous bits.

Fig. 1 Frequency Allowable Fluctuation Rate vs. Number of the Same Code Continuous Bits (Maximum Length)

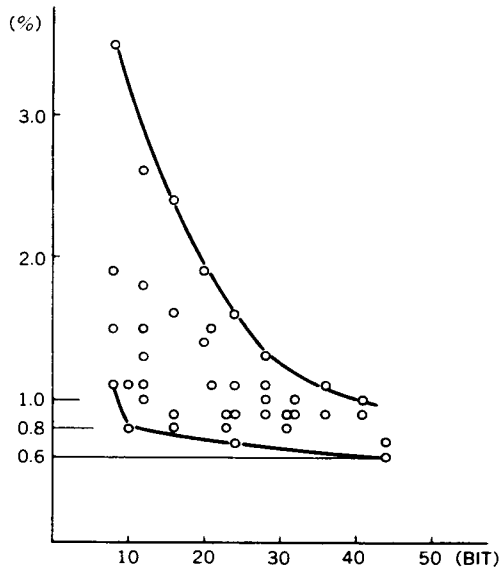
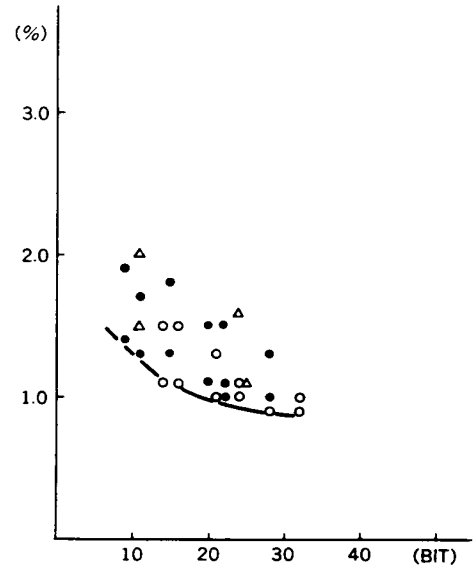


Fig. 2 Frequency Allowable Fluctuation Rate vs. Number of the Same Code Continuous Bits (Maximum Length)



Including one "0101" pattern : ○
Including two "0101" patterns : ●
Including three "0101" patterns : △

As shown in the above figures, for a pattern containing bit strings of the same code too much, the receiver cannot follow the frequency difference of the transmitter.

When the μPD6131 is applied, be careful not to provide bit strings of the same code too much.

When fluctuation of the operating frequency between the transmitter and receiver is within ±1 %, set transmission bit patterns as follows:

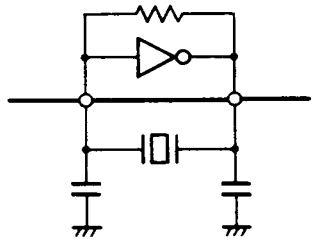
(1) When "0101" pattern is not included, the same code must not continue for 9 bits or more.
(2) When one "0101" pattern is included, the same code must not continue for 16 bits or more.
(3) When two "0101" patterns are included, the same code must not continue for 20 bits or more.
(4) When three "0101" patterns are included, the same code must not continue for 25 bits or more.

Use the ceramic oscillator for μPD6131 as shown below to set the operating frequency fluctuation to ±1 % or less.
For details of the oscillation characteristics, contact each oscillator manufacturer.

Manufacturer	Manufacturer type number
Murata Mfg. Co., Ltd.	CSB460E930
Toko Inc.	P11ACRK460-M31

Application Circuit

Application circuit



ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Supply Voltage	V_{DD}	7.0	V
Input Voltage	V_{IN}	−0.3 to V_{DD} + 0.3	V
Operating Temperature	T_{opt}	−40 to +85	°C
Storage Temperature	T_{stg}	−40 to +125	°C

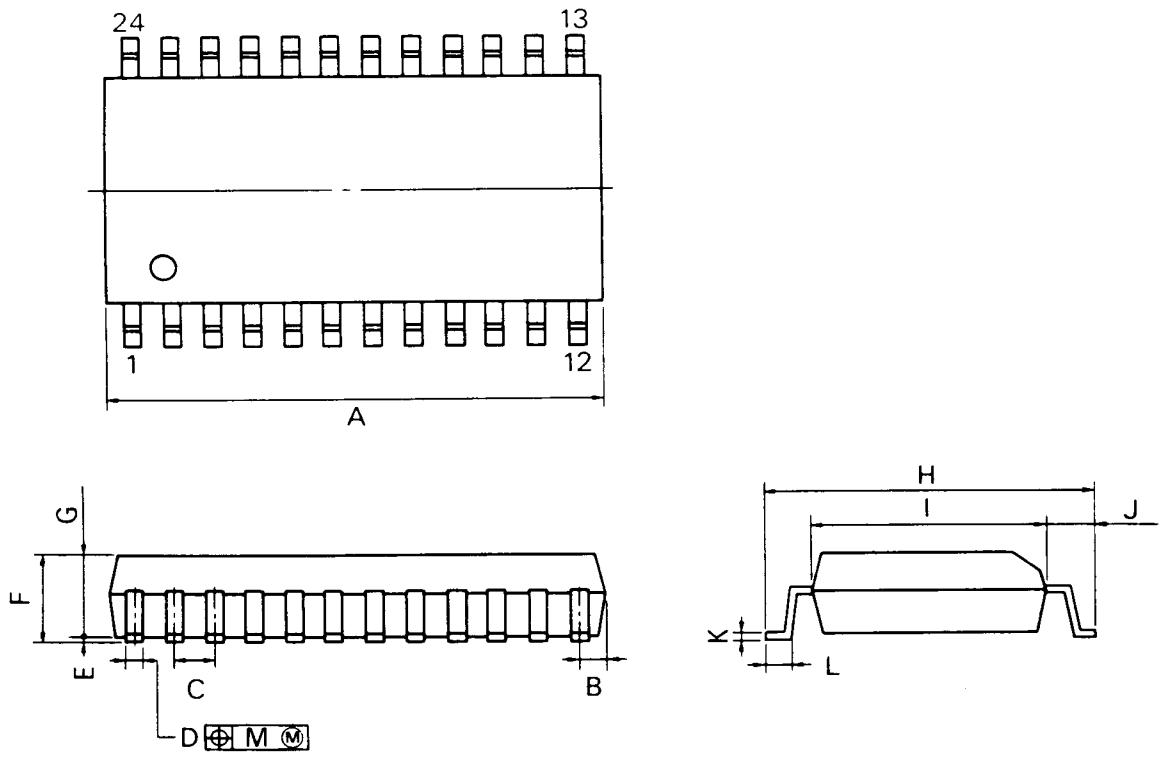
RECOMMENDED OPERATING CONDITION (T_a = −40 to +85 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Operating Supply Voltage Range	V_{DD}	2.2	3.0	6.0	V
Oscillation Frequency 1 (X_1, X_2)	f_1	400	460.8	500	kHz
Oscillation Frequency 2 (X_3, X_4)	f_2		32.768		kHz
Receiving Input Signal (RI)	v_{in}	0.05	0.2	1.0	V_{p-p}

ELECTRICAL CHARACTERISTICS (V_{DD} = 3.0 V, f_1 = 460.8 kHz, f_2 = 32.768 kHz, T_a = 25 °C)

CHARACTEISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Current Consumption 1	I_{DD1}	0.5	1	2	mA	f_1 = 460.8 kHz, f_2 = 32 kHz
Current Consumption 2	I_{DD2}		2.5	5.0	μA	f_1 = STOP, f_2 = 32 kHz
$K_{I/O}$ and I/O High Level Input Current	I_{IH1}	10		35	μA	$V_I = V_{DD}$
$K_{I/O}$ and I/O Low Level Input Current	I_{IL1}			−0.2	μA	$V_I = V_{SS}$
$K_{I/O}$ and I/O High Level Output Current	I_{OH1}	−0.8		−3	mA	V_O = 2.7 V
$K_{I/O}$ and I/O Low Level Output Current	I_{OL1}	25		110	μA	V_O = 2.1 V
S-IN High Level Input Current	I_{IH2}	6		20	μA	$V_I = V_{DD}$
S-IN Low Level Input Current	I_{IL2}			−0.2	μA	$V_I = V_{SS}$
S-IN High Level Input Current	I_{IH2}'			0.2	μA	$V_I = V_{DD}$ (No pull-down resistor)
Transmission Output Voltage (TO)	v_O	0.5	0.6	0.7	V_{p-p}	$R_L = \infty$
Receiving Input Voltage (RI)	v_i	0.05		1.0	V_{p-p}	
Receiving Input Impedance (RI)	R_i	120	200	350	kΩ	

24PIN PLASTIC SOP (375 mil)



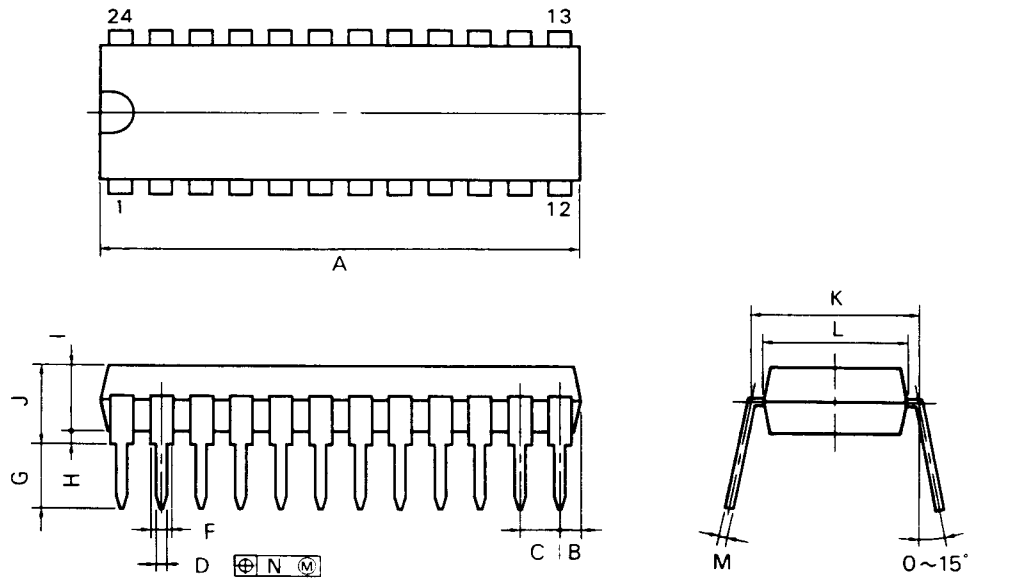
P24GM-50-375B-1

NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	15.54 MAX.	0.612 MAX.
B	0.78 MAX.	0.031 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.40^{+0.10}_{-0.05}$	$0.016^{+0.004}_{-0.003}$
E	0.1 ± 0.1	0.004 ± 0.004
F	2.9 MAX.	0.115 MAX.
G	2.50	0.098
H	10.3 ± 0.3	$0.406^{+0.012}_{-0.013}$
I	7.2	0.283
J	1.6	0.063
K	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.002}$
L	0.8 ± 0.2	$0.031^{+0.009}_{-0.008}$
M	0.12	0.005

24PIN PLASTIC SHRINK DIP (300 mil)



S24C-70-300B

NOTES

1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	23.12 MAX.	0.911 MAX.
B	1.78 MAX.	0.070 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	$0.50^{-0.10}$	$0.020^{-0.004}_{-0.005}$
F	0.85 MIN.	0.033 MIN.
G	$3.2^{-0.3}$	$0.126^{-0.012}$
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	7.62 (T.P.)	0.300 (T.P.)
L	6.5	0.256
M	$0.25^{-0.10}_{-0.05}$	$0.010^{-0.004}_{-0.003}$
N	0.17	0.007

RECOMMENDED SOLDERING CONDITIONS

The following conditions (see table below) must be met when soldering this product. Please consult with our sales offices in case other soldering process is used, or in case soldering is done under different conditions.

TYPES OF SURFACE MOUNT DEVICE

For more details, refer to our document "SMT MANUAL" (IEI-1207).

μPD6131GT

Soldering Process	Soldering Conditions	Symbol
Infrared ray reflow	Peak package's surface temperature : 230 °C or below, Reflow time : 30 seconds or below (210 °C or higher), Number of reflow process : 1, Exposure limit* : None	IR30-00
VPS	Peak package's surface temperature : 215 °C or below, Reflow time : 40 seconds or below (200 °C or higher), Number of reflow process : 1, Exposure limit* : None	VP15-00
Wave Soldering	Solder temperature : 260 °C or below, Flow time : 10 seconds or below, Number of flow process : 1, Exposure limit* : None	WS60-00
Partial heating method	Terminal temperature : 300 °C or below, Flow time : 10 seconds or below, Exposure limit* : None	

*: Exposure limit before soldering after dry-pack package is opened.
Storage conditions : 25 °C and relative humidity at 65 % or less.

Note: Do not apply more than a single process at once, except for "Partial heating method".

TYPES OF THROUGH HOLE MOUNT DEVICE

μPD6131CS

Soldering Process	Soldering Conditions
Wave Soldering	Solder temperature : 260 °C or below, Flow time : 10 seconds or below