

### DESCRIPTION

This family is a 4M bit dynamic RAM organized 262.144 x 16-bit configuration with CMOS DRAMs. The circuit and process design allow this device to achieve high performance and low power dissipation. Optional features are access time (60,70 or 80ns) and package type (SOJ, TSOP-II and reverse TSOP-II) and power consumption (Normal or Low power with Self refresh). Hyundai's advanced circuit design and process technology allow this device to achieve high bandwidth, low power consumption and high reliability.

### ORDERING INFORMATION

| Part Number    | SPEED    | Power   | Pkg.       |
|----------------|----------|---------|------------|
| HY51V4260BJC   | 60/70/80 |         | SOJ        |
| HY51V4260BLJC  | 60/70/80 | L-part  | SOJ        |
| HY51V4260BSLJC | 60/70/80 | SL-part | SOJ        |
| HY51V4260BLTC  | 60/70/80 |         | TSOP-II    |
| HY51V4260BLTC  | 60/70/80 | L-part  | TSOP-II    |
| HY51V4260BSLTC | 60/70/80 | SL-part | TSOP-II    |
| HY51V4260BRC   | 60/70/80 |         | TSOP-II(R) |
| HY51V4260BLRC  | 60/70/80 | L-part  | TSOP-II(R) |
| HY51V4260BSLRC | 60/70/80 | SL-part | TSOP-II(R) |

### FEATURES

- Low power dissipation
  - Max. battery back-up 1.08mW (SL-part)
  - Max. CMOS standby 0.72mW (SL-part)
  - 3.6mW
  - Max. TTL standby 7.2mW
  - Max. Self Refresh 0.72mW (SL-part)
  - Max. operating

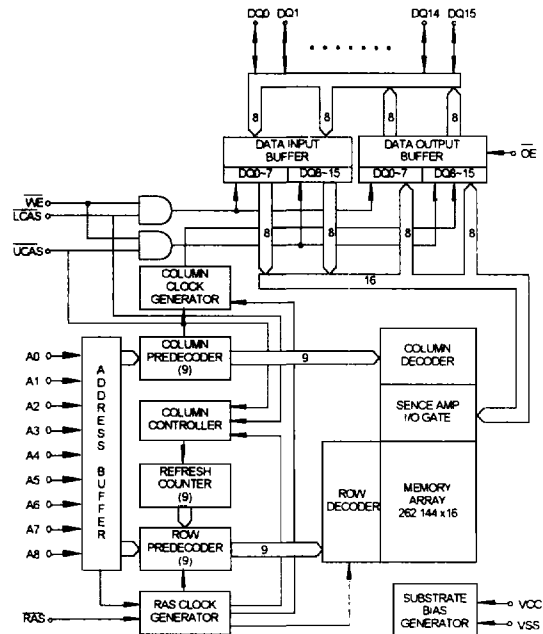
| Speed | Power   |
|-------|---------|
| 60    | 468.0mW |
| 70    | 432.0mW |
| 80    | 396.0mW |

- Single power supply of 3.3V ± 10%
- TTL compatible inputs and outputs
- Fast access time and cycle time
 

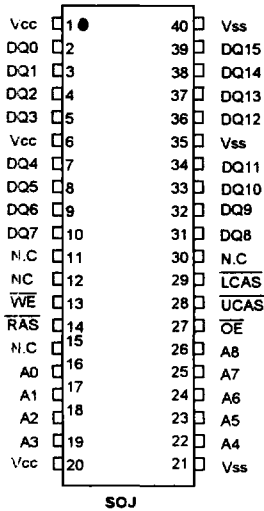
| Speed | tRAC | tCAC | tPC  |
|-------|------|------|------|
| 60ns  | 60ns | 15ns | 40ns |
| 70ns  | 70ns | 20ns | 45ns |
| 80ns  | 80ns | 20ns | 50ns |
- Fast page mode Operation
- /2/CAS inputs for upper and lower byte control
- Read-Modify-Write Capability
- /CAS-before-/RAS, /RAS-only, Hidden refresh and Self Refresh capability
- 512 refresh cycles / 128ms(SL-part)
- 512 refresh cycles / 8ms

- JEDEC standard pinout
  - 40-pin SOJ (400mil)
  - 40/44-pin TSOP(400mil)

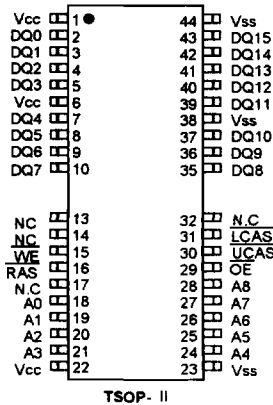
### BLOCK DIAGRAM



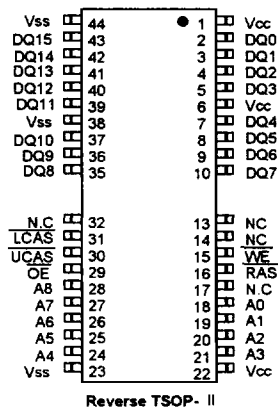
**PIN CONFIGURATION (Marking Side)**



**40-pin SOJ (400mil)**



**40/44-pin TSOP-II (400mil)**



**40/44-pin TSOP-II(R) (400mil)**

**PIN DESCRIPTION**

|              |                       |
|--------------|-----------------------|
| /RAS         | Row Address Strobe    |
| /LCAS, /UCAS | Column Address Strobe |
| /WE          | Write Enable          |
| /OE          | Output Enable         |
| A0-A8        | Address Input         |
| DQ0-DQ15     | Data I/O              |
| Vcc          | Power (+3.3V)         |
| Vss          | Ground                |

**ABSOLUTE MAXIMUM RATINGS**

| SYMBOL    | PARAMETER                          | RATING      | UNIT     |
|-----------|------------------------------------|-------------|----------|
| TA        | Ambient Temperature                | 0 to 70     | °C       |
| TSTG      | Storage Temperature                | -55 to 150  | °C       |
| VIN, VOUT | Voltage on Any Pin relative to Vss | -0.5 to 4.6 | V        |
| VCC       | Voltage on Vcc relative to Vss     | -0.5 to 4.6 | V        |
| Ios       | Short Circuit Output Current       | 20          | mA       |
| PD        | Power Dissipation                  | 1.0         | W        |
| TSOLDER   | Soldering Temperature · Time       | 260 · 10    | °C · sec |

Note: Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

**RECOMMENDED DC OPERATING CONDITIONS**

(TA=0°C to 70°C)

| SYMBOL | PARAMETER            | MIN. | TYP. | MAX.    | UNIT |
|--------|----------------------|------|------|---------|------|
| VCC    | Power Supply Voltage | 3.0  | 3.3  | 3.6     | V    |
| VIH    | Input High Voltage   | 2.0  | -    | VCC+0.3 | V    |
| VIL    | Input Low Voltage    | -0.3 | -    | 0.8     | V    |

Note: All voltages are referenced to Vss.



**DC CHARACTERISTICS**

( $T_A=0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ ,  $V_{CC}=3.3\text{V} \pm 10\%$ ,  $V_{SS}=0\text{V}$ , unless otherwise noted.)

| Symbol           | Parameter   | Test Conditions  | Speed/<br>Power | Min.        | Max.              | Unit                | Note  |
|------------------|---|--|-----------------|-------------|-------------------|---------------------|-------|
| I <sub>LI</sub>  | Input Leakage current<br>(Any Input Pins)                           | $V_{SS} \leq V_{IN} \leq 6.5\text{V}$<br>All other pins not under test = $V_{SS}$  |                 | -10         | 10                | $\mu\text{A}$       |       |
| I <sub>LO</sub>  | Output Leakage current<br>(High Impedance State)                    | $V_{SS} \leq V_{OUT} \leq 5.5\text{V}$<br>/RAS & /CAS at $V_{IH}$  |                 | -10         | 10                | $\mu\text{A}$       |       |
| I <sub>CC1</sub> | V <sub>CC</sub> Supply Current,<br>Operating                        | t <sub>RC</sub> =t <sub>RC</sub> (min.)  | 60<br>70<br>80  | -<br>-<br>- | 130<br>120<br>110 | mA                  | 1,2,3 |
| I <sub>CC2</sub> | V <sub>CC</sub> Supply Current,<br>TTL Standby                      | /RAS & /CAS at $V_{IH}$ , (min.) other<br>inputs $\geq V_{SS}$   |                 | -           | 2                 | mA                  |       |
| I <sub>CC3</sub> | V <sub>CC</sub> Supply Current,<br>/RAS-only Refresh                | t <sub>RC</sub> =t <sub>RC</sub> (min.)  | 60<br>70<br>80  | -<br>-<br>- | 130<br>120<br>110 | mA                  | 1,3   |
| I <sub>CC4</sub> | V <sub>CC</sub> Supply Current,<br>Fast Page Mode                   | t <sub>PC</sub> =t <sub>PC</sub> (min.)  | 60<br>70<br>80  | -<br>-<br>- | 80<br>70<br>60    | mA                  | 1,2,3 |
| I <sub>CC5</sub> | V <sub>CC</sub> Supply Current,<br>CMOS Standby                     | /RAS & /CAS $\geq V_{CC} - 0.2\text{V}$  | SL-part         | -           | 1<br>200          | mA<br>$\mu\text{A}$ | 5     |
| I <sub>CC6</sub> | V <sub>CC</sub> Supply Current,<br>/CAS-before-/RAS<br>Refresh      | t <sub>RC</sub> =t <sub>RC</sub> (min.)  | 60<br>70<br>80  | -<br>-<br>- | 130<br>120<br>110 | mA                  | 1,3   |
| I <sub>CC7</sub> | V <sub>CC</sub> Supply Current<br>Battery Back Up<br>(SL-part only) | t <sub>RC</sub> = 250 $\mu\text{s}$ , t <sub>RAS</sub> $\leq 1\mu\text{s}$ ,<br>/CAS = CBR cycling or 0.2 V<br>/OE & /WE = $V_{CC} - 0.2\text{V}$ ,<br>A0-9 = $V_{CC} - 0.2\text{V}$ or 0.2V<br>DQ0-DQ3 = 0.2, $V_{CC} - 0.2\text{V}$ or<br>open |                 | -           | 300               | $\mu\text{A}$       | 1,4,5 |
| I <sub>CC8</sub> | V <sub>CC</sub> Supply Current<br>Self Refresh<br>(SL-part only)    | /RAS & /CAS $\leq 0.2\text{V}$<br>other pins same as I <sub>CC7</sub>  |                 | -           | 200               | $\mu\text{A}$       | 5     |
| V <sub>OL</sub>  | Output Low Voltage  | I <sub>OL</sub> = 4.2mA  |                 | -           | 0.4               | V                   |       |
| V <sub>OH</sub>  | Output High Voltage   | I <sub>OH</sub> = -5mA   |                 | 2.4         | -                 | V                   |       |

**NOTE**

- I<sub>CC1</sub>, I<sub>CC3</sub>, I<sub>CC4</sub> and I<sub>CC6</sub> depend on cycle rates.
- I<sub>CC1</sub>, I<sub>CC3</sub>, I<sub>CC4</sub> and I<sub>CC6</sub> are dependent on output loading. Specified values are obtained with the output open.
- I<sub>CC</sub> is specified as an average current. In I<sub>CC1</sub>, I<sub>CC3</sub>, I<sub>CC6</sub>, Address can be changed maximum two times while /RAS= $V_{IL}$ . In I<sub>CC4</sub>, Address can be changed maximum once while /CAS= $V_{IH}$ .
- Only t<sub>RAS</sub>(max.) = 1 $\mu\text{s}$  is applied to refresh of battery backup but t<sub>RAS</sub>(max.) = 10 $\mu\text{s}$  is to applied to normal functional operation.
- I<sub>CC5</sub>(max.), I<sub>CC7</sub> and I<sub>CC8</sub> are applied to SL-part only.

**AC CHARACTERISTICS**

(T<sub>A</sub>=0°C to 70°C, V<sub>CC</sub>=3.3V ± 10%, V<sub>SS</sub>=0V, unless otherwise noted.) NOTE : 1,2, 3,13

| #  | SYMBOL            | PARAMETER                                   | HY51V4260B |      |      |      |      |      | UNIT | NOTE   |
|----|-------------------|---|------------|------|------|------|------|------|------|--------|
|    |                   |   | -60        |      | -70  |      | -80  |      |      |        |
|    |                   |   | MIN.       | MAX. | MIN. | MAX. | MIN. | MAX. |      |        |
| 1  | t <sub>RC</sub>   | Random Read or Write Cycle Time             | 110        | -    | 130  | -    | 150  | -    | ns   |        |
| 2  | t <sub>RWC</sub>  | Read-Modify-Write Cycle Time                | 155        | -    | 185  | -    | 205  | -    | ns   |        |
| 3  | t <sub>PC</sub>   | Fast Page Mode Cycle Time                   | 40         | -    | 45   | -    | 50   | -    | ns   |        |
| 4  | t <sub>PRWC</sub> | Fast Page Mode Read-Modify-Write Cycle Time | 80         | -    | 95   | -    | 105  | -    | ns   |        |
| 5  | t <sub>RAC</sub>  | Access Time from /RAS                       | -          | 60   | -    | 70   | -    | 80   | ns   | 4,9,10 |
| 6  | t <sub>CAC</sub>  | Access Time from /CAS                       | -          | 15   | -    | 20   | -    | 20   | ns   | 4,9    |
| 7  | t <sub>AA</sub>   | Access Time from Column Address             | -          | 30   | -    | 35   | -    | 40   | ns   | 4,10   |
| 8  | t <sub>CPA</sub>  | Access Time from Column Precharge           | -          | 35   | -    | 40   | -    | 45   | ns   | 4,15   |
| 9  | t <sub>CLZ</sub>  | /CAS to Output Low Impedance                | 0          | -    | 0    | -    | 0    | -    | ns   | 4      |
| 10 | t <sub>OFF</sub>  | Output Buffer Turn-off Delay Time           | 0          | 15   | 0    | 15   | 0    | 15   | ns   |        |
| 11 | t <sub>T</sub>    | Transition Time (Rise and Fall)             | 3          | 50   | 3    | 50   | 3    | 50   | ns   | 3      |
| 12 | t <sub>RP</sub>   | /RAS Precharge Time                         | 40         | -    | 50   | -    | 60   | -    | ns   |        |
| 13 | t <sub>RAS</sub>  | /RAS Pulse Width                            | 60         | 10k  | 70   | 10k  | 80   | 10k  | ns   |        |
| 14 | t <sub>RASP</sub> | /RAS Pulse Width (Fast Page Mode)           | 60         | 100k | 70   | 100k | 80   | 100k | ns   |        |
| 15 | t <sub>RSH</sub>  | /RAS Hold Time                              | 15         | -    | 20   | -    | 20   | -    | ns   |        |
| 16 | t <sub>CSH</sub>  | /CAS Hold Time                              | 60         | -    | 70   | -    | 80   | -    | ns   |        |
| 17 | t <sub>CAS</sub>  | /CAS Pulse Width                            | 15         | 10k  | 20   | 10k  | 20   | 10k  | ns   |        |
| 18 | t <sub>RCD</sub>  | /RAS to /CAS Delay Time                     | 20         | 45   | 20   | 50   | 20   | 60   | ns   | 9      |
| 19 | t <sub>RAD</sub>  | /RAS to Column Address Delay Time           | 15         | 30   | 15   | 35   | 15   | 40   | ns   | 10     |
| 20 | t <sub>CRP</sub>  | /CAS to /RAS Precharge Time                 | 5          | -    | 5    | -    | 5    | -    | ns   | 15     |
| 21 | t <sub>CP</sub>   | /CAS Precharge Time                         | 10         | -    | 10   | -    | 10   | -    | ns   | 17     |
| 22 | t <sub>ASR</sub>  | Row Address Set-up Time                     | 0          | -    | 0    | -    | 0    | -    | ns   |        |
| 23 | t <sub>RAH</sub>  | Row Address Hold Time                       | 10         | -    | 10   | -    | 10   | -    | ns   |        |
| 24 | t <sub>ASC</sub>  | Column Address Set-up Time                  | 0          | -    | 0    | -    | 0    | -    | ns   | 14     |
| 25 | t <sub>CAH</sub>  | Column Address Hold Time                    | 15         | -    | 15   | -    | 15   | -    | ns   | 14     |
| 26 | t <sub>AR</sub>   | Column Address Hold Time from /RAS          | 50         | -    | 55   | -    | 60   | -    | ns   |        |
| 27 | t <sub>RAL</sub>  | Column Address to /RAS Lead Time            | 30         | -    | 35   | -    | 40   | -    | ns   |        |
| 28 | t <sub>RCS</sub>  | Read Command Set-up Time                    | 0          | -    | 0    | -    | 0    | -    | ns   | 14     |
| 29 | t <sub>RCH</sub>  | Read Command Hold Time Referenced to /CAS   | 0          | -    | 0    | -    | 0    | -    | ns   | 6,14   |
| 30 | t <sub>RRH</sub>  | Read Command Hold Time Referenced to /RAS   | 0          | -    | 0    | -    | 0    | -    | ns   | 5      |
| 31 | t <sub>WCH</sub>  | Write Command Hold Time                     | 10         | -    | 15   | -    | 20   | -    | ns   | 14     |
| 32 | t <sub>WCR</sub>  | Write Command Hold Time from /RAS           | 45         | -    | 55   | -    | 60   | -    | ns   |        |
| 33 | t <sub>WP</sub>   | Write Command Pulse Width                   | 10         | -    | 10   | -    | 15   | -    | ns   |        |
| 34 | t <sub>RWL</sub>  | Write Command to /RAS Lead Time             | 15         | -    | 20   | -    | 20   | -    | ns   |        |
| 35 | t <sub>CWL</sub>  | Write Command to /CAS Lead Time             | 15         | -    | 20   | -    | 20   | -    | ns   | 16     |
| 36 | t <sub>DS</sub>   | Data-In Set-up Time                         | 0          | -    | 0    | -    | 0    | -    | ns   | 7      |
| 37 | t <sub>DH</sub>   | Data-In Hold Time                           | 15         | -    | 15   | -    | 20   | -    | ns   | 7      |
| 38 | t <sub>DHR</sub>  | Data-In Hold Time Referenced to /RAS        | 45         | -    | 55   | -    | 60   | -    | ns   |        |

4M

**AC CHARACTERISTICS**

(Continued)

| #  | SYMBOL | PARAMETER                                  | HY51V4260B |      |          |      |          |      | UNIT | NOTE      |
|----|--------|--|------------|------|----------|------|----------|------|------|-----------|
|    |        |  | -60        |      | -70      |      | -80      |      |      |           |
|    |        |  | MIN.       | MAX. | MIN.     | MAX. | MIN.     | MAX. |      |           |
| 39 | tREF   | Refresh Period (512cycles)<br>(SL-part)    | 8<br>128   | -    | 8<br>128 | -    | 8<br>128 | -    | ms   | 12,<br>11 |
| 40 | tWCS   | Write Command Set-up Time                  | 0          | -    | 0        | -    | 0        | -    | ns   | 8,14      |
| 41 | tCWD   | /CAS to /WE Delay Time                     | 40         | -    | 50       | -    | 50       | -    | ns   | 8         |
| 42 | tRWD   | /RAS to /WE Delay Time                     | 85         | -    | 100      | -    | 110      | -    | ns   | 8         |
| 43 | tAWD   | Column Address to /WE Delay Time           | 55         | -    | 65       | -    | 70       | -    | ns   | 8         |
| 44 | tCSR   | /CAS Set-up Time (CBR Cycle)               | 5          | -    | 5        | -    | 5        | -    | ns   | 14        |
| 45 | tCHR   | /CAS Hold Time (CBR Cycle)                 | 10         | -    | 10       | -    | 10       | -    | ns   | 15        |
| 46 | tRPC   | /RAS to /CAS Precharge Time                | 5          | -    | 5        | -    | 5        | -    | ns   | 14        |
| 47 | tCPT   | /CAS Precharge Time (CBR Counter Test)     | 20         | -    | 25       | -    | 30       | -    | ns   | 17        |
| 48 | tROH   | /RAS Hold Time Reference to /OE            | 0          | -    | 0        | -    | 0        | -    | ns   |           |
| 49 | tOEA   | /OE Access Time                            | -          | 15   | -        | 20   | -        | 20   | ns   |           |
| 50 | tOED   | /OE to Data Delay Time                     | 15         | -    | 20       | -    | 20       | -    | ns   |           |
| 51 | tOEZ   | Output Buffer Turn Off Delay Time from /OE | 0          | 15   | 0        | 20   | 0        | 20   | ns   | 5         |
| 52 | tOEH   | /OE Command Hold Time                      | 15         | -    | 20       | -    | 20       | -    | ns   |           |
| 53 | tCPWD  | /WE Delay Time from /CAS Precharge         | 55         | -    | 65       | -    | 75       | -    | ns   | 8         |
| 54 | tRHCP  | /RAS Hold Time from /CAS Precharge         | 35         | -    | 40       | -    | 45       | -    | ns   |           |
| 55 | tRASS  | /RAS Pulth Width (Self Refresh)            | 100        | -    | 100      | -    | 100      | -    | ns   |           |
| 56 | tRPS   | /RAS Precharge Time (Self Refresh)         | 130        | -    | 150      | -    | 180      | -    | ns   |           |
| 57 | tCHS   | /CAS Hold Time from /RAS (Self Refresh)    | -50        | -    | -50      | -    | -50      | -    | ns   |           |

**NOTE**

1. An initial pause of 200us is required after power-up followed by 8 /RAS cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 /CAS-before-/RAS initialization cycles instead of 8 /RAS-only refresh cycles are required.
2. If /RAS=Vss during power-up, the HY51V4260B could begin an active cycle. This condition results in higher current than necessary current which is demanded from the power supply during power-up. It is recommended that /RAS and /CAS track with Vcc during power-up or be held at a valid VIH in order to minimize the power-up current.
3. VIH(min.) and VIL(max.) are reference levels for measuring timing of input signals. Transition times are measured between VIH(min.) and VIL(max.), and are assumed to be 5ns for all inputs.
4. Measured at VOH=2.0V and VOL=0.8V with a load equivalent to 1 TTL loads and 100pF.
5. tOFF(max.) and tOEZ define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
6. Either tRCH or tRRH must be satisfied for a read cycle.
7. These parameters are referenced to /LCAS or /UCAS leading edge in early write cycles and to /WE leading edge in Read-Modify-Write cycles.
8. tWCS, tRWD, tCWD, tAWD and tCPWD are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If tWCS ≥ tWCS(min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle. If tRWD ≥ tRWD(min.), tCWD ≥ tCWD(min.), tAWD ≥ tAWD(min.), and tCPWD ≥ tCPWD(min.), the cycle is a Read-Modify-Write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
9. Operation within the tRCD(max.) limit ensures that tRAC(max.) can be met. tRCD(max.) is specified as a reference point only. If tRCD is greater than the specified tRCD(max.) limit, then access time is controlled by tCAC.
10. Operation within the tRAD(max.) limit ensures that tRAC(max.) can be met. tRAD(max.) is specified as a reference point only. If tRAD is greater than the specified tRAD(max.) limit, then access time is controlled by tAA.
11. tREF(max.)=128ms is applied to SL-parts only.
12. A burst of 512 /CAS-before-/RAS refresh cycles must be executed within 8ms (128ms for SL-parts) after exiting self refresh.
13. When both /LCAS and /UCAS go low at the same time, all 16-bits data are written into the device. /LCAS and /UCAS must be transited simultaneously within a same read or write cycle.
14. These parameters are determined by the earlier falling edge of /LCAS or /UCAS.
15. These parameters are determined by the later rising edge of /LCAS or /UCAS.
16. tCWL must be satisfied by both /LCAS and /UCAS for 16-bits access cycles.
17. tCP and tCPT are measured when both /LCAS and /UCAS are high state.



**CAPACITANCE**

(TA=25°C, Vcc=3.3V ± 10%, Vss=0V, If = 1MHz, unless otherwise noted.)

| SYMBOL | PARAMETER  | TYP. | MAX. | UNIT |
|--------|--|------|------|------|
| CIN1   | Input Capacitance (A0 - A8)                      | -    | 5    | pF   |
| CIN2   | Input Capacitance (/RAS, /LCAS, /UCAS, /WE, /OE) | -    | 7    | pF   |
| CDQ    | Data Input /Output Capacitance (DQ0 - DQ15)      | -    | 7    | pF   |