

ACL Products

FEATURES

- High-speed parallel registers with positive edge-triggered D-type flip-flops
- Extra data width for wide address/data paths or buses with parity
- Output capability: $\pm 24\text{mA}$
- CMOS (AC) and TTL (ACT) voltage level inputs
- 50Ω incident wave switching
- Center-pin V_{CC} and ground configuration to minimize high-speed switching noise
- I_{CC} category: MSI

DESCRIPTION

The 74AC/ACT11824 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The AC/ACT11824 is a 9-bit wide buffered inverting register with Clock Enable and Master Reset which are ideal for parity bus interfacing in high-performance microprogrammed systems.

74AC/ACT11824

9-Wide D-Type Flip-Flop with Reset and Enable; Positive-Edge Trigger; 3-State; INV

Objective Specification

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS $T_A = 25^\circ\text{C}; \text{GND} = 0\text{V};$ $V_{CC} = 5.0\text{V}$	TYPICAL		UNIT
			AC	ACT	
t_{PLH} / t_{PHL}	Propagation delay CP to \bar{Q}_n	$C_L = 50\text{pF}$	6.0	8.5	ns
C_{PD}	Power dissipation capacitance per flip-flop ¹	$f = 1\text{MHz};$ $C_L = 50\text{pF}$	Enabled: 75 Disabled: 65	100 80	pF
C_{IN}	Input capacitance	$V_I = 0\text{V}$ or V_{CC}	4.5	4.5	pF
C_{OUT}	Output capacitance	$V_O = 0\text{V}$ or V_{CC} : Disabled	10	10	pF
I_{LATCH}	Latch-up current	Per Jeduc JC40.2 Standard 17	500	500	mA
f_{MAX}	Maximum clock frequency; CP to \bar{Q}_n	$C_L = 50\text{pF}$	125	100	MHz

Note:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_I + \sum (C_L \times V_{CC}^2 \times f_O) \text{ where:}$$

f_I = input frequency in MHz, C_L = output load capacitance in pF,

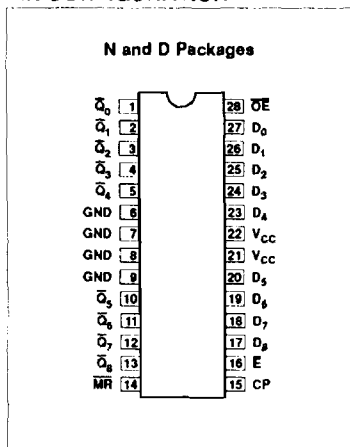
f_O = output frequency in MHz, V_{CC} = supply voltage in V,

$\sum (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

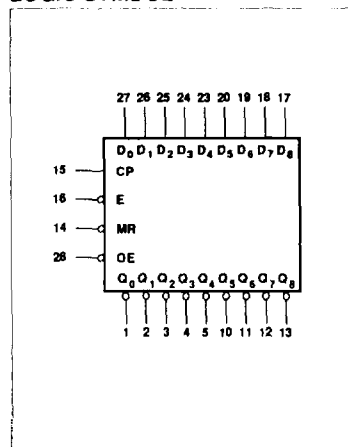
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
28-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11824N 74ACT11824N
28-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11824D 74ACT11824D

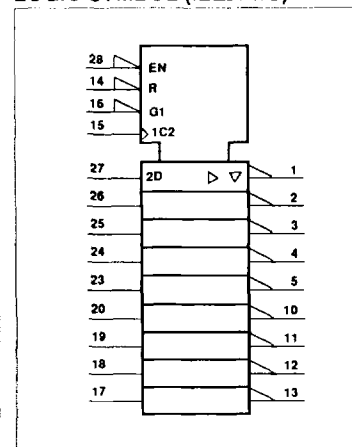
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



9-Wide D-Type Flip-Flop with Reset and Enable; Positive-Edge Trigger; 3-State; INV

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PIN DESCRIPTION

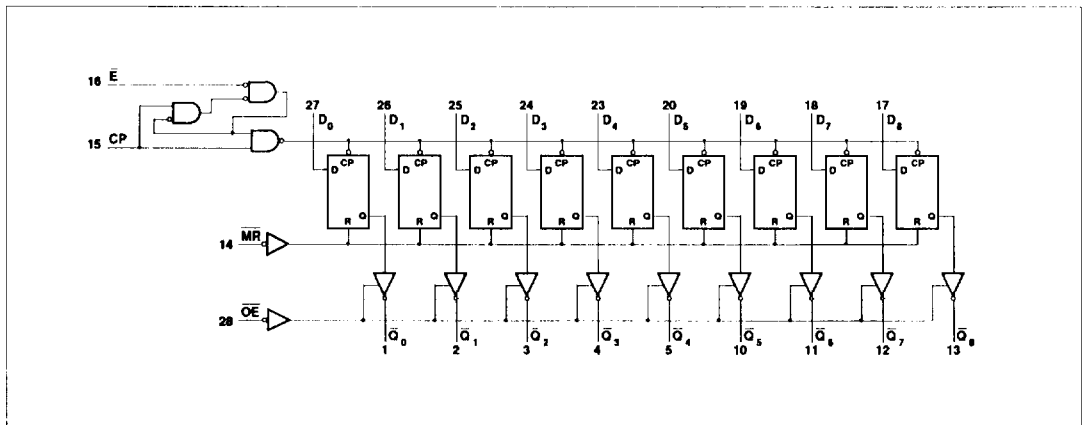
PIN NUMBER	SYMBOL	NAME AND FUNCTION
28	\overline{OE}	Output enable input (active-Low)
15	CP	Clock input
16	\overline{E}	Clock enable input (active-Low)
14	\overline{MR}	Master reset input (active-Low)
1, 2, 3, 4, 5, 10, 11, 12, 13	$D_0 - D_8$	Data inputs
27, 26, 25, 24, 23, 20, 19, 18, 17	$\overline{Q}_0 - \overline{Q}_8$	Data outputs
6, 7, 8, 9	GND	Ground (0V)
21, 22	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS					OUTPUTS
\overline{OE}	\overline{MR}	\overline{E}	CP	D_n	\overline{Q}_n
L	L	X	X	X	H
L	H	L	↑	l	H
L	H	L	↑	h	L
L	H	H	X	X	No change
H	X	X	X	X	Z

H = High voltage level
 h = High voltage level one setup time prior to the Low-to-High clock transition
 L = Low voltage levels
 l = Low voltage level one setup time prior to the Low-to-High clock transition
 X = Don't Care
 ↑ = Low-to-High clock transition

LOGIC DIAGRAM



9-Wide D-Type Flip-Flop with Reset and Enable; Positive-Edge Trigger; 3-State; INV

74AC/ACT11824

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11824			74ACT11824			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0 ¹	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta V/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:

- No electrical or switching characteristics are specified at $V_{CC} < 3V$. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS¹

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK} or V_I	DC input diode current ²	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to $V_{CC} + 0.5$	V
I_{OK} or V_O	DC output diode current ²	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to $V_{CC} + 0.5$	V
I_O	DC output source or sink current per output pin	$V_O = 0$ to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±225	mA
	DC ground current		±225	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C: derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C: derate linearly by 6mW/K	400	mW

NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

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DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	V _{CC}	74AC11824				74ACT11824				UNIT	
				T _A = +25°C		T _A = -40°C to +85°C		T _A = +25°C		T _A = -40°C to +85°C			
				V	Min	Max	Min	Max	Min	Max	Min		Max
V _{IH}	High-level input voltage		3.0	2.10		2.10						V	
			4.5	3.15		3.15		2.0		2.0			
			5.5	3.85		3.85		2.0		2.0			
V _{IL}	Low-level input voltage		3.0		0.90		0.90					V	
			4.5		1.35		1.35		0.8		0.8		
			5.5		1.65		1.65		0.8		0.8		
V _{OH}	High-level output voltage	V _I = V _{IL} or V _{IH}	I _{OH} = -50μA	3.0	2.9		2.9					V	
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I _{OH} = -4mA	3.0	2.58		2.48						
				4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
				5.5			3.85				3.85		
V _{OL}	Low-level output voltage	V _I = V _{IL} or V _{IH}	I _{OL} = 50μA	3.0		0.1		0.1				V	
				4.5		0.1		0.1		0.1			0.1
				5.5		0.1		0.1		0.1			0.1
			I _{OL} = 12mA	3.0	0.36		0.44						
				4.5	0.36		0.44		0.36		0.44		
				5.5	0.36		0.44		0.36		0.44		
				5.5			1.65				1.65		
I _I	Input leakage current	V _I = V _{CC} or GND	5.5		±0.1		±1.0		±0.1		±1.0	μA	
I _{OZ}	3-State output off-state current	V _I = V _{IL} or V _{IH} ; V _O = V _{CC} or GND	5.5		±0.5		±5.0		±0.5		±5.0	μA	
I _{CC}	Quiescent supply current	V _I = V _{CC} or GND, I _O = 0	5.5		8.0		80		8.0		80	μA	
ΔI _{CC}	Supply current, TTL inputs High ²	One input at 3.4V, other inputs at V _{CC} or GND	5.5						0.9		1.0	mA	

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.