DALLAS SEMICONDUCTOR

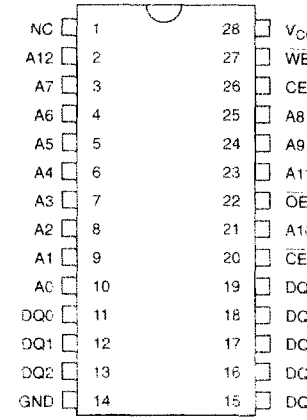
DS2064
8K x 8 Static RAM

FEATURES

- Low power CMOS design
- Standby current

  50 nA max at $t_A = 25°C$ $V_{CC} = 3.0V$
  100 nA max at $t_A = 25°C$ $V_{CC} = 5.5V$
  1 µA max at $t_A = 60°C$ $V_{CC} = 5.5V$
- Full operation for V_{CC} = 4.5V to 5.5V
- Data Retention Voltage = 5.5V to 2.0V
- Access time equals 200 ns at 5.0V
- Operating temperature range of –40°C to +85°C
- Full static operation
- TTL compatible inputs and outputs
- Available in 28–pin DIP and 28–pin SOIC packages
- Suitable for both battery operated and battery backup applications

PIN ASSIGNMENT



DS2064–200 28–PIN DIP (600 MIL)
DS2064S–200 28–PIN SOIC (330 MIL)

PIN DESCRIPTION

A0–A12	–	Address Inputs
DQ0–DQ7	–	Data Input/Output
$\overline{CE1}$, CE2	–	Chip Enable Inputs
$\overline{WE}$	–	Write Enable Input
$\overline{OE}$	–	Output Enable Input
V_{CC}	–	5V Power Supply Input
GND	–	Ground
NC	–	No Connection

DESCRIPTION

The DS2064 is a 65536–bit low power, fully static random access memory organized as 8192 words by eight bits using CMOS technology. The device operates from a single power supply with a voltage input between 4.5V and 5.5V. The chip enable inputs ($\overline{CE1}$ and CE2) are used for device selection and can be used in order to achieve the minimum standby current mode, which facilitates both battery operate and battery backup applications. The device provides fast access time of 200 ns and is most suitable for low power applications where battery operation or battery backup for nonvolatility is required. The DS2064 is a JEDEC–standard 8K x 8 SRAM and is pin–compatible with ROM and EPROM of similar density.