184pin Low Profile Registered DDR SDRAM DIMM

Based on 128Mx4 DDR SDRAM C Die device

Features

• 184 Dual In-Line Registered Memory Module (RDIMM)
• Registered DDR DIMM based on 90nm 512Mb Die C device organized as 128Mx4 (NT5DS128M4CG-5T).
• Performance:

	PC3200	Unit
Speed Sort	5T	
DIMM $\overline{CAS}$ Latency	3	
f_{CK} Clock Frequency	200	MHz
t_{CK} Clock Cycle	5	ns
f_{DQ} DQ Burst Frequency	400	MHz

• Intended for 200MHz applications
• Inputs and outputs are SSTL-2 compatible
• Error Check Correction (ECC) support
• Phase lock loop (PLL) clock driver to reducing clock loading
• Registered inputs with one clock delay
• $V_{DD} = V_{DDQ} = 2.6V \pm 0.1V$
• SDRAMs have 4 internal banks for concurrent operation
• Differential clock inputs
• Data is read or written on both clock edges
• DRAM DLL aligns DQ and DQS transitions with clock transitions
• Address and control signals are fully synchronous to positive clock edge
• Programmable Operation:
  - DIMM $\overline{CAS}$ Latency: 3
  - Burst Type: Sequential or Interleave
  - Burst Length: 2, 4, 8
  - Operation: Burst Read and Write
• Auto Refresh (CBR) and Self Refresh Modes
• Automatic and controlled precharge commands
• 7.8 µs Max. Average Periodic Refresh Interval
• Serial Presence Detect EEPROM
• Gold contacts on modules
• SDRAMs are packaged in 60-ball BGA packages
• RoHS compliant

Description

NT1GD72S4PC0FV and NT2GD72S4NC0FV are registered 184-Pin Double Data Rate (DDR) Synchronous DRAM Dual In-Line Memory Module (DIMM) with ECC organized. NT1GD72S4PC0FV has a single rank using eighteen 128Mx4 BGA devices. NT2GD72S4NC0FV is double rank using thirty-six 128Mx4 BGA devices.

Depending on the speed grade, these DIMMs are intended for use in applications operating up to 200 MHz clock speeds and achieves high-speed data transfer rates of up to 400 MHz. Prior to any access operation, the device $\overline{CAS}$ latency and burst/length/operation type must be programmed into the DIMM by address inputs and I/O inputs BA0 and BA1 using the mode register set cycle.

The DIMM uses a serial EEPROM and through the use of a standard IIC protocol the serial presence-detect implementation (SPD) can be accessed. The first 128 bytes of the SPD data are programmed with the module characteristics as defined by JEDEC.

Ordering Information

Part Number	Organization	Speed			Power	Leads
NT1GD72S4PC0FV-5T	128Mx72	DDR400	PC3200 3-3-3	200MHz (5ns @ CL = 3)	2.6V	Gold
NT2GD72S4NC0FV-5T	256Mx72	DDR400	PC3200 3-3-3	200MHz (5ns @ CL = 3)	2.6V	Gold

Note: The registered inputs will add 1 initial clock delay to all modules

For the closest sales office or information, please visit: www.nanya.com

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Pin Description

CK0, CK1, CK2, $\overline{CK0}$, $\overline{CK1}$, $\overline{CK2}$	Differential Clock Inputs.	DQ0-DQ63	DIMM memory data bus
CKE0, CKE1	Clock Enable	DQS0-DQS8	Bidirectional data strobes
$\overline{RAS}$	Row Address Strobe	DQS9-DQS17	Data strobes
$\overline{CAS}$	Column Address Strobe	V_{DD}	Positive power supply
$\overline{WE}$	Write Enable	V_{DDQ}	I/O Driver positive power supply
$\overline{S0}$,$\overline{S1}$	Chip Select	V_{SS}	Ground
A0-A12	Address Bus	NC/NU	No Connect / Not Useable
A10/AP	Address Input/Auto-precharge	SCL	IIC serial bus clock for EEPROM
BA0, BA1	SDRAM Bank Address Inputs	SDA	IIC serial bus data line for EEPROM
V_{REF}	Ref. Voltage for SSTL_2 inputs	SA0-2	IIC slave address select for EEPROM
CB0-CB7	DIMM ECC check bits	V_{DDSPD}	Serial EEPROM positive power supply
V_{DDID}	V_{DD} Identification flag.	$\overline{RESET}$	Reset pin (force register outputs low)

Pinout

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	V_{REF}	93	V_{SS}	32	A5	124	V_{SS}	62	V_{DDQ}	154	$\overline{RAS}$
2	DQ0	94	DQ4	33	DQ24	125	A6	63	$\overline{WE}$	155	DQ45
3	V_{SS}	95	DQ5	34	V_{SS}	126	DQ28	64	DQ41	156	V_{DDQ}
4	DQ1	96	V_{DDQ}	35	DQ25	127	DQ29	65	$\overline{CAS}$	157	$\overline{S0}$
5	DQS0	97	DM0/DQS9	36	DQS3	128	V_{DDQ}	66	V_{SS}	158	NA, $\overline{S1}$*
6	DQ2	98	DQ6	37	A4	129	DM3/DQS12	67	DQS5	159	DM5/DQS14
7	V_{DD}	99	DQ7	38	V_{DD}	130	A3	68	DQ42	160	V_{SS}
8	DQ3	100	V_{SS}	39	DQ26	131	DQ30	69	DQ43	161	DQ46
9	NC	101	NC	40	DQ27	132	V_{SS}	70	V_{DD}	162	DQ47
10	$\overline{RESET}$	102	NC	41	A2	133	DQ31	71	NC	163	NC
11	V_{SS}	103	NC	42	V_{SS}	134	CB4	72	DQ48	164	V_{DDQ}
12	DQ8	104	V_{DDQ}	43	A1	135	CB5	73	DQ49	165	DQ52
13	DQ9	105	DQ12	44	CB0	136	V_{DDQ}	74	V_{SS}	166	DQ53
14	DQS1	106	DQ13	45	CB1	137	CK0	75	$\overline{CK2}$	167	NC
15	V_{DDQ}	107	DM1/DQS10	46	V_{DD}	138	$\overline{CK0}$	76	CK2	168	V_{DD}
16	CK1	108	V_{DD}	47	DQS8	139	V_{SS}	77	V_{DDQ}	169	DM6/DQS15
17	$\overline{CK1}$	109	DQ14	48	A0	140	DM8/DQS17	78	DQS6	170	DQ54
18	V_{SS}	110	DQ15	49	CB2	141	A10	79	DQ50	171	DQ55
19	DQ10	111	CKE1	50	V_{SS}	142	CB6	80	DQ51	172	V_{DDQ}
20	DQ11	112	V_{DDQ}	51	CB3	143	V_{DDQ}	81	V_{SS}	173	NC
21	CKE0	113	NC	52	BA1	144	CB7	82	V_{DDID}	174	DQ60
22	V_{DDQ}	114	DQ20	KEY		KEY		83	DQ56	175	DQ61
23	DQ16	115	A12	53	DQ32	145	V_{SS}	84	DQ57	176	V_{SS}
24	DQ17	116	V_{SS}	54	V_{DDQ}	146	DQ36	85	V_{DD}	177	DM7/DQS16
25	DQS2	117	DQ21	55	DQ33	147	DQ37	86	DQS7	178	DQ62
26	V_{SS}	118	A11	56	DQS4	148	V_{DD}	87	DQ58	179	DQ63
27	A9	119	DM2/DQS11	57	DQ34	149	DM4/DQS13	88	DQ59	180	V_{DDQ}
28	DQ18	120	V_{DD}	58	V_{SS}	150	DQ38	89	V_{SS}	181	SA0
29	A7	121	DQ22	59	BA0	151	DQ39	90	NU	182	SA1
30	V_{DDQ}	122	A8	60	DQ35	152	V_{SS}	91	SDA	183	SA2
31	DQ19	123	DQ23	61	DQ40	153	DQ44	92	SCL	184	V_{DDSPD}

* For 2G RDIMM only

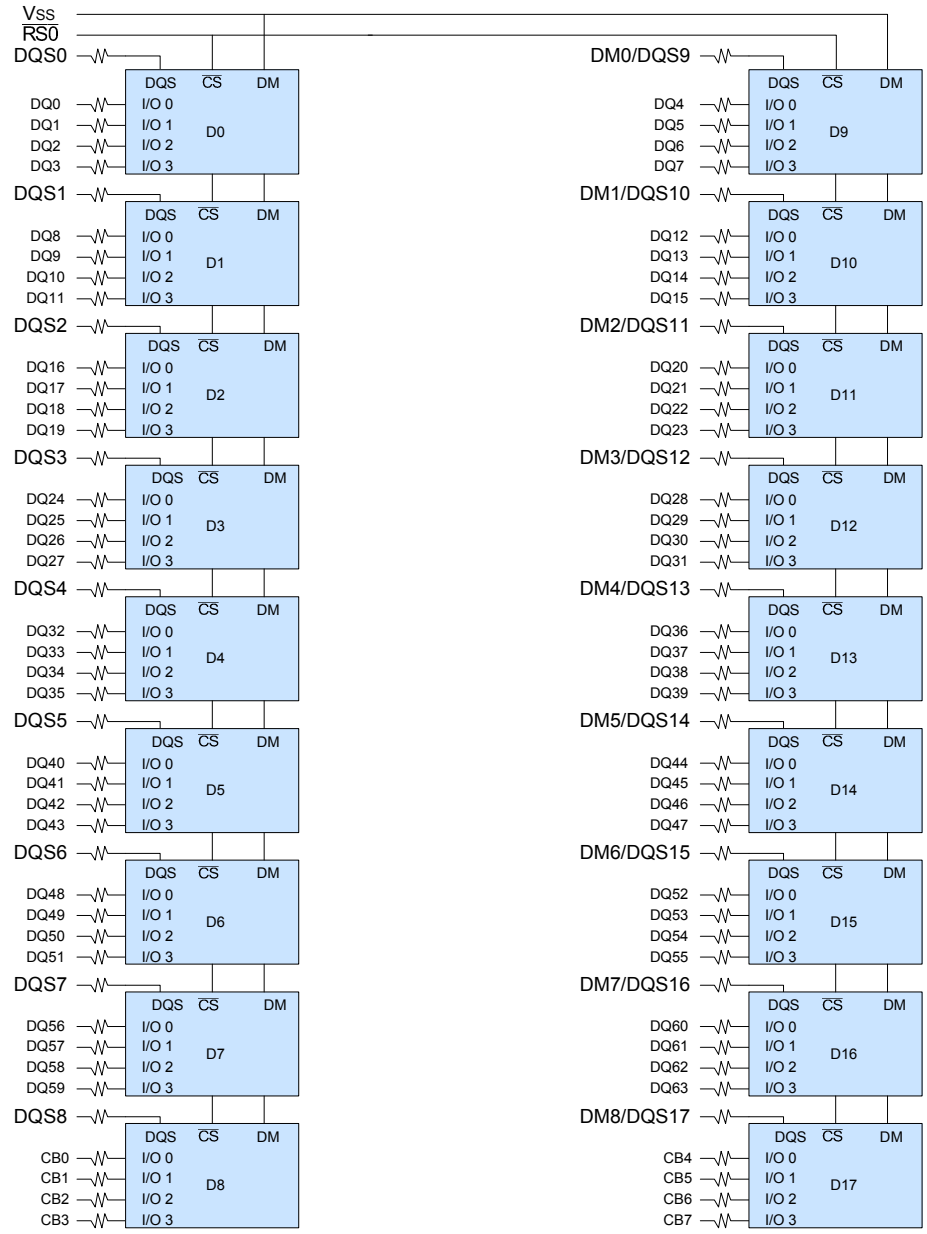
Input/Output Functional Description

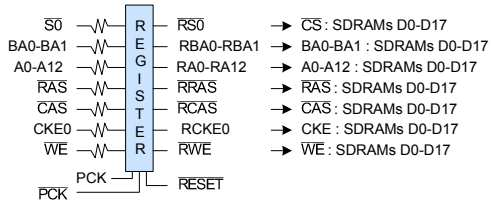
Symbol	Type	Polarity	Function
CK0, CK1, CK2, $\overline{CK0}$, $\overline{CK1}$, $\overline{CK2}$	(SSTL)	Cross point	The system clock inputs. All address and command lines are sampled on the cross point of the rising edge of CK and falling edge of CK. A Delay Locked Loop (DLL) circuit is driven from the clock inputs and output timing for read operations is synchronized to the input clock.
CKE0, CKE1	(SSTL)	Active High	Activates the DDR SDRAM CK signal when high and deactivates the CK signal when low. By deactivating the clocks, CKE low initiates the Power Down mode or the Self Refresh mode.
$\overline{S0}$, $\overline{S1}$*	(SSTL)	Active Low	Enables the associated DDR SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue. Physical Bank 0 is selected by S0.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	(SSTL)	Active Low	When sampled at the positive rising edge of the clock, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ define the operation to be executed by the SDRAM.
V_{REF}	Supply		Reference voltage for SSTL-2 inputs
V_{DDQ}	Supply		Isolated power supply for the DDR SDRAM output buffers to provide improved noise immunity
BA0, BA1	(SSTL)	-	Selects which SDRAM bank is to be active.
A0 - A9 A10/AP A11-A12	(SSTL)	-	During a Bank Activate command cycle, A0-A12 defines the row address (RA0-RA12) when sampled at the rising clock edge. During a Read or Write command cycle, A0-A11 defines the column address (CA0-CA11) when sampled at the rising clock edge. In addition to the column address, AP is used to invoke auto-precharge operation at the end of the Burst Read or Write cycle. If AP is high, auto-precharge is selected and BA0/BA1 defines the bank to be precharged. If AP is low, auto-precharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA0/BA1 to control which bank(s) to precharge. If AP is high all 4 banks will be precharged regardless of the state of BA0/BA1. If AP is low, then BA0/BA1 are used to define which bank to pre-charge.
DQ0 - DQ63	(SSTL)	-	Data and Check Bit input/output pins operate in the same manner as on conventional DRAMs.
DQS0 – DQS8, DQS9 – DQS17	(SSTL)	Active High	Data strobes: Output with read data, input with write data. Edge aligned with read data, centered on write data. Used to capture write data.
CB0 – CB7	(SSTL)	-	Data Check Bit Input/Output pins. Used on ECC modules and is not used on x64 modules.
DM0 – DM8	Input	Active High	The data write masks, associated with one data byte. In Write mode, DM operates as a byte mask by allowing input data to be written if it is low but blocks the write operation if it is high. In Read mode, DM lines have no effect. DM8 is associated with check bits CB0-CB7, and is not used on x64 modules.
V_{DD}, V_{SS}	Supply		Power and ground for the DDR SDRAM input buffers and core logic
SA0 – SA2		-	Address inputs. Connected to either V_{DD} or V_{SS} on the system board to configure the Serial Presence Detect EEPROM address.
SDA		-	This bi-directional pin is used to transfer data into or out of the SPD EEPROM. A resistor must be connected from the SDA bus line to V_{DD} to act as a pull-up.
SCL		-	This signal is used to clock data into and out of the SPD EEPROM. A resistor may be connected from the SCL bus time to V_{DD} to act as a pull-up.
V_{DDSPD}	Supply		Serial EEPROM positive power supply.

* For 2G RDIMM only

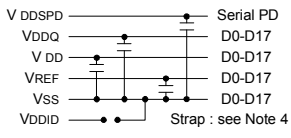
Functional Block Diagram

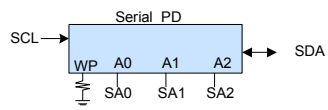
1 Rank, 18 devices, 128Mx4 DDR SDRAMs





Notes :
1. DQ-to-I/O wiring may be changed within a byte.
2. DQ/DQS/DM/CKE/CS relationships are maintained as shown.
3. DQ/DQS resistors are 22 Ohms.
4. V_{DDID} strap connections (for memory device V_{DD},V_{DDQ}):
   STRAP OUT (OPEN): $V_{DD} = V_{DDQ}$
   STRAP IN (V_{SS}): V_{DD} is not equal to V_{DDQ}
5. Address and control resistors are 22 Ohms.

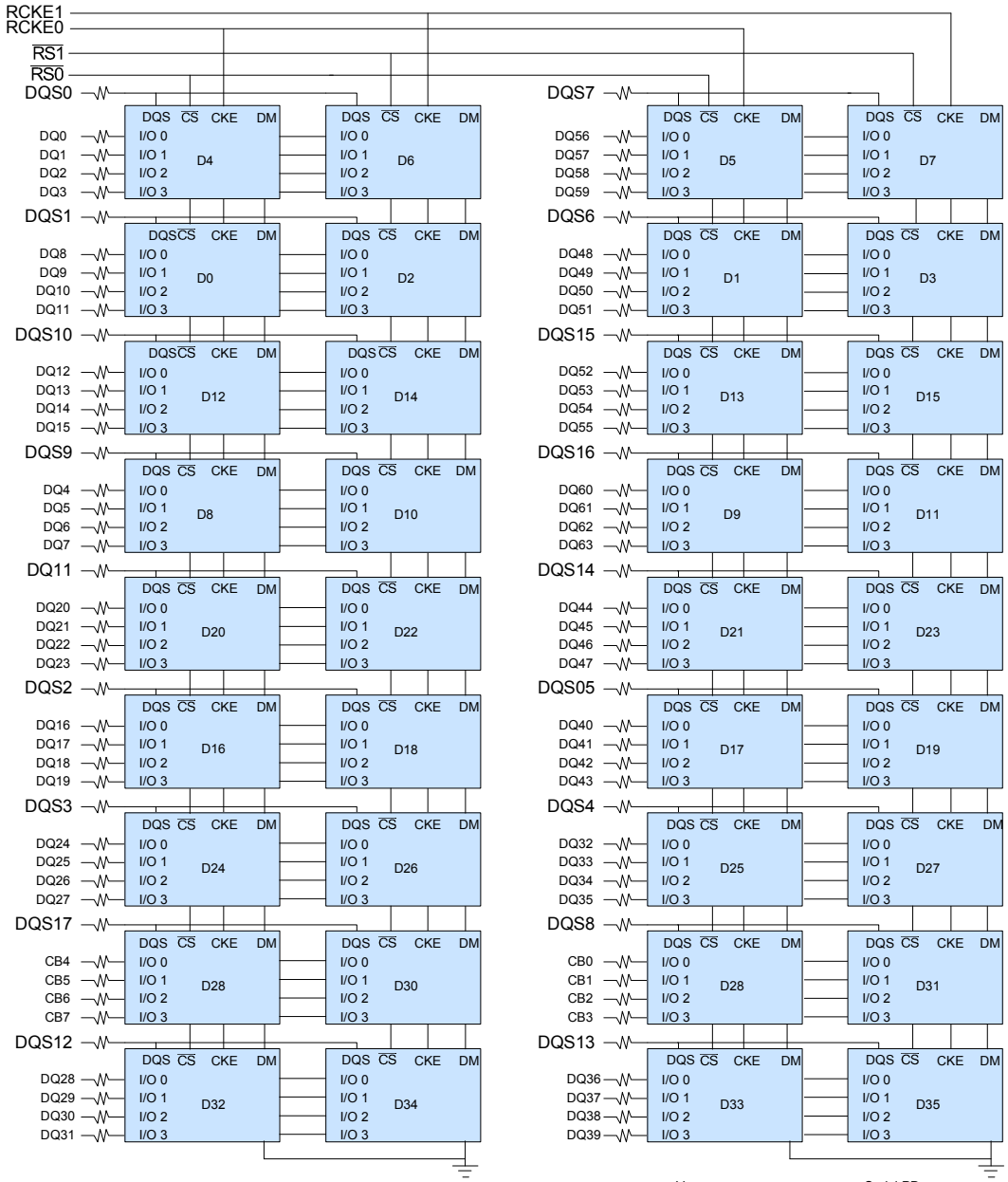




CK0, CK0 --------- PLL*
* Wire per Clock Loading Table/Wiring Diagrams

Functional Block Diagram

2 Rank, 36 devices, 128Mx4 DDR SDRAMs



Notes :
1. DQ-to-I/O wiring may be changed within a byte.
2. DQ/DQS/DM/CKE/CS relationships are maintained as shown.
3. DQ/DQS resistors are 22 Ohms.
4. V_{DDID} strap connections (for memory device V_{DD},V_{DDQ}):
   STRAP OUT (OPEN): $V_{DD} = V_{DDQ}$
   STRAP IN (V_{SS}): V_{DD} is not equal to V_{DDQ}
5. Address and control resistors are 22 Ohms.
6. Each Chip Select and CKE pair alternate between decks for thermal enhancement

Serial Presence Detect (1/2)

Byte	Description	Value		Hex		Note
		1GB	2GB	1GB	2GB	
0	Number of Serial PD Bytes Written during Production	128		80		
1	Total Number of Bytes in Serial PD device	256		08		
2	Fundamental Memory Type	DDR SDRAM		07		
3	Number of Row Addresses on Assembly	13		0D		
4	Number of Column Addresses on Assembly	12		0C		
5	Number of DIMM Bank	1	2	01	02	
6	Data Width of Assembly	x72		48		
7	Data Width of Assembly (cont')	x72		00		
8	Voltage Interface Level of this Assembly	SSTL 2.5V		04		
9	DDR SDRAM Device Cycle Time	5.0ns		50		
10	DDR SDRAM Device Access Time from Clock	0.65ns		65		
11	DIMM Configuration Type	ECC		02		
12	Refresh Rate/Type	SR/1x(7.8u μs)		82		
13	Primary DDR SDRAM Width	X4		04		
14	Error Checking DDR SDRAM Device Width	X4		04		
15	DDR SDRAM Device Attr: Min CLK Delay, Random Col Access	1 Clock		01		
16	DDR SDRAM Device Attributes: Burst Length Supported	2,4,8		0E		
17	DDR SDRAM Device Attributes: Number of Device Banks	4		04		
18	DDR SDRAM Device Attributes: CAS Latencies Supported	2.5/3		18		
19	DDR SDRAM Device Attributes: CS Latency	0		01		
20	DDR SDRAM Device Attributes: WE Latency	1		02		
21	DDR SDRAM Device Attributes	Differential Clock, PLL, REGISTER		26		
22	DDR SDRAM Device Attributes: General	±0.2V Voltage Tolerance		C0		
23	Minimum Clock Cycle	6.0ns		60		
24	Maximum Data Access Time (t_{AC}) from Clock at CL=2	0.70ns		70		
25	Minimum Clock Cycle Time at CL=1	N/A		00		
26	Maximum Data Access Time from Clock at CL=1	N/A		00		
27	Minimum Row Precharge Time (t_{RP})	15ns		3C		
28	Minimum Row Active to Row Active delay (t_{RRD})	10ns		28		
29	Minimum RAS to CAS delay (t_{RCD})	15ns		3C		
30	Minimum RAS Pulse Width (t_{RAS})	40ns		28		
31	Module Bank Density	1GB		01		
32	Address and Command Setup Time Before Clock	0.60ns		60		
33	Address and Command Hold Time After Clock	0.60ns		60		
34	Data Input Setup Time Before Clock	0.40ns		40		
35	Data Input Hold Time After Clock	0.40ns		40		

Serial Presence Detect (2/2)

Byte	Description	Value		Hex		Note
		1GB	2GB	1GB	2GB	
36-40	Reserved	Undefined		00		
41	Minimum Active/Auto-refresh Time (t_{RC})	55ns		37		
42	Auto-refresh to Active/Auto-refresh Command Period (t_{RFC})	70ns		46		
43	Max Cycle Time ($t_{CK\ max}$)	12ns		30		
44	Maximum DQS-DQ Skew Time (t_{DQSQ})	0.4ns		28		
45	Maximum Read Data Hold Skew Factor (t_{QHS})	0.5ns		50		
46	Superset Information (may be used in future)	Undefined		00		
47	DIMM Height	28.57mm		01		
48-61	Superset Information (may be used in future)	Undefined		00		
62	SPD Revision	1.0		10		
63	Checksum Data	Checksum		59	5A	
64-71	Manufacturer's JEDEC ID Code	0B Hex bank 3		7F7F7F0B 00000000		
72-255	Reserved	--		--		

Note:

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{IN}, V_{OUT}	Voltage on I/O pins relative to V_{SS}	-0.5 to V_{DDQ} +0.5	V
V_{IN}	Voltage on Inputs relative to V_{SS}	-1.0 to +3.6	V
V_{DD}	Voltage on V_{DD} supply relative to V_{SS}	-1.0 to +3.6	V
V_{DDQ}	Voltage on V_{DDQ} supply relative to V_{SS}	-1.0 to +3.6	V
T_A	Operating Temperature (Ambient)	0 to +70	℃
T_{STG}	Storage Temperature (Plastic)	-55 to +150	℃
P_D	Power Dissipation (per device component)	1	W
I_{OUT}	Short Circuit Output Current	50	mA

Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics and Operating Conditions

T_A= 0℃ ~ 70℃; V_{DDQ}= V_{DD}= 2.6V±0.1V

Symbol	Parameter	Min	Max	Units	Notes
VDD	Supply Voltage	2.5	2.7	V	
VDDQ	I/O Supply Voltage	2.5	2.7	V	
VSS, VSSQ	Supply Voltage, I/O Supply Voltage	0	0	V	
VREF	I/O Reference Voltage	0.49 x VDDQ	0.51 x VDDQ	V	1
VTT	I/O Termination Voltage (System)	VREF - 0.04	VREF + 0.04	V	2
VIH (DC)	Input High (Logic1) Voltage	VREF + 0.15	VDD + 0.3	V	
VIL (DC)	Input Low (Logic0) Voltage	-0.3	VREF - 0.15	V	
VIN (DC)	Input Voltage Level, CK and $\overline{CK}$ Inputs	-0.3	VDDQ + 0.3	V	
VID (DC)	Input Differential Voltage, CK and $\overline{CK}$ Inputs	0.36	V DDQ + 0.6	V	3
II	Input Leakage Current Any input 0V ≤ VIN ≤ VDD; (All other pins not under test = 0V)	-2	2	μA	
IOZ	Output Leakage Current (DQs are disabled; 0V ≤ Vout ≤ VDDQ	-5	5	μA	
IOH	Output High Current (VOUT = 1.95V)	-16.2	-	mA	
IOL	Output Low Current (VOUT = 0.35V)	16.2	-	mA	

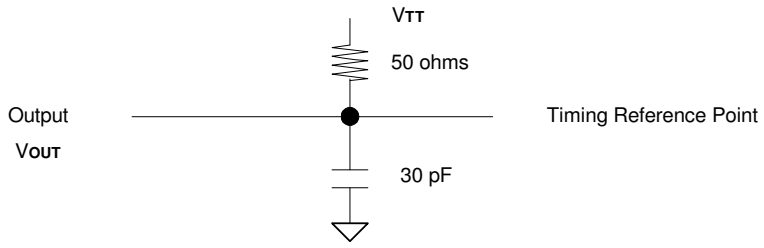
Note:
1. VREF is expected to be equal to 0.5 V DDQ of the transmitting device, and to track variations in the DC level of the same. Peak-to-peak noise on VREF may not exceed 2% of the DC value.
2. VTT is not applied directly to the DIMM. VTT is a system supply for signal termination resistors, is expected to be set equal to VREF, and must track variations in the DC level of VREF.
3. VID is the magnitude of the difference between the input level on CK and the input level on $\overline{CK}$.

AC Characteristics

Notes 1-6 apply to the following Tables; Electrical Characteristics and DC Operating Conditions, AC Operating Conditions, Operating, Standby, and Refresh Currents, and Electrical Characteristics and AC Timing.

1. All voltages referenced to V_{SS}.
2. Tests for AC timing, IDD, and electrical, AC and DC characteristics, may be conducted at nominal reference/supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.
3. Outputs measured with equivalent load. Refer to the AC Output Load Circuit below.
4. AC timing and IDD tests may use a V_{IL} to V_{IH} swing of up to 1.5V in the test environment, but input timing is still referenced to V_{REF} (or to the crossing point for CK, $\overline{CK}$), and parameter specifications are guaranteed for the specified AC input levels under normal use conditions. The minimum slew rate for the input signals is 1V/ns in the range between $V_{IL\,(AC)}$ and $V_{IH\,(AC)}$ unless otherwise specified.
5. The AC and DC input level specifications are as defined in the SSTL_2 Standard (i.e. the receiver effectively switches as a result of the signal crossing the AC input level, and remains in that state as long as the signal does not ring back above (below) the DC input LOW (HIGH) level.
6. Inputs are not recognized as valid until V_{REF} stabilizes. Exception: during the period before V_{REF} stabilizes, CKE <= $0.2V_{DDQ}$ is recognized as low.

AC Output Load Circuits



AC Operating Conditions

T_A = 0 ℃ ~ 70 ℃; V_{DDQ}= V_{DD}= 2.6V ± 0.1V

Symbol	Parameter/Condition	Min	Max	Unit	Notes
$V_{IH\,(AC)}$	Input High (Logic 1) Voltage.	V_{REF} + 0.31		V	
$V_{IL\,(AC)}$	Input Low (Logic 0) Voltage.		V_{REF} - 0.31	V	
$V_{ID\,(AC)}$	Input Differential Voltage, CK and $\overline{CK}$ Inputs	0.7	V_{DDQ} + 0.6	V	1
$V_{IX\,(AC)}$	Input Differential Pair Cross Point Voltage, CK and $\overline{CK}$ Inputs	(0.5* V_{DDQ}) - 0.2	(0.5* V_{DDQ}) + 0.2	V	2

1. V_{ID} is the magnitude of the difference between the input level on CK and the input level on $\overline{CK}$.
2. The value of V_{IX} is expected to equal $0.5*V_{DDQ}$ of the transmitting device and must track variations in the DC level of the same.

Operating, Standby, and Refresh Currents

T_A = 0 ℃ ~ 70 ℃; V_{DDQ}= V_{DD}= 2.6V ± 0.1V

Symbol	Parameter/Condition	PC3200 (-5T)		Unit
		1GB	2GB	
IDD0	Operating Current: one bank; active/precharge; t_{RC} = $t_{RC\ (MIN)}$; t_{CK} = $t_{CK\ (MIN)}$; DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	623	1118	mA
IDD1	Operating Current: one bank; active/read/precharge; Burst = 2; t_{RC} = $t_{RC\ (MIN)}$; CL=2.5; t_{CK} = $t_{CK\ (MIN)}$; I_{OUT} = 0mA; address and control inputs changing once per clock cycle	606	1116	mA
IDD2P	Precharge Power-Down Standby Current: all banks idle; power-down mode; CKE ≤ $V_{IL\ (MAX)}$; t_{CK} = $t_{CK\ (MIN)}$	255.7	385.0	mA
IDD2F	Precharge floating standby current: $\overline{CS}$ ≥ $V_{IH\ (MIN)}$; all banks idle; CKE ≥ $V_{IH\ (MIN)}$; t_{CK} = 5ns; address and control inputs changing once per clock cycle	405.1	699.2	mA
IDD2Q	Precharge quiet standby current: $\overline{CS}$ ≥ $V_{IH\ (MIN)}$; all banks idle; CKE ≥ $V_{IH\ (MIN)}$; t_{CK} = 5ns; address and other control inputs stable at ≥ $V_{IH(min)}$ or ≤ $V_{IL(max)}$.	245	361.8	mA
IDD3P	Active Power-Down Standby Current: one bank active; power-down mode; CKE ≤ $V_{IL\ (MAX)}$; t_{CK} = $t_{CK\ (MIN)}$	315.3	503.3	mA
IDD3N	Active Standby Current: one bank; active/precharge; CS ≥ $V_{IH\ (MIN)}$; CKE ≥ $V_{IH\ (MIN)}$; t_{RC} = $t_{RAS\ (MAX)}$; t_{CK} = $t_{CK\ (MIN)}$; DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	441.3	752.0	mA
IDD4R	Operating Current: one bank; Burst = 2; reads; continuous burst; address and control inputs changing once per clock cycle; DQ and DQS outputs changing twice per clock cycle; CL = 2.5; t_{CK} = $t_{CK\ (MIN)}$; I_{OUT} = 0mA	691	1276	mA
IDD4W	Operating Current: one bank; Burst = 2; writes; continuous burst; address and control inputs changing once per clock cycle; DQ and DQS inputs changing twice per clock cycle; CL=2.5; t_{CK} = $t_{CK\ (MIN)}$	575	1003	mA
IDD5	Auto-Refresh Current: t_{RC} = $t_{RFC\ (MIN)}$	1050	1964	mA
IDD6	Self-Refresh Current: CKE ≤ 0.2V	49.1	131.0	mA
IDD7	Operating Current: four bank; four bank interleaving with BL = 4, address and control inputs randomly changing; 50% of data changing at every transfer; t_{RC} = $t_{RC\ (min)}$; I_{OUT} = 0mA.	1731	3066	mA

Note: All IDD values are average values derived from measurements.

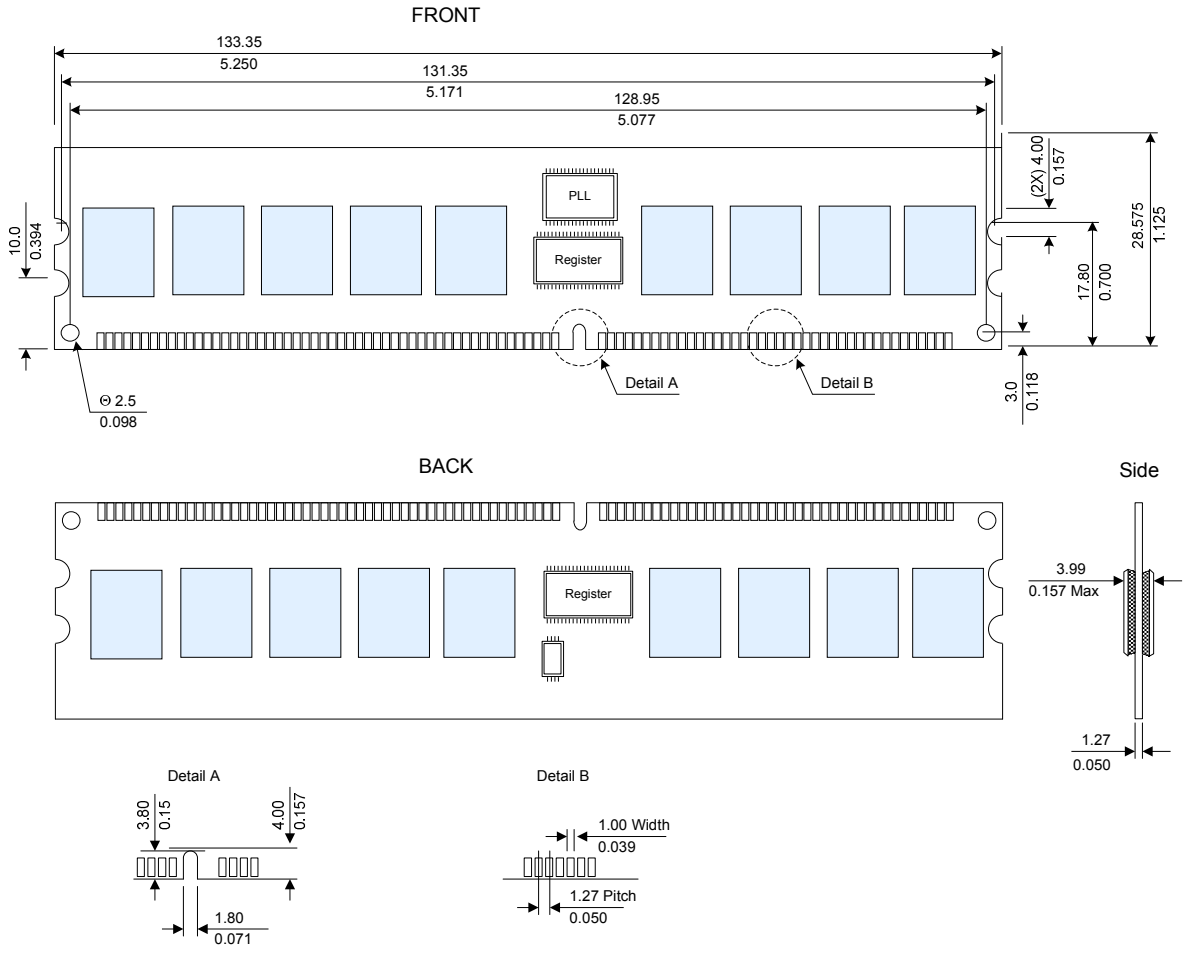
Electrical Characteristics & AC Timing – Absolute Specifications

(T_A = 0 ℃ ~ 70 ℃; V_{DDQ}= V_{DD}= 2.6V ± 0.1V)

Symbol	Parameter	Min.	Max.	Unit	Notes
tAC	DQ output access time from CK/$\overline{CK}$	-0.7	+0.7	ns	
tDQSCK	DQS output access time from CK/$\overline{CK}$	-0.6	+0.6	ns	
tCH	CK high-level width	0.45	0.55	t_{CK}	
tCL	CK low-level width	0.45	0.55	t_{CK}	
tHP	Minimum half clk period for any given cycle; defined by clk high (tCH) or clk low (tCL) time	tCH or tCL		t_{CK}	
tCK	Clock cycle time	5	8	ns	
tDH	DQ and DM input hold time	0.4		ns	
tDS	DQ and DM input setup time	0.4		ns	
tIPW	Control & Address Input pulse width (each input)	2.2		ns	
tDIPW	DQ and DM input pulse width (each input)	1.75		ns	
tHZ	DQ & DQS high-impedance time from CK/$\overline{CK}$		0.7	ns	
tLZ	DQ & DQS low-impedance time from CK/$\overline{CK}$	-0.7	0.7	ns	
tDQSQ	DQS-DQ skew (DQS & associated DQ signals)		0.4	ns	
tQHS	Data hold Skew Factor		0.5	ns	
tQH	Data output hold time from DQS	tHP - tQHS		ns	
tDQSS	Write command to 1st DQS latching transition	0.72	1.25	t_{CK}	
tDQSH	DQS input high pulse width (write cycle)	0.35		t_{CK}	
tDQSL	DQS input low pulse width (write cycle)	0.35		t_{CK}	
tDSS	DQS falling edge to CK setup time (write cycle)	0.2		t_{CK}	
tDSH	DQS falling edge hold time from CK (write cycle)	0.2		t_{CK}	
tMRD	Mode register set command cycle time	2		t_{CK}	
tWPRES	Write preamble setup time	0		ns	
tWPST	Write postamble	0.4	0.6	t_{CK}	
tWPRE	Write preamble	Max(0.25* tck,1.5)		ns	
tIH	Address and control input hold time (fast slew rate)	0.6		ns	
tIS	Address and control input setup time (fast slew rate)	0.6		ns	
tIH	Address and control input hold time (slow slew rate)	0.7		ns	
tIS	Address and control input setup time (slow slew rate)	0.7		ns	
tRPRE	Read preamble	0.9	1.1	t_{CK}	
tRPST	Read postamble	0.4	0.6	t_{CK}	
tRAS	Active to Pre-Charge command	40	70,000	ns	
tRC	Active to Active/Auto Refresh command period	55		ns	
tRFC	Auto Refresh to Active/Auto refresh command period	70		ns	
tRCD	Active to READ or WRITE delay	15		ns	
tRP	Pre-Charge command period	15		ns	
tRAP	Active to Auto Pre-Charge Delay	tRCD or tRAS min		ns	
tRRD	Active bank A to Active bank B command	10		ns	
tWR	Write recovery time	15		ns	
tWTR	Internal Write to Read command delay	2		t_{CK}	
tXSNR	Exit self refresh to a Non-read command	75		ns	
tXSRD	Exit self refresh to a Read command	200		t_{CK}	
tREFI	Average Period Refresh Interval		7.8	us	

Package Dimensions

1GB, Register ECC, 18 BGA devices



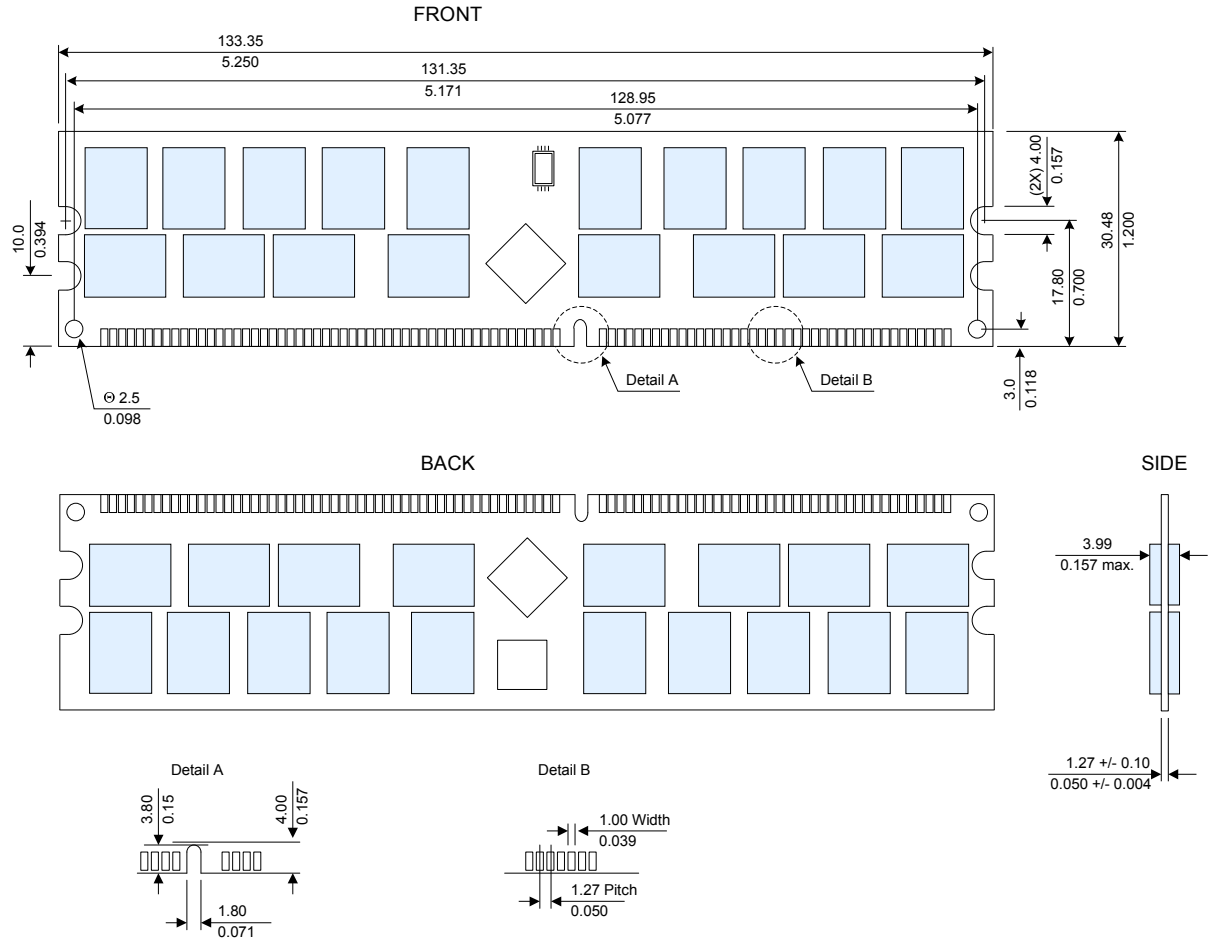
Note: All dimensions are typical with tolerances of +/- 0.15 (0.006) unless otherwise stated.

Units: Millimeters (Inches)

Note: For all drawings, devices are drawn as a reference only

Package Dimensions

2GB, Register ECC, 36 BGA devices



Note: All dimensions are typical with tolerances of +/- 0.15 (0.006) unless otherwise stated.

Units: Millimeters (Inches)

Note: For all drawings, devices are drawn as a reference only

Revision Log

Rev	Date	Modification
0.1	February 24, 2006	Initial Release.
0.2	March 7, 2007	Add 2GB spec.
1.0	April 20, 2007	Official Release.
1.1	July 13, 2006	Update typo on Module Organization in Page 2.

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