54F/74F402

Serial Data Polynomial Generator/Checker

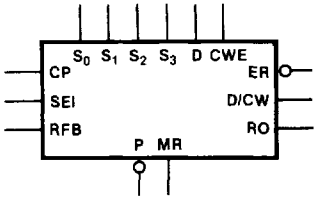
Description

The 'F402 expandable Serial Data Polynomial generator/checker is an expandable version of the 'F401. It provides an advanced tool for the implementation of the most widely used error detection scheme in serial digital handling systems. A 4-bit control input selects one-of-six generator polynomials. The list of polynomials includes CRC-16, CRC-CCITT and Ethernet, as well as three other standard polynomials (56^{th} order, 48^{th} order, 32^{nd} order). Individual clear and preset inputs are provided for floppy disk and other applications. The Error output indicates whether or not a transmission error has occurred. The CWG Control input inhibits feedback during check word transmission. The 'F402 is compatible with Fairchild Advanced Schottky TTL (FAST) devices and is fully compatible with all TTL families.

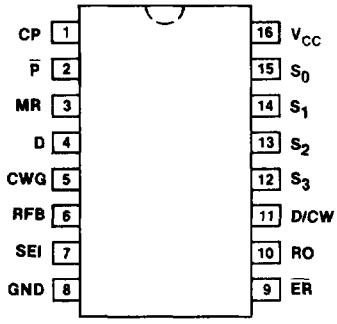
- **Guaranteed 30 MHz Data Rate**
- **Six Selectable Polynomials**
- **Other Polynomials Available**
- **Separate Preset and Clear Controls**
- **Expandable**
- **Automatic Right Justification**
- **Error Output Open Collector**
- **Typical Applications**
  - **Floppy and Other Disk Storage Systems**
  - **Digital Cassette and Cartridge Systems**
  - **Data Communication Systems**

Ordering Code: See Section 5

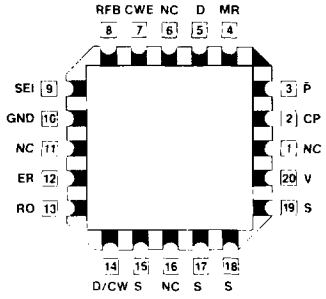
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
S_0-S_3	Polynomial Select Inputs	0.5/0.25
CWG	Check Word Generate Input	0.5/0.25
D/CW	Serial Data/Check Word	10/5(2.5)
D	Data Input	0.5/0.25
$\overline{ER}$	Error Output	*/10(5)
RO	Register Output	10/5(2.5)
CP	Clock Pulse	0.5/0.25
SEI	Serial Expansion Input	0.5/0.25
RFB	Register Feedback	0.5/0.25
MR	Master Reset	0.5/0.25
$\overline{P}$	Preset	0.5/0.25

*Open Collector

Functional Description

The 'F402 Serial Data Polynomial Generator/ Checker is an expandable 16-bit programmable device which operates on serial data streams and provides a means of detecting transmission errors. Cyclic encoding and decoding schemes for error detection are based on polynomial manipulation in modulo arithmetic. For encoding, the data stream (message polynomial) is divided by a selected polynomial. This division results in a remainder (or residue) which is appended to the message as check bits. For error checking, the bit stream containing both data and check bits is divided by the same selected polynomial. If there are no detectable errors, this division results in a zero remainder. Although it is possible to choose many generating polynomials of a given degree, standards exist that specify a small number of useful polynomials. The 'F402 implements the polynomials listed in Table 1 by applying the appropriate logic levels to the select pins S_0, S_1, S_2, and S_3.

The 'F402 consists of a 16-bit register, a Read Only Memory (ROM) and associated control circuitry as shown in the Block Diagram. The polynomial control code presented at inputs S_0, S_1, S_2, and S_3 is decoded by the ROM, selecting the desired polynomial or part of a polynomial by establishing shift mode operation on the register with Exclusive OR (XOR) gates at appropriate inputs. To generate the check bits, the data stream is entered via the Data Inputs (D), using the LOW-to-HIGH transition of the Clock Input (CP). This data is gated with the most significant Register Output (RO) via the Register Feedback Input (RFB), and controls the XOR gates. The Check Word Generate (CWG) must be held HIGH while the data is being entered. After the last data bit is entered, the CWG is brought LOW and the check bits are shifted out of the register(s) and appended to the data bits (no external gating is needed).

To check an incoming message for errors, both the data and check bits are entered through the D Input with the CWG Input held HIGH. The Error Output becomes valid after the last check bit has been entered into the 'F402 by a LOW-to-HIGH transition of CP, with the exception of the Ethernet polynomial (see Applications paragraph). If no detectable errors have occurred during the data transmission, the resultant internal register bits are all LOW and the Error Output ($\overline{ER}$) is HIGH. If a detectable error has occurred, $\overline{ER}$ is LOW. $\overline{ER}$ remains valid until the next LOW-to-HIGH transition of CP or until the device has been preset or reset.

A HIGH on the Master Reset Input (MR) asynchronously clears the entire register. A LOW on the Preset Input ($\overline{P}$) asynchronously sets the entire register with the exception of:

1) The Ethernet residue selection, in which the registers containing the non-zero residue are cleared;
2) The 56th order polynomial, in which the 8 least significant register bits of the least significant device are cleared; and,
3) Register S = 0, in which all bits are cleared.

Block Diagram

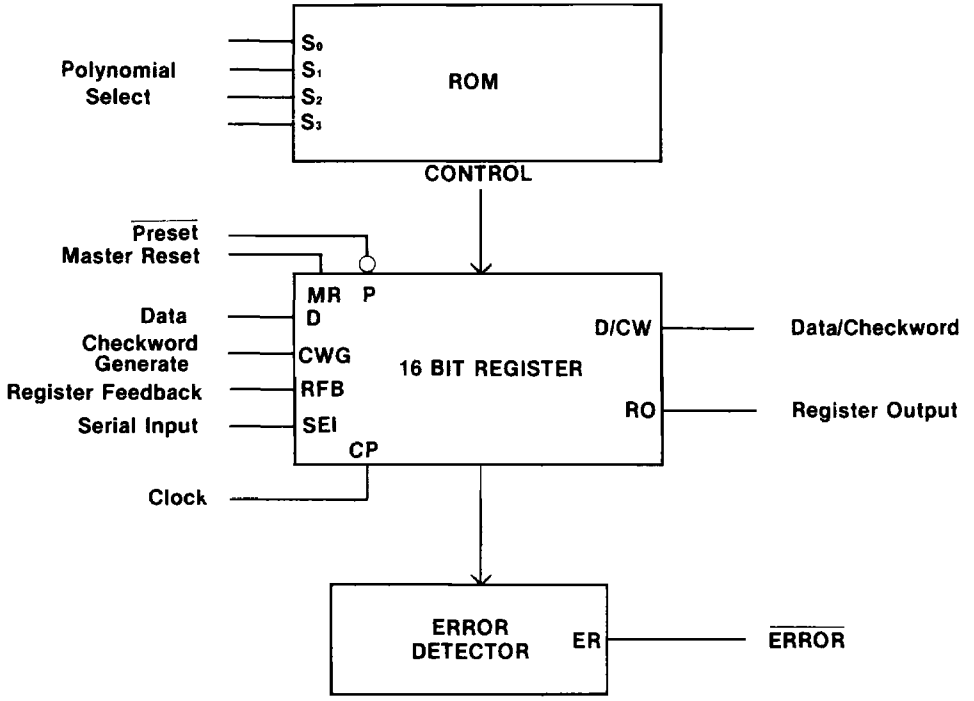


Table 1

Hex	Select Code S_3	S_2	S_1	S_0	Polynomial	Remarks
0	L	L	L	L	0	S = 0
C D	H H	H H	L L	L H	$X^{32}+X^{26}+X^{23}+X^{22}+X^{16}+$ $X^{12}+X^{11}+X^{10}+X^8+X^7+X^5+X^4+X^2+X+1$	Ethernet Polynomial
E F	H H	H H	H H	L H	$X^{32}+X^{31}+X^{27}+X^{26}+X^{25}+X^{19}+X^{16}+$ $X^{15}+X^{13}+X^{12}+X^{11}+X^9+X^7+X^6+X^5+X^4+X^2+X+1$	Ethernet Residue
7	L	H	H	H	$X^{16}+X^{15}+X^2+1$	CRC-16
B	H	L	H	H	$X^{16}+X^{12}+X^{12}+X^5+1$	CRC-CCITT
3 2 4 8	L L L H	L L H L	H H L L	H L L L	$X^{56}+X^{55}+X^{49}+X^{45}+X^{41}+$ $X^{39}+X^{38}+X^{37}+X^{36}+X^{31}+$ $X^{22}+X^{19}+X^{17}+X^{16}+X^{15}+X^{14}+X^{11}+X^9+$ X^5+X+1	56th Order
5 9 1	L H L	H L L	L L L	H H H	$X^{48}+X^{36}+X^{35}+$ $X^{23}+X^{21}+$ $X^{15}+X^{13}+X^8+X^2+1$	48th Order
6 A	L H	H L	H H	L L	$X^{32}+X^{23}+X^{21}+$ $X^{11}+X^2+1$	32nd Order

Table 2

Select Code	P_3	P_2	P_1	P_0	C_2	C_1	C_0	Polynomial
0	0	0	0	0	1	0	0	S = 0
C D	1 1	1 1	1 1	1 1	1 1	0 0	1 1	Ethernet Polynomial
E F	0 0	0 0	0 0	0 0	0 0	0 1	0 0	Ethernet Residue
7	1	1	1	1	1	0	0	CRC-16
B	1	1	1	1	1	0	0	CRC-CCITT
3 2 4 8	1 1 1 0	1 1 1 0	1 1 1 1	1 1 1 1	1 1 1 1	0 0 0 0	0 0 0 0	56th Order
5 9 1	1 1 1	1 1 1	1 1 1	1 1 1	1 1 1	0 0 0	0 0 0	48th Order
6 A	1 1	1 1	1 1	1 1	1 1	0 0	0 0	32nd Order

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		110	165	mA	V_{CC} = Max

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F T_A = +25°C, V_{CC} = +5.0 V, C_L = 50 pF			54F T_A, V_{CC} = Mil, C_L = 50 pF		74F T_A, V_{CC} = Com, C_L = 50 pF		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	30	45				30		MHz	3-1
t_{PLH} t_{PHL}	Propagation Delay CP to D/CW	8.5 10.5	15.0 18.0	19.0 23.0			9.5 9.0	21.0 24.0	ns	3-1 3-7
t_{PLH} t_{PHL}	Propagation Delay CP to RO	8.0 8.0	13.5 14.0	17.0 18.0			7.0 7.0	19.0 20.0	ns	3-1 3-7
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{ER}$	15.5 8.5	26.0 14.5	33.0 18.5			13.5 7.5	35.0 20.5	ns	3-1 3-7
t_{PLH} t_{PHL}	Propagation Delay $\overline{P}$ to D/CW	11.0 11.5	18.5 19.5	23.5 24.5			9.5 10.0	25.5 26.5	ns	3-1 3-8
t_{PLH}	Propagation Delay $\overline{P}$ to RO	9.5	16.0	20.5			8.5	22.5	ns	3-1 3-8
t_{PLH}	Propagation Delay $\overline{P}$ to $\overline{ER}$	10.0	17.0	21.5			9.0	23.5	ns	3-1 3-8
t_{PLH} t_{PHL}	Propatation Delay MR to D/CW	10.5 11.0	18.0 19.0	23.0 24.0			9.5 10.0	25.0 26.0	ns	3-1 3-11
t_{PHL}	Propagation Delay MR to RO	9.0	15.5	19.5			8.0	21.5	ns	3-1 3-11
t_{PLH}	Propagation Delay MR to $\overline{ER}$	16.5	28.0	35.5			14.5	37.5	ns	3-1 3-11
t_{PLH} t_{PHL}	Propagation Delay D to D/CW	6.0 7.5	10.5 12.0	13.5 16.0			5.0 6.5	15.0 18.0	ns	3-1 3-4
t_{PLH} t_{PHL}	Propagation Delay CWG to D/CW	6.5 7.0	11.0 12.0	14.0 15.5			5.5 6.0	15.5 17.5	ns	3-1 3-4
t_{PLH} t_{PHL}	Propagation Delay S_n to D/CW	11.5 9.5	19.5 16.0	24.5 20.0			10.5 8.5	26.5 22.0	ns	3-1 3-4

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F	54F	74F	Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\,V$	T_A, V_{CC} = Mil	T_A, V_{CC} = Com		
		Min Typ Max	Min Max	Min Max		
$t_s(H)$ $t_s(L)$	Set up Time, HIGH or LOW SEI to CP	4.5 4.5		5.0 5.0	ns	3-6
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW SEI to CP	0 0		0 0		
$t_s(H)$ $t_s(L)$	Set up Time, HIGH or LOW RFB to CP	11.0 11.0		12.0 12.0	ns	3-6
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW RFB to CP	0 0		0 0		
$t_s(H)$ $t_s(L)$	Set up Time, HIGH or LOW S_1 to CP	13.5 13.0		15.0 14.5	ns	3-6
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW S_1 to CP	0 0		0 0		
$t_s(H)$ $t_s(L)$	Set up Time, HIGH or LOW D to CP	9.0 9.0		10.0 10.0	ns	3-6
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW D to CP	0 0		0 0		
$t_s(H)$ $t_s(L)$	Set up Time, HIGH or LOW CWG to CP	7.0 5.5		8.0 6.5	ns	3-6
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW CWG to CP	0 0		0 0		
$t_w(H)$ $t_w(L)$	Clock Pulse Width HIGH or LOW	4.0 4.0		4.5 4.5	ns	3-7
$t_w(H)$	MR Pulse Width, HIGH	4.0		4.5	ns	3-11
$t_w(L)$	$\overline{P}$ Pulse Width, LOW	4.0		4.5	ns	3-11
t_{rec}	Recovery Time MR to CP	3.0		2.5	ns	3-6
t_{rec}	Recovery Time $\overline{P}$ to CP	5.0		6.0		

Applications

In addition to polynomial selection there are four other capabilities provided for in the 'F402 ROM. The first is set or clear selectability. The sixteen internal registers have the capability to be either set or cleared when $\overline{P}$ is brought LOW. This set or clear capability is done in four groups of 4 (see Table 2, P_0-P_3). The second ROM capability (C_0) is in determining the polarity of the check word. As is the case with the Ethernet polynomial the check word can be inverted when it is appended to the data stream or as is the case with the other polynomials, the residue is appended with no inversion. Thirdly, the ROM contains a bit (C_1) which is used to select the RFB input instead of the SEI input to be fed into the LSB. This is used when the polynomial selected is actually a residue (least significant) stored in the ROM which indicates whether the selected location is a polynomial or a residue. If the latter, then it inhibits the RFB input.

As mentioned previously, upon a successful data transmission, the CRC register has a zero residue. There is an exception to this, however, with respect to the Ethernet polynomial. This polynomial, upon a successful data transmission, has a non-zero residue in the CRC register (C7 04 DD 7B)$_{16}$. In order to provide a no-error indication, two ROM locations have been preloaded with the residue so that by selecting these locations and clocking the device one additional time, after the last check bit has been entered, will result in zeroing the CRC register. In this manner a no-error indication is achieved.

With the present mix of polynomials, the largest is 56th order requiring four devices while the smallest is 16th order requiring just one device. In order to accommodate multiplexing between high order polynomials (X 16th order) and lower order polynomials, a location of all zeros is provided. This allows the user to choose a lower order polynomial even if the system is configured for a higher order one.

The 'F402 expandable CRC generator checker contains 6 popular CRC polynomials, 2-16th Order, 2-32nd Order, 1-48th Order and 1-56th Order. The application diagram shows the 'F402 connected for a 56th Order polynomial. Also shown are the input patterns for other polynomials. When the 'F402 is used with a gated clock, disabling the clock in a HIGH state will ensure no erroneous clocking occurs when the clock is re-enabled. Preset and Master Reset are asynchronous inputs presetting the register to S or clearing to 0s respectively (note Ethernet residue and 56th Order select code 8, LSB, are exceptions to this).

To generate a CRC, the pattern for the selected polynomial is applied to the S inputs, the register is preset or cleared as required, clock is enabled, CWG is set HIGH, data is applied to D input, output data is on D/CW. When the last data bit has been entered, CWG is set LOW and the register is clocked for n bits (where n is the order of the polynomial). The clock may now be stopped if desired (holding CWG LOW and clocking the register will output zeros from D/CW after the residue has been shifted out).

To check a CRC, the pattern for the selected polynomial is applied to the S inputs, the register is preset or cleared as required, clock is enabled, CWG is set HIGH, the data stream including the CRC is applied to D input. When the last bit of the CRC has been entered, the $\overline{ER}$ output is checked: HIGH = error free data, LOW = corrupt data. The clock may now be stopped if desired.

To implement polynomials of lower order than 56th, select the number of packages required for the order of polynomial and apply the pattern for the selected polynomial to the S inputs (0000 on S inputs disables the package from the feedback chain).

Applications