ADE-207-054

HD153130F
Color Palette with Three Eight-Bit DAC Channels for High-Resolution CRTs

HITACHI

Preliminary
Rev. 0
Dec. 1991

The HD153130 stores color information and converts digital pixel data to analog color output signals. Fabricated using Hitachi's Hi-BiCMOS process, it includes high-speed logic, high-speed SRAM, and high-precision eight-bit D/A converters on a single chip. Color signals can be output at a maximum dot rate of 135 MHz, enabling non-interlaced display of color graphics on a high-resolution CRT with up to 1280 bits × 1024 rasters.

The input section includes a pixel data multiplexer, so that pixel data can be input in parallel at 1/4 or 1/2 the dot rate. The palette RAM stores 256 words × 24 bits. The digital-to-analog converter section has three high-precision eight-bit D/A converter channels. Up to 256 out of 16.77 million colors can be displayed simultaneously.

Comparators built into the analog output section can be used to check that a monitor is connected and to discriminate between monochrome and color monitors.

Features

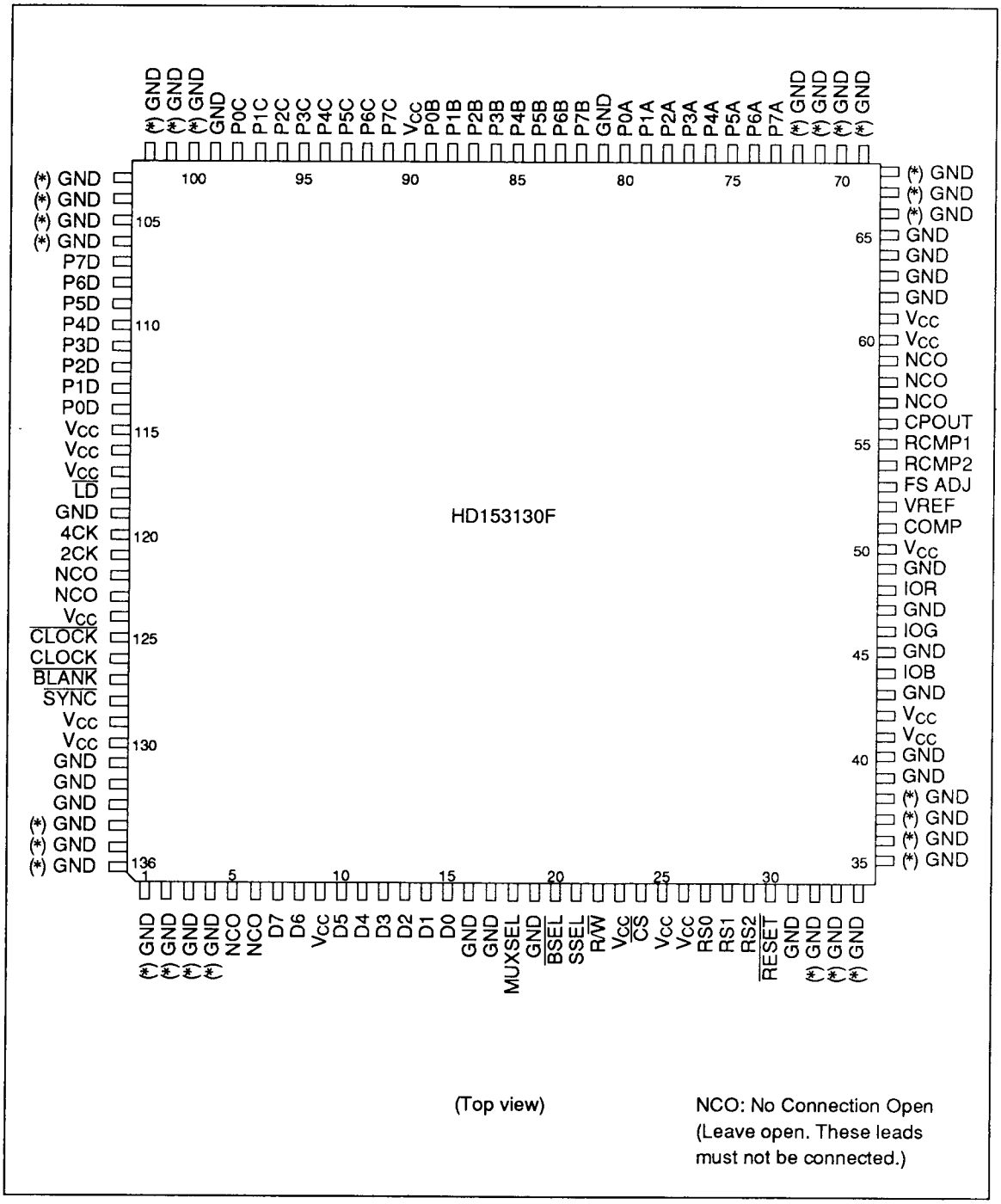
- On-chip eight-bit D/A converters: three channels.
- Maximum operating frequency: 110 or 135 MHz.
- Can simultaneously display 256 out of 16.77 million colors.
- Read mask function for display control.
- Interface conforms to VGA™ graphics standard.
- Composite signal can include the blanking and sync signals needed for CRT control.
- 4:1 or 2:1 input multiplexer; pixel data can be input at standard TTL level.
- Variable black level (0 or 7.5 IRE units)
- D/A converter output specifications conform to RS-343A.
- Compact surface-mountable 136-lead QFP package.

Ordering Information

Product Number	Maximum Clock Rate	Package
HD153130F	110 MHz	136-pin plastic QFP
HD153130F-135	135 MHz	

Note: VGA is a registered trademark of IBM Corporation.

Pin Arrangement



(Top view)

NCO: No Connection Open
(Leave open. These leads must not be connected.)

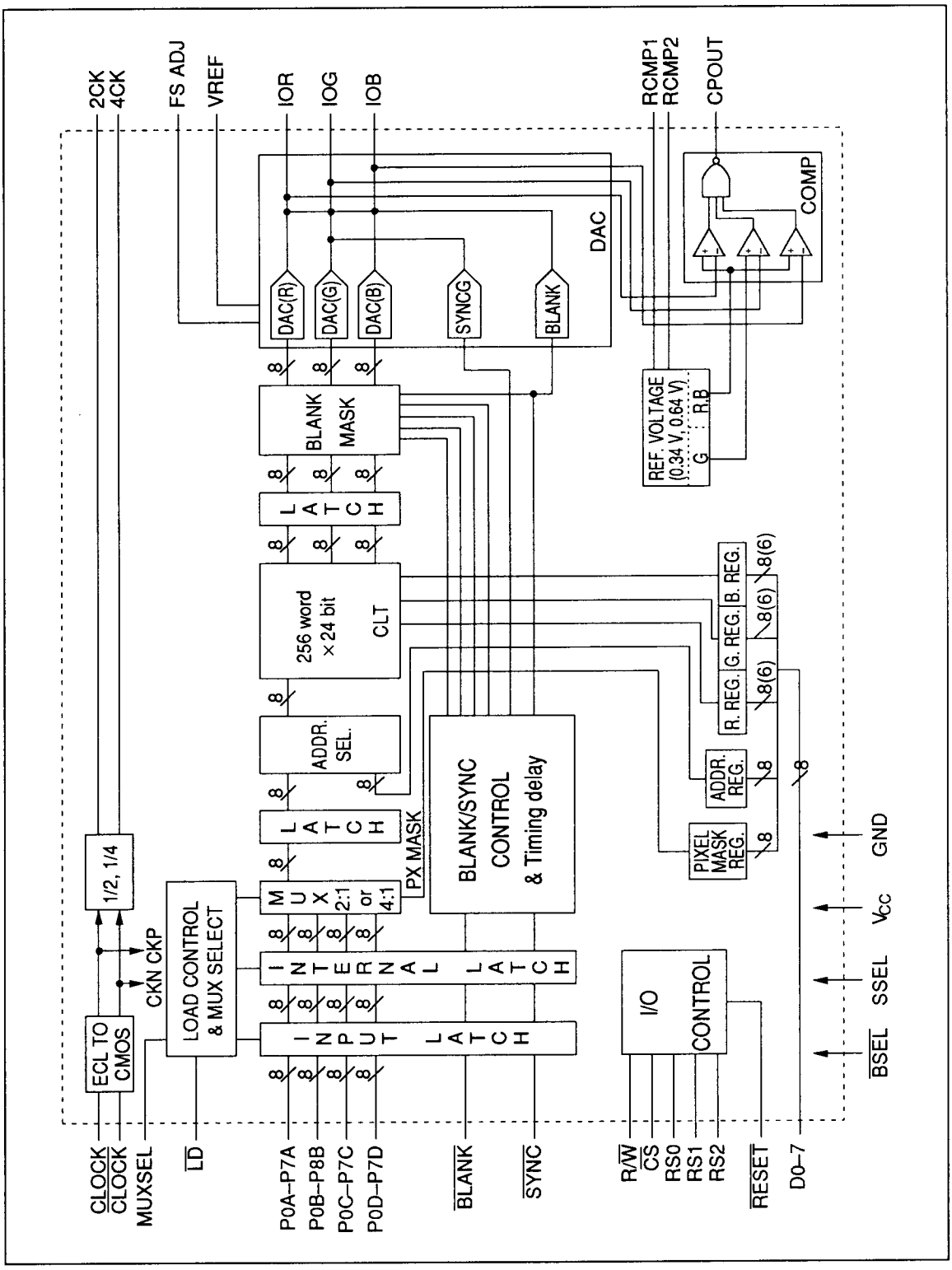
Pin Description

Pin No.	Symbol	Function
7 to 8, 10 to 15	D7 to D0	Data input/output lines for reading and writing the CLT and registers. D7 is the MSB; D0 is the LSB.
73 to80	P7A to P0A	Input lines for pixel data addressing the CLT. P7A is the MSB; P0A is the LSB.
82 to 89	P7B to P0B	Input lines for pixel data addressing the CLT. P7B is the MSB; P0B is the LSB.
91 to 98	P7C to P0C	Input lines for pixel data addressing the CLT. P7C is the MSB; P0C is the LSB.
107 to 114	P7D to P0D	Input lines for pixel data addressing the CLT. P7D is the MSB; P0D is the LSB.
24	$\overline{CS}$	Chip select line for reading and writing the CLT and registers.
22	R/$\overline{W}$	Mode select line for reading and writing the CLT and registers. R/$\overline{W}$ is valid when $\overline{CS}$ = 0, R/$\overline{W}$ = 1 selects read mode. R/$\overline{W}$ = 0 selects write mode.
29 to 27	RS2 to RS0	Register select lines for reading and writing the CLT and registers.
118	$\overline{LD}$	Strobe input line for pixel data and the $\overline{SYNC}$ and $\overline{BLANK}$ signals. The $\overline{LD}$ frequency should be 1/2 the clock frequency (2:1 multiplexing) or 1/4 the clock frequency (4:1 multiplexing).
126, 125	CLOCK, $\overline{CLOCK}$	Clock input lines. Two opposite-phase inputs are required. Operations from pixel data input to analog output are clocked by these inputs.
127	$\overline{BLANK}$	Forces the analog signals from the DACs to the blanking level.
128	$\overline{SYNC}$	$\overline{SYNC}$ signal input line. If SSEL = 1, when $\overline{SYNC}$ = 0 sync level is included in the green-channel DAC analog output. If the $\overline{SYNC}$ line is not used, leave it unconnected or pull it up to the 1 level.
20	$\overline{BSEL}$	Selects composite or non-composite blanking level for the DAC output. $\overline{BSEL}$ = 0 selects composite; $\overline{BSEL}$ = 1 selects non-composite.
21	SSEL	Selects composite or non-composite sync level for the DAC output. SSEL = 1 selects composite; SSEL = 0 selects non-composite.
48	IOR	Analog output line for the red-channel DAC.
46	IOG	Analog output line for the green-channel DAC.
44	IOB	Analog output line for the blue-channel DAC.
51	COMP	For connection of phase-compensating capacitors. Insert a 0.1-μF (ceramic) and 4.7-μF (electrolytic) capacitor between this lead and ground.
52	VREF	DAC reference level input line. See the sample connection diagram for external components.
53	FS ADJ	Connect a resistor (R_{SET}) for adjusting the DAC output level. Normally R_{SET} should be about 550 Ω.

Pin Description (cont)

Pin No.	Symbol	Function
55, 54	RCMP1, RCMP2	Lines for generating comparator reference voltages: RCMP1 is for the red and blue comparators; RCMP2 is for the green comparator. Normally, connect resistors of about 750 Ω.
56	CPOUT	Comparator result output line. Results of comparing the RGB output voltages with the reference voltages are output on this line as a digital signal.
120, 121	4CK, 2CK	Output lines for clock signals obtained by dividing the dot clock frequency by four (4CK) and two (2CK).
18	MUXSEL	Selects the input multiplex mode. MUXSEL = 1 selects 2:1. MUXSEL = 0 selects 4:1.
30	$\overline{\text{RESET}}$	Resets internal registers, flip-flops, etc. Reset is performed when $\overline{\text{RESET}}$ = 0.
9, 23, 25, 26, 41, 42, 50, 60, 61, 90, 115 to 117, 124, 129, 130	V_{CC}	Power supply voltage lines
16, 17, 19, 31, 39, 40, 43, 45, 47, 49, 62 to 65, 81, 99, 119, 131 to 133	GND	Ground lines
1 to 4, 32 to 38, 66 to 72, 100 to 106 134 to 136	(*)GND	Ground lines for heat dissipation

Block Diagram



Functional Description

MPU Access to CLT and Registers

The CLT (Color Lookup Table) and registers are accessed using the $\overline{CS}$, R/$\overline{W}$, RS2 to RS0, and D7 to D0 signals. RS2 to RS0 select the palette or register as indicated in table 1.

- Write to CLT: Figure 1 shows the timing for auto-increment writing data to the CLT. The write procedure is as follows:
  - Write address information in the address register.
  - Input data on D0 to D7 in the order of red, green, blue. All 24 bits (or 18 bits) are written together to the CLT after inputting of the blue data.
  - After the data are written, the address is automatically incremented by 1. Continue inputting data in the order of red, green, blue.
- Read from CLT: Figure 2 shows the timing for auto-increment reading data from the CLT. The read procedure is as follows:
  - Write address information in the address register.
  - Data are read from the specified address in the order of red, green, blue.
  - After the blue data have been read, the address is automatically incremented by 1, so the red, green, and blue data at the next address can be read.
- Register Write: To write data in registers, input the data on D0 to D7 as shown in figure 5.
- Register Read: Data are read from registers via D0 to D7. See the timing diagram in figure 6.

Pixel Data Input Control

- Pixel Data Input: Pixel data are input on lines P7 (A to D) to P0 (A to D). The data should be inputted at 1/4 or 1/2 the video output dot rate. The input data are multiplexed internally in A-to-D order (P7A-P0A, P7B-P0B, P7C-P0C, then P7D-P0D) and the CLT is accessed to obtain video output at the dot rate.

  In 2:1 multiplexing, only P7C to P0C and P7D to P0D are used.
- Pixel Mask Function: An on-chip pixel mask register enables arbitrary bits to be masked in the pixel data input on P7 (A to D) to P0 (A to D). Masked bits are held to 0. Table 2 lists the signal names of the pixel mask register. Table 3 indicates how bits are masked.
- Video Output Control Signals: The $\overline{BLANK}$, $\overline{SYNC}$, $\overline{BSEL}$, and SSEL input signals can be used to have either composite or non-composite sync and blanking levels supplied to the red, green, and blue video output lines. For details, see table 4.

Table 1 Address Mapping

RS2	RS1	RS0	Selected Palette or Register
0	0	0	Address register (write)
0	0	1	CLT (0 to 255)
0	1	0	Pixel mask register
0	1	1	Address register (read)
1	0	0	8-bit/6-bit control register
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

8-Bit and 6-Bit Modes

An on-chip register can be used to set the bit width of the red, green, and blue DA converters to eight or six bits. BC5 = 1 selects eight bits. BC5 = 0 selects six bits. (See table 2.)

Video Output and Connection Check Function

Red, green, and blue output comparators and reference current sources that generate reference levels for the comparators are integrated onto the chip. These can be used to have a test program implement software checks of interconnections to a graphics board, coaxial cables, and the CRT. The reference levels of the comparators can be adjusted by the resistances connected to the RCMP1 and RCMP2 lines. The reference level supplied to the comparators (Vcref) is related to the external resistance values (Rcmp1, Rcmp2) as follows:

Double Termination Mode

- Non-composite sync (red, green and bluechannels)

  Vcref (mV) = 0.458 (mA) × Rcmp1 (Ω)
  (Rcmp2)

- Composite sync

  Vcref (mV) = 0.458 (mA) × Rcmp1 (Ω)
  [red and blue channels]

  Vcref (mV) = 0.860 (mA) × Rcmp2 (Ω)
  [green channel]

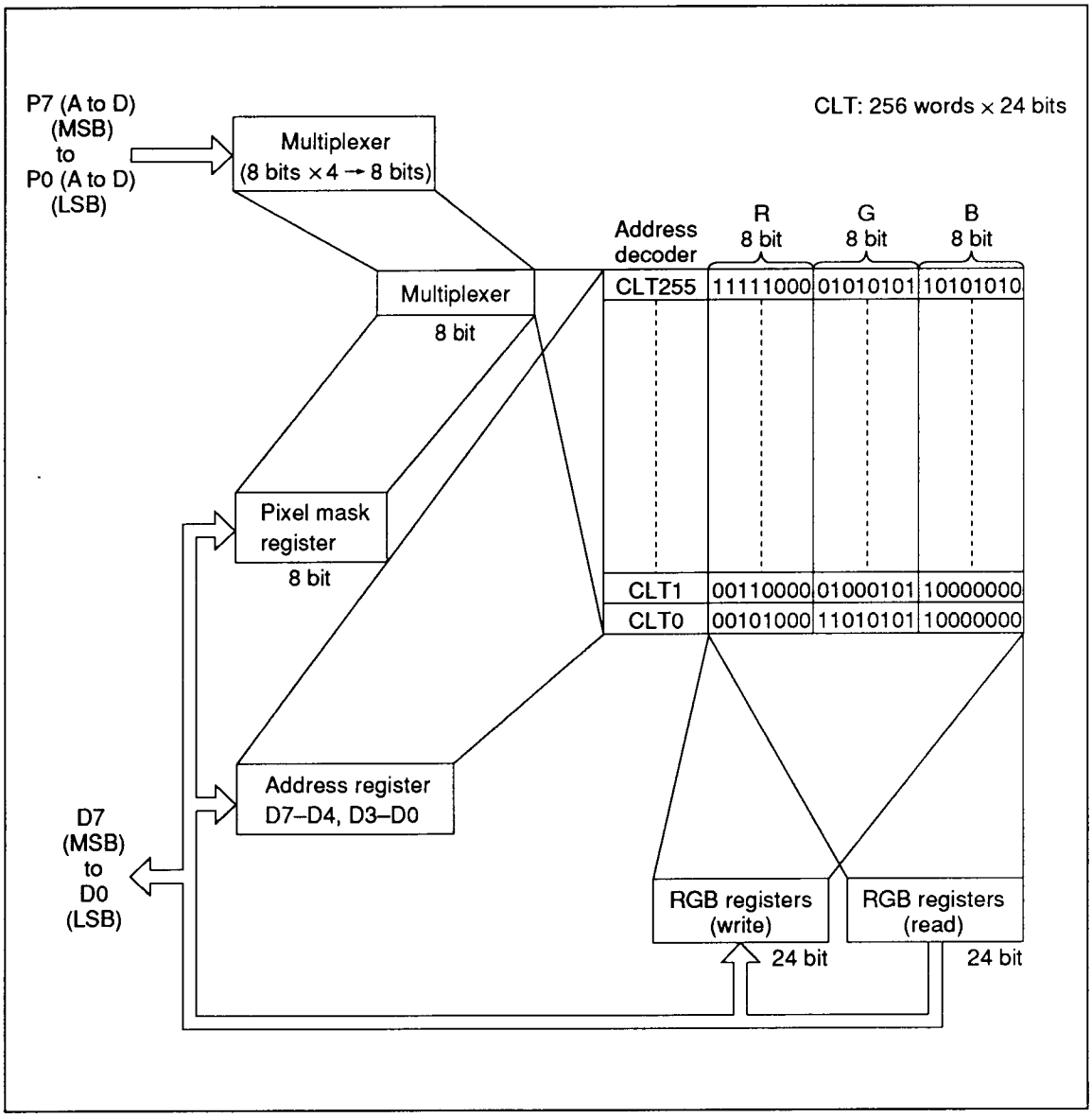
Table 2 Register Signal Names

	D7	D6	D5	D4	D3	D2	D1	D0
Pixel mask register	PM7	PM6	PM5	PM4	PM3	PM2	PM1	PM0
8-bit/6-bit register	—	—	BC5	—	—	—	—	—

Table 3 Pixel Mask Function

	Pixel Mask Function
PM7	Bit 7 masked when PM7 = 0
PM6	Bit 6 masked when PM6 = 0
PM5	Bit 5 masked when PM5 = 0
PM4	Bit 4 masked when PM4 = 0
PM3	Bit 3 masked when PM3 = 0
PM2	Bit 2 masked when PM2 = 0
PM1	Bit 1 masked when PM1 = 0
PM0	Bit 0 masked when PM0 = 0

Map of Registers and CLT



• **Write to CLT (Auto-increment)**

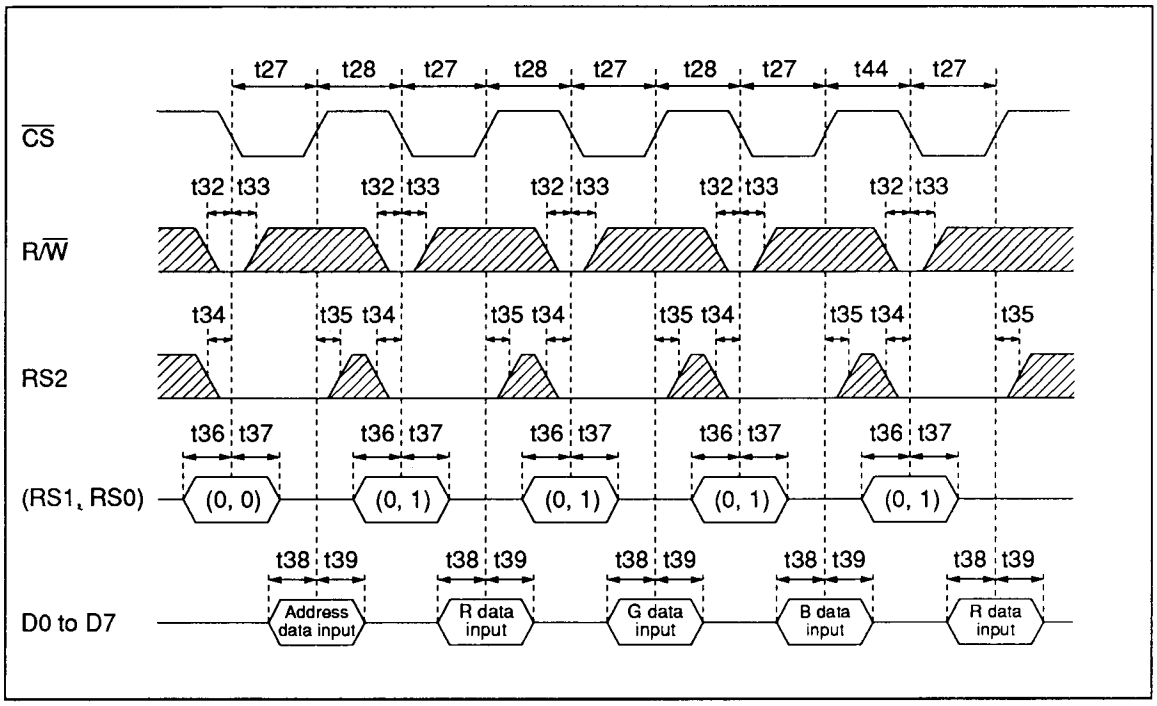
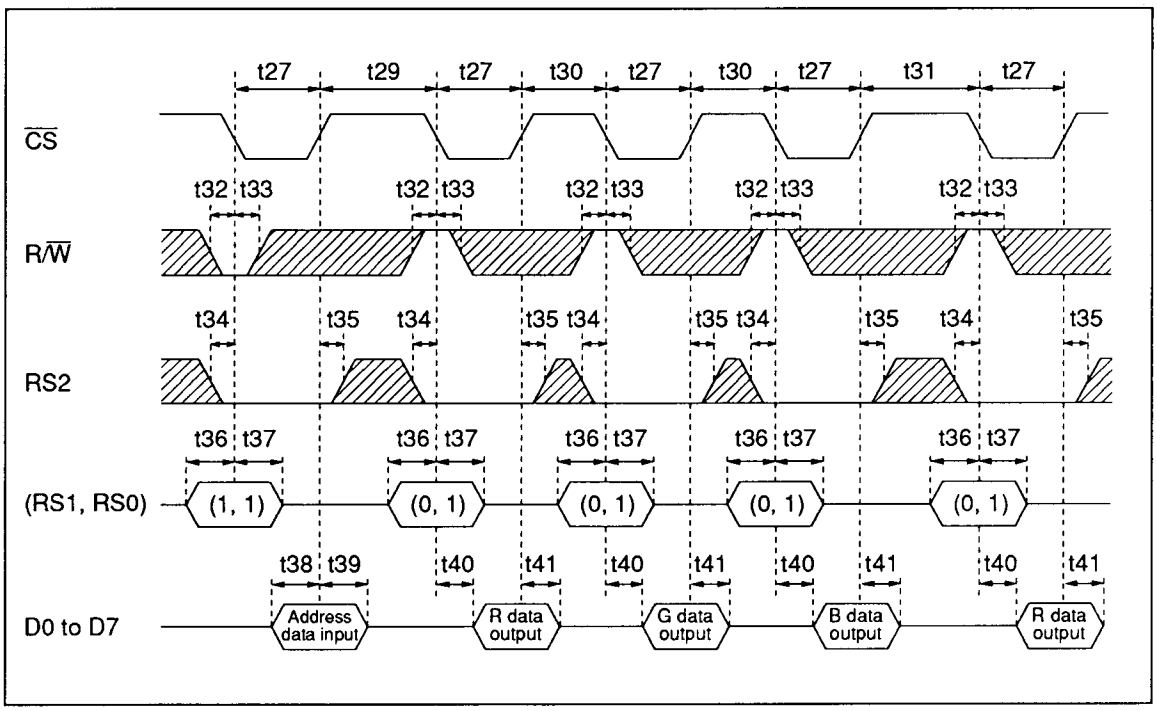


Figure 1

• **Read from CLT (Auto-increment)**



• **Read after Write**

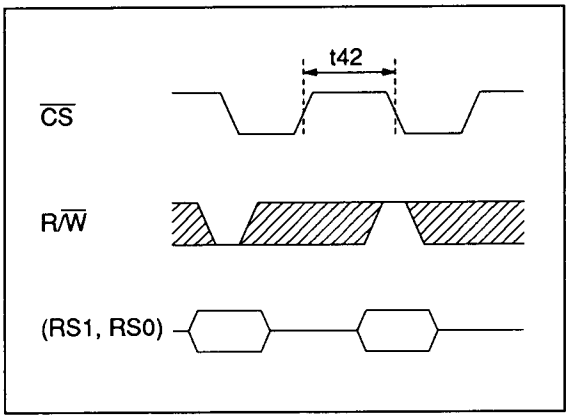


Figure 3

• **Write after Read**

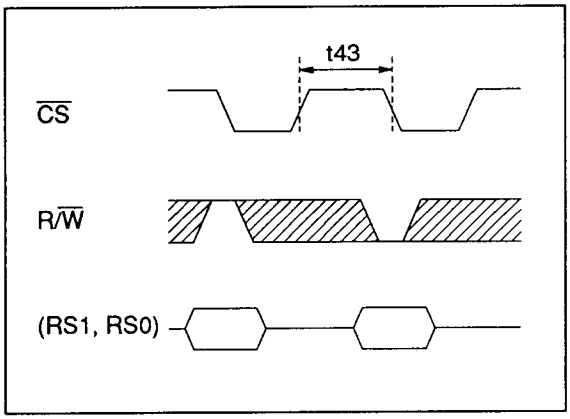


Figure 4

• **Write to CLT and Register**

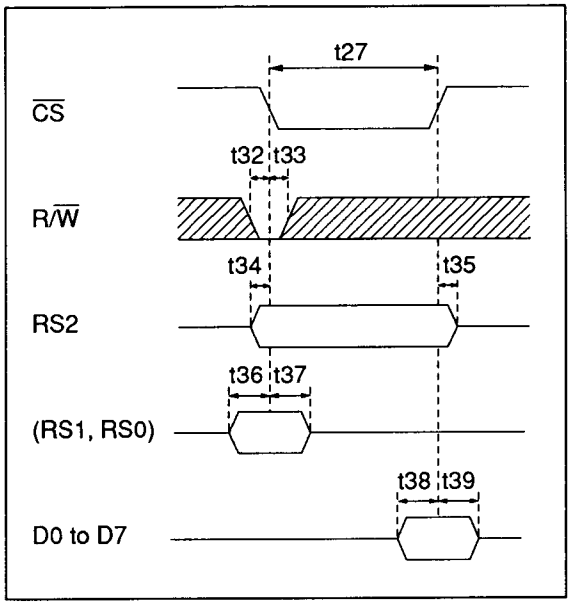


Figure 5

• **Read from CLT and Register**

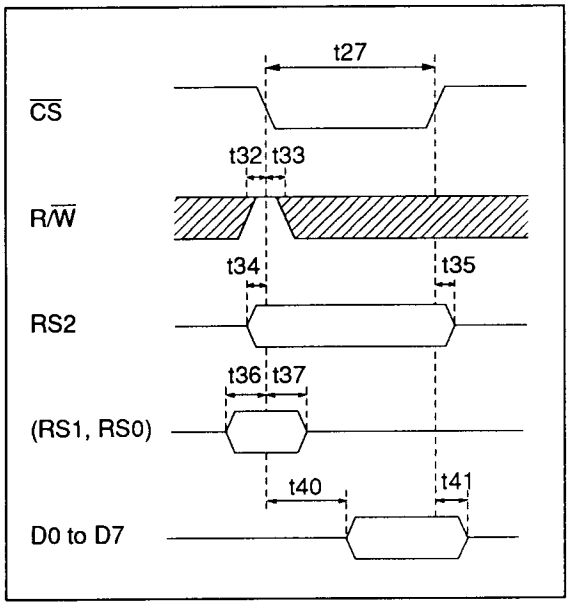


Figure 6

MPU Interface

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
$\overline{CS}$ signal low time	t27	50	—	—	ns	
$\overline{CS}$ signal high time (1)	t28	t1 × 4	—	—	ns	t1: clock cycle
$\overline{CS}$ signal high time (2)	t29	t1 × 7	—	—	ns	
$\overline{CS}$ signal high time (3)	t30	t1 × 4	—	—	ns	
$\overline{CS}$ signal high time (4)	t31	t1 × 7	—	—	ns	
$\overline{CS}$ signal high time (5)	t42	t1 × 7	—	—	ns	
$\overline{CS}$ signal high time (6)	t43	t1 × 7	—	—	ns	
$\overline{CS}$ signal high time (7)	t44	t1 × 7	—	—	ns	
R/$\overline{W}$ setup time to $\overline{CS}$	t32	10	—	—	ns	
R/$\overline{W}$ hold time to $\overline{CS}$	t33	10	—	—	ns	
RS2 setup time to $\overline{CS}$	t34	10	—	—	ns	Not tested
RS2 hold time to $\overline{CS}$	t35	10	—	—	ns	
RS0–RS1 setup time to $\overline{CS}$	t36	10	—	—	ns	
RS0–RS1 hold time to $\overline{CS}$	t37	10	—	—	ns	
D0–D7 setup time to $\overline{CS}$	t38	10	—	—	ns	
D0–D7 hold time to $\overline{CS}$	t39	10	—	—	ns	
Data output delay time	t40	5	—	40	ns	
Data output hold time	t41	5	—	—	ns	

Absolute Maximum Ratings (T_a = 25°C)

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}			7.0	V
TTL input voltage	V_{IT}	–0.5		5.5	V
ECL input voltage	V_{IE}	–0.5		5.5	V
Voltage across ECL input lines	DV_{IE}	0		2.0	V
Storage temperature	T_{str}	–55		150	°C
DAC output current	I_{OA}	0		–28.0	mA
Operating temperature Note	T_{opr}	0		70	°C

Note: Ambient temperature prior to operation of the HD153130.

Electrical Characteristics (T_a = 0 to +70°C, V_{CC} = 5 V ±5% unless otherwise specified)

DC Characteristics

Analog Output

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Resolution		8	8	8	Bit	R_L = 37.5 Ω
Integral linearity error	ILE	–1	—	1	LSB	V_{CC} = 5 V
Differential linearity error	DLE	–1	—	1	LSB	T_a = 25°C
Full-scale error		–5	—	5	%	
Output voltage		—	1	—	V	
Output matching characteristic		—	—	5	%	

Digital Input

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
TTL high input voltage	V_{IHT}	2.2	—	5.5	V	
TTL low input voltage	V_{ILT}	–0.3	—	0.7	V	
ECL high input voltage	V_{IHE}	4	—	5	V	
ECL low input voltage	V_{ILE}	0	—	3.4	V	
Voltage across ECL input lines	DV_{IE}	0.7	—	1.7	V	
TTL high input current (VI = 2.2 V)	I_{IHT}	–0.3	—	20	µA	V_{CC} = 5.25 V
TTL low input current (VI = 0.7 V)	I_{ILT}	–0.3	—	–20	µA	
ECL high input current (VI = 4.0 V)	I_{IHE}	–50	—	50	µA	
ECL low input current (VI = 3.4 V)	I_{ILE}	–50	—	50	µA	

Recommended Operating Conditions

Item	Symbol	Min	Typ	Max	Unit
Power supply voltage	V_{CC}	4.75	5.0	5.25	V
TTL high input voltage	V_{IHT}	2.4	—	V_{CC}	V
TTL low input voltage	V_{ILT}	0	—	0.5	V
ECL high input voltage	V_{IHE}	4.4	—	V_{CC}	V
ECL low input voltage	V_{ILE}	0	—	3.1	V
DAC output resistance	R_L	37.5	—	75	Ω
Reference voltage	V_{REF}	—	1.20	—	V
Reference resistance	V_{EXT}	—	542	—	Ω
Operating temperature	T_a	0	25	50	°C

AC Characteristics

Pixel Data

		HD153130F-110			HD153130F-135				
Item	Symbol	Min	Typ	Max	Min	Typ	Max	Unit	Test Conditions
Clock frequency	fmax	20	—	110	20	—	135	MHz	
Clock cycle time	t1	9.1	—	—	7.4	—	—	ns	
Clock high time	t2	3.6	—	—	3	—	—	ns	Not tested
Clock low time	t3	3.6	—	—	3	—	—	ns	Not tested
2CK frequency	f2max	10	—	55	10	—	67.5	MHz	
2CK cycle time	t4	18.2	—	—	14.8	—	—	ns	
2CK high time	t5	7.3	—	—	5.9	—	—	ns	Not tested
2CK low time	t6	7.3	—	—	5.9	—	—	ns	Not tested
2CK delay time	t7	—	7	—	—	7	—	ns	C_L = 15 pF
2CK duty		30	50	70	30	50	70	%	C_L = 15 pF, not tested
4Ck frequency	f4max	5	—	27.5	5	—	33.75	MHz	
4CK cycle time	t8	36.4	—	—	29.6	—	—	ns	
4CK high time	t9	14.5	—	—	11.8	—	—	ns	Not tested
4CK low time	t10	14.5	—	—	11.8	—	—	ns	Not tested
4CK delay time	t11	—	7	—	—	7	—	ns	C_L = 15 pF
4CK duty		30	50	70	30	50	70	%	C_L = 15 pF, not tested

• 2:1 multiplex

		HD153130F-110			HD153130F-135				
Item	Symbol	Min	Typ	Max	Min	Typ	Max	Unit	Test Conditions
$\overline{LD}$ cycle time	t13	18.2	—	—	14.8	—	—	ns	
$\overline{LD}$ high time	t14	5	—	—	5	—	—	ns	Not tested
$\overline{LD}$ low time	t15	5	—	—	5	—	—	ns	Not tested
Data setup time to $\overline{LD}$	t16	4	—	—	4	—	—	ns	TESTER SPEC: t16 = 5 ns
Data hold time from $\overline{LD}$	t17	3	—	—	3	—	—	ns	TESTER SPEC: t17 = 4 ns

• 4:1 multiplex

		HD153130F-110			HD153130F-135				
Item	Symbol	Min	Typ	Max	Min	Typ	Max	Unit	Test Conditions
$\overline{LD}$ cycle time	t18	36.4	—	—	29.6	—	—	ns	
$\overline{LD}$ high time	t19	10	—	—	10	—	—	ns	Not tested
$\overline{LD}$ low time	t20	10	—	—	10	—	—	ns	Not tested
Data setup time to $\overline{LD}$	t21	4	—	—	4	—	—	ns	TESTER SPEC: t21 = 5 ns
Data hold time from $\overline{LD}$	t22	3	—	—	3	—	—	ns	TESTER SPEC: t22 = 4 ns

• Analog output

		HD153130F-110			HD153130F-135				
Item	Symbol	Min	Typ	Max	Min	Typ	Max	Unit	Test Conditions
Analog output delay time	t23	—	20	—	—	20	—	ns	C_L = 15 pF
Settling time	t24	—	5	—	—	5	—	ns	±1 LSB/FSR, not tested
Analog output rise time	t25	—	1.5	—	—	1.5	—	ns	20% to 80%, not tested
Analog output fall time	t26	—	1.5	—	—	1.5	—	ns	80% to 20%, not tested
Analog output skew		—	0.5	—	—	0.5	—	ns	Not tested

Pixel Data Timing

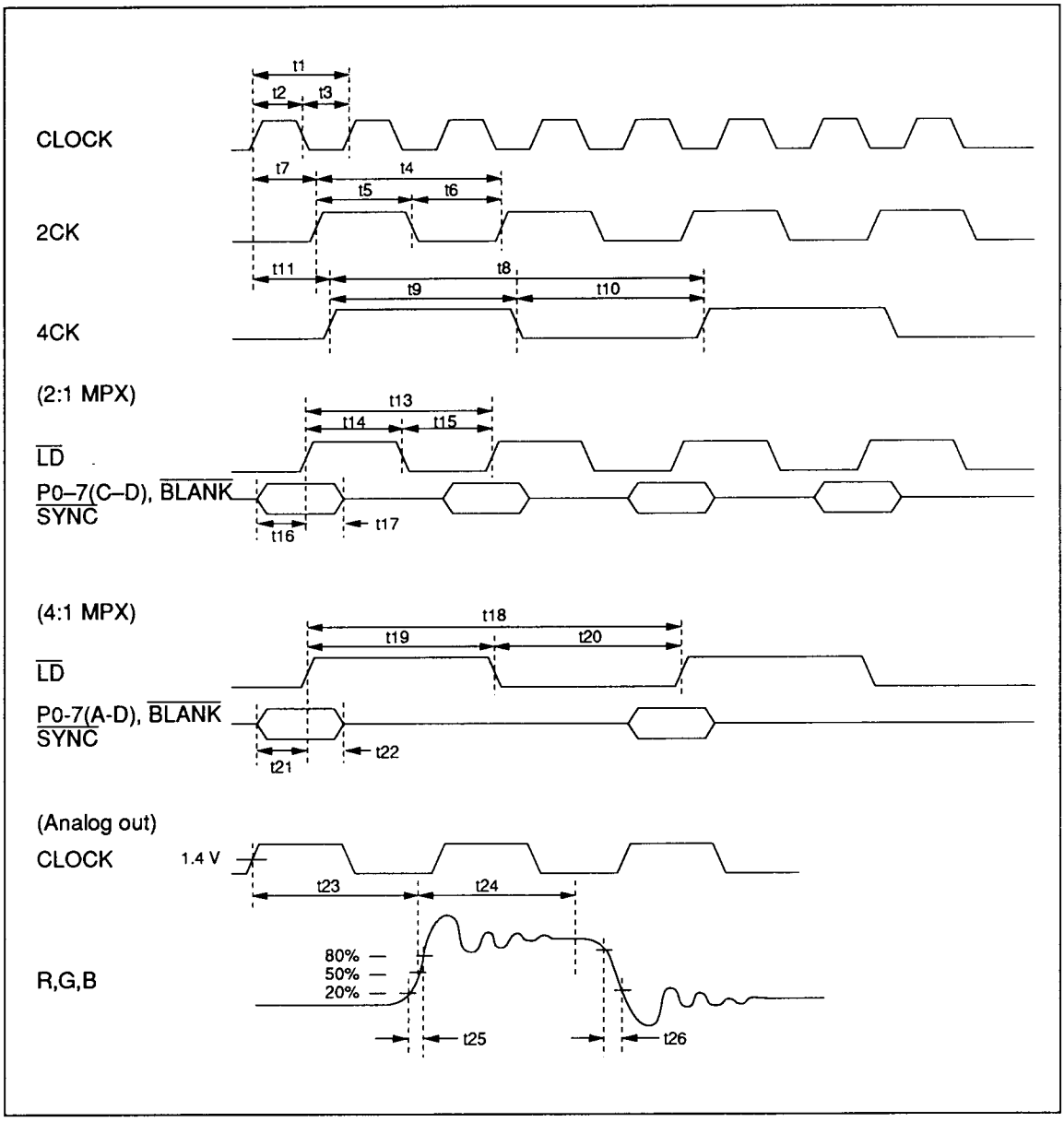


Table 4 Video Output Modes

$\overline{\text{BLANK}}$	$\overline{\text{SYNC}}$	$\overline{\text{BSEL}}$	SSEL	R	G	B
H	H	H	H	color (1)	color (3)	color (1)
H	H	H	L	color (1)	color (1)	color (1)
H	H	L	H	color (2)	color (4)	color (2)
H	H	L	L	color (2)	color (2)	color (2)
×	L	×	×	BOTTOM	BOTTOM	BOTTOM
L	H	H	H	BOTTOM	BLACK/BLANK (*)	BOTTOM
L	H	H	L	BOTTOM	BOTTOM	BOTTOM
L	H	L	H	BOTTOM	BLACK/BLANK (*)	BOTTOM
L	H	L	L	BOTTOM	BOTTOM	BOTTOM

Notes: ×: Don't care

color (1) Normal color level

color (2) Composite blanking level

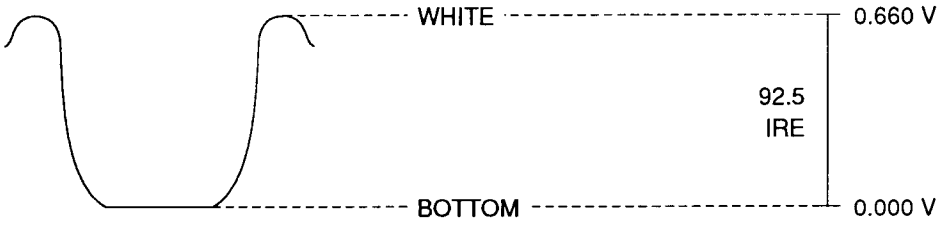
color (3) Composite sync level

color (4) Composite blanking and sync levels

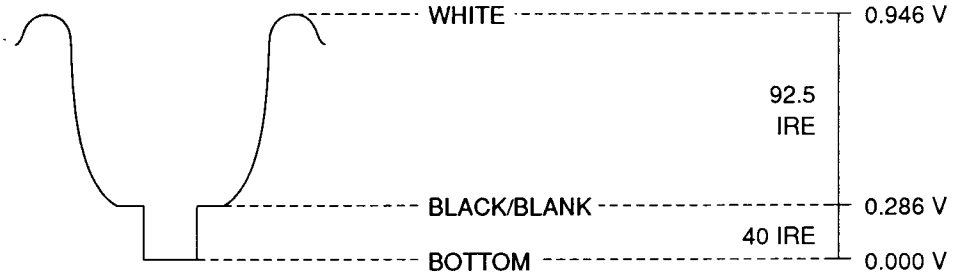
BLACK/BLANK (*) Composite sync level

Video Output Waveforms (1) (R_{SET} = 550 Ω)

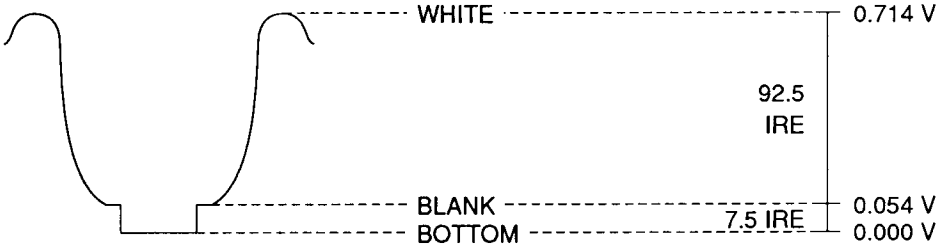
Non-composite sync and blanking (Red, Green, and Blue)



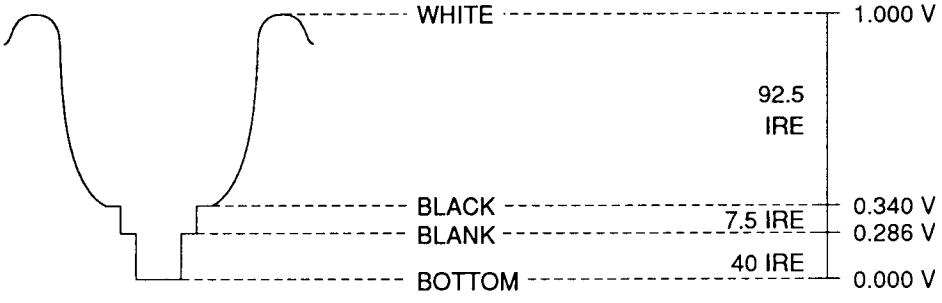
Composite sync, non-composite blanking (Green only)



Non-composite sync, composite blanking (Red, Green, and Blue)

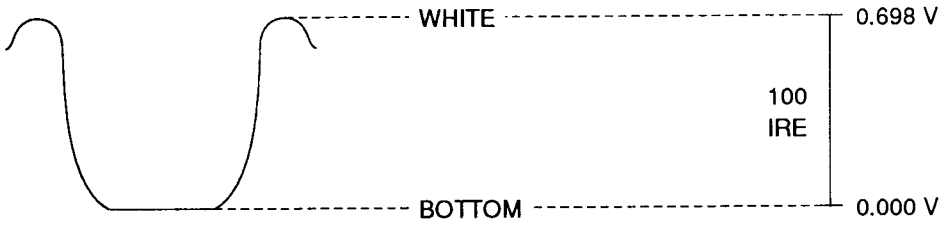


Composite sync and blanking (Green only)

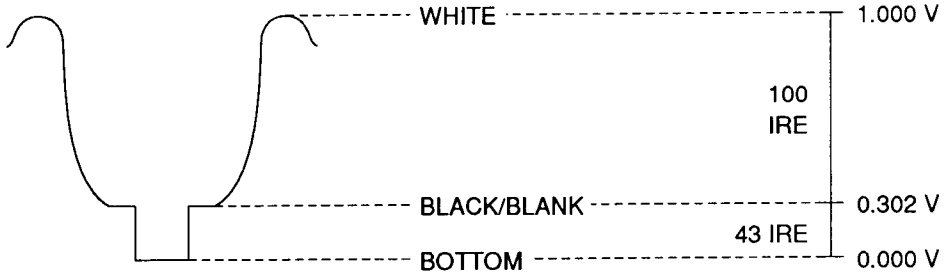


Video Output Waveforms (2) (R_{SET} = 529 Ω)

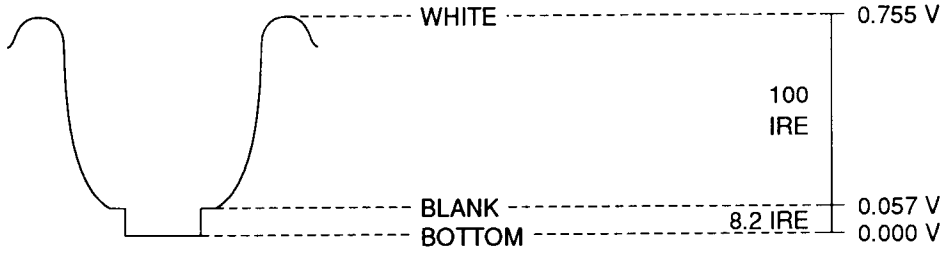
Non-composite sync and blanking (Red, Green, and Blue)



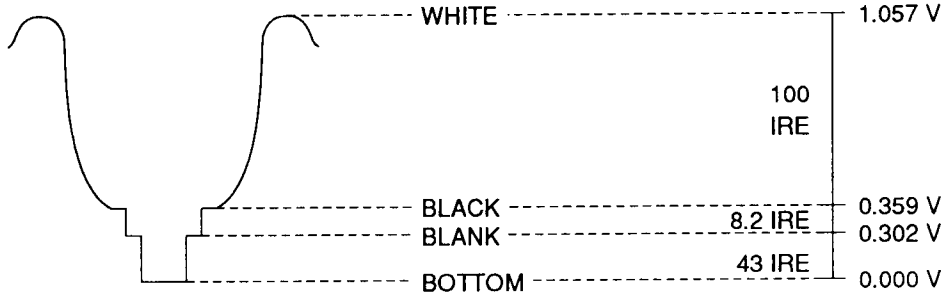
Composite sync, non-composite blanking (Green only)



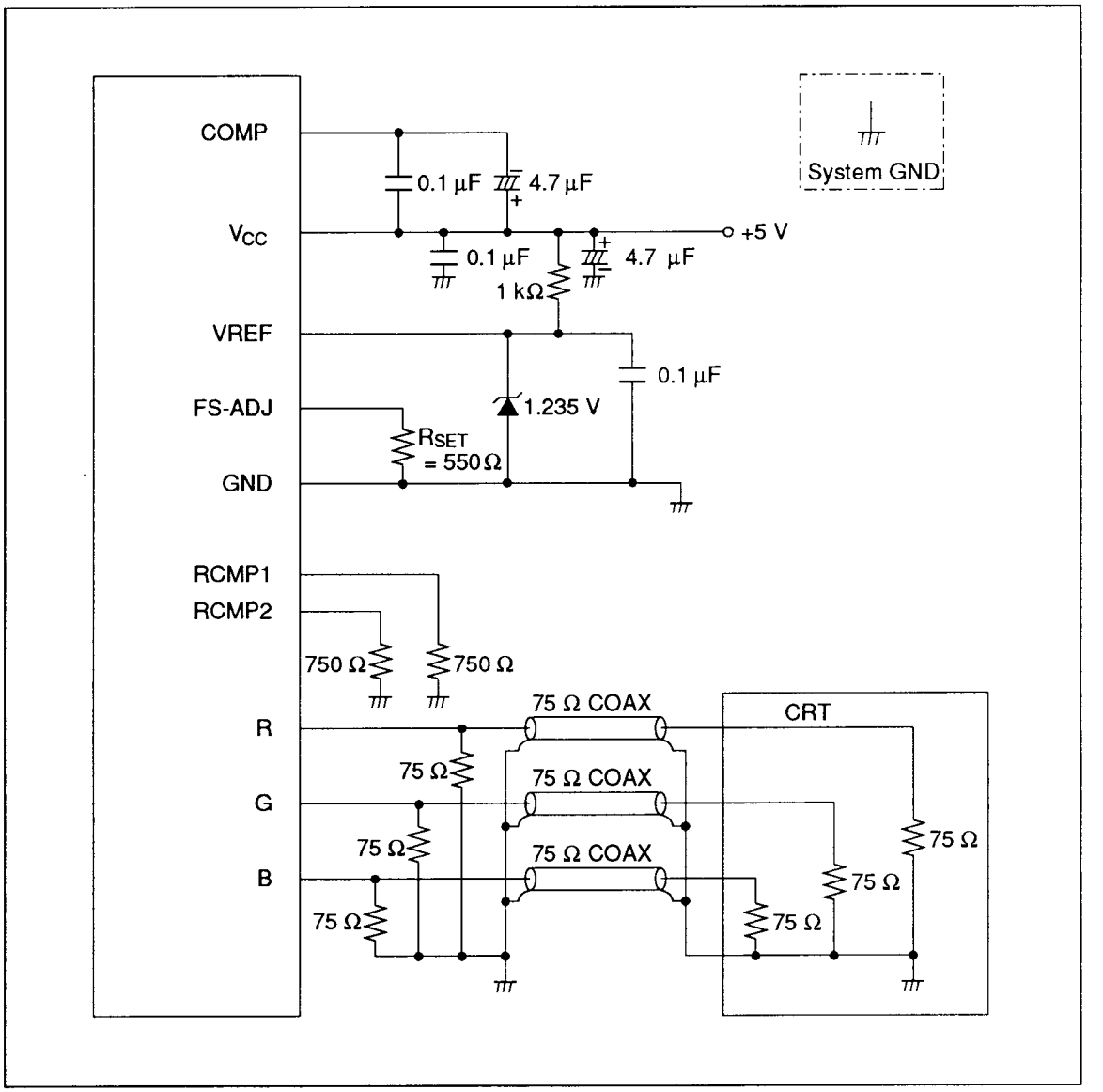
Non-composite sync, composite blanking (Red, Green, and Blue)



Composite sync and blanking (Green only)

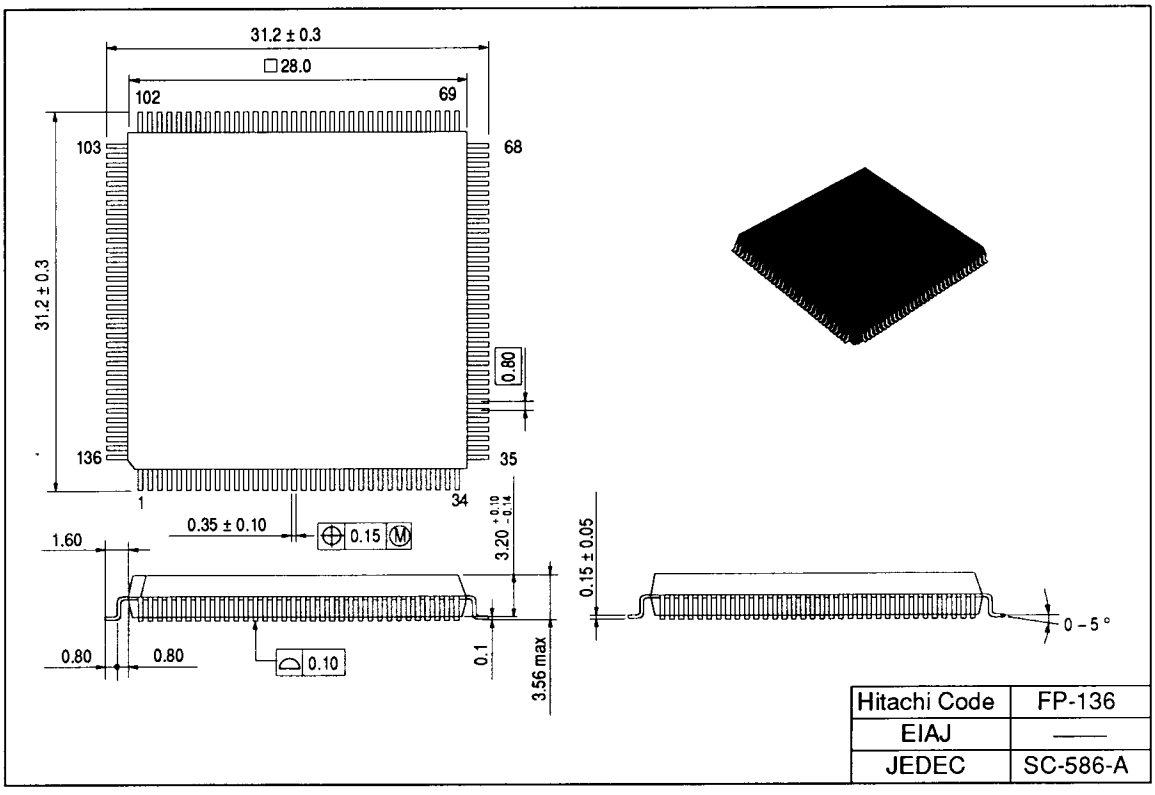


Sample Connection Diagram



Package Dimensions

Unit: mm



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