Triple 2-Input Exclusive OR/ Exclusive NOR Gate

MC10107

The MC10107 is a triple–2 input exclusive OR/NOR gate.

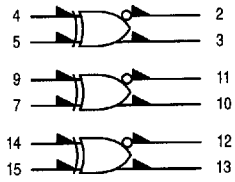
P_D = 40 mW typ/gate (No Load)
t_{pd} = 2.8 ns typ
t_r, t_f = 2.5 ns typ (20%–80%)

L SUFFIX
CERAMIC PACKAGE
CASE 620–10

P SUFFIX
PLASTIC PACKAGE
CASE 648–08

FN SUFFIX
PLCC
CASE 775–02

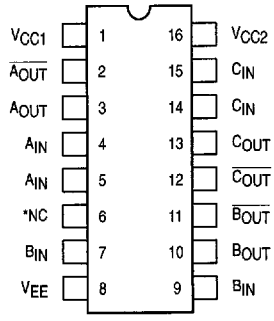
LOGIC DIAGRAM



$3 = (4 \bullet \overline{5}) + (\overline{4} \bullet 5)$
$2 = (\overline{4} \bullet \overline{5}) + (4 \bullet 5)$

V_{CC1} = PIN 1
V_{CC2} = PIN 16
V_{EE} = PIN 8

DIP
PIN ASSIGNMENT



***NC = No Connection**

Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 6–11.

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ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	Test Limits							Unit
			−30°C		+25°C			+85°C		
			Min	Max	Min	Typ	Max	Min	Max	
Power Supply Drain Current	I_E	8		31			28		31	mAdc
Input Current	I_{inH}	4, 9, 14 5, 7, 15		425 350			265 220		265 220	µAdc
	I_{inL}	*	0.5		0.5			0.3		µAdc
Output Voltage Logic 1	V_{OH}	2 2 3 3	−1.060 −1.060 −1.060 −1.060	−0.890 −0.890 −0.890 −0.890	−0.960 −0.960 −0.960 −0.960		−0.810 −0.810 −0.810 −0.810	−0.890 −0.890 −0.890 −0.890	−0.700 −0.700 −0.700 −0.700	Vdc
Output Voltage Logic 0	V_{OL}	2 2 3 3	−1.890 −1.890 −1.890 −1.890	−1.675 −1.675 −1.675 −1.675	−1.850 −1.850 −1.850 −1.850		−1.650 −1.650 −1.650 −1.650	−1.825 −1.825 −1.825 −1.825	−1.615 −1.615 −1.615 −1.615	Vdc
Threshold Voltage Logic 1	V_{OHA}	2 2 3 3	−1.080 −1.080 −1.080 −1.080		−0.980 −0.980 −0.980 −0.980			−0.910 −0.910 −0.910 −0.910		Vdc
Threshold Voltage Logic 0	V_{OLA}	2 2 3 3		−1.655 −1.655 −1.655 −1.655			−1.630 −1.630 −1.630 −1.630		−1.595 −1.595 −1.595 −1.595	Vdc
Switching Times (50Ω Load)					Min	Typ	Max			ns
Propagation Delay	t++	Inputs	−1.1	3.8	1.1	2.0	3.7	1.1	4.0	
	t+−	4,9 or 14	1.1	3.8	1.1	2.0	3.7	1.1	4.0	
	t−+	to either	1.1	3.8	1.1	2.0	3.7	1.1	4.0	
	t−−	Output	1.1	3.8	1.1	2.0	3.7	1.1	4.0	
	t++	Inputs	1.1	3.8	1.1	2.8	3.7	1.1	4.0	
	t+−	5,7 or 15	1.1	3.8	1.1	2.8	3.7	1.1	4.0	
	t−+	to either	1.1	3.8	1.1	2.8	3.7	1.1	4.0	
	t−−	Output	1.1	3.8	1.1	2.8	3.7	1.1	4.0	
Rise Time (20 to 80%)	t+	**	1.1	3.5	1.1	2.5	3.5	1.1	3.8	
Fall Time (20 to 80%)	t−	**	1.1	3.5	1.1	2.5	3.5	1.1	3.8	

* Individually test each input applying V_{IH} or V_{IL} to input under test.
** Any Output.

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ELECTRICAL CHARACTERISTICS (continued)

@ Test Temperature	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
–30°C	–0.890	–1.890	–1.205	–1.500	–5.2
+25°C	–0.810	–1.850	–1.105	–1.475	–5.2
+85°C	–0.700	–1.825	–1.035	–1.440	–5.2

TEST VOLTAGE VALUES (Volts)

Characteristic		Symbol	Pin Under Test	TEST VOLTAGE APPLIED TO PINS LISTED BELOW V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current		I_E	8	5, 7, 15				8	1, 16
Input Current		I_{inH}	4, 9, 14	*				8	1, 16
			5, 7, 15	*				8	1, 16
		I_{inL}	*		*			8	1, 16
Output Voltage	Logic 1	V_{OH}	2	4, 5				8	1, 16
			2					8	1, 16
			3	4				8	1, 16
			3	5				8	1, 16
Output Voltage	Logic 0	V_{OL}	2	4				8	1, 16
			2	5				8	1, 16
			3	4, 5				8	1, 16
			3					8	1, 16
Threshold Voltage	Logic 1	V_{OHA}	2	5		4		8	1, 16
			2				4	8	1, 16
			3			4		8	1, 16
			3			5		8	1, 16
Threshold Voltage	Logic 0	V_{OLA}	2			4		8	1, 16
			2			5		8	1, 16
			3	5		4		8	1, 16
			3				4	8	1, 16
Switching Times	(50Ω Load)			+1.1V		Pulse In	Pulse Out	–3.2 V	+2.0 V
Propagation Delay		t++	Inputs	5, 7, 15		Input 4, 9 or 14	Corresponding XOR/XNOR Outputs	8	1, 16
		t+ –	4,9 or 14	5, 7, 15				8	1, 16
		t–+	to either	5, 7, 15				8	1, 16
		t– –	Output	5, 7, 15				8	1, 16
		t++	Inputs	4, 9, 14		Input 5, 7 or 15	Corresponding XOR/XNOR Outputs	8	1, 16
		t+ –	5,7 or 15	4, 9, 14				8	1, 16
		t–+	to either	4, 9, 14				8	1, 16
		t– –	Output	4, 9, 14				8	1, 16
Rise Time	(20 to 80%)	t+	**	4, 9, 14		Any Input	Corresponding XOR/XNOR Outputs	8	1, 16
Fall Time	(20 to 80%)	t–	**	4, 9, 14		Any Input		8	1, 16

* Individually test each input applying V_{IH} or V_{IL} to input under test.

** Any Output.

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to –2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.