

54LS/74LS384

010021

8-BIT SERIAL/PARALLEL TWO'S COMPLEMENT MULTIPLIER

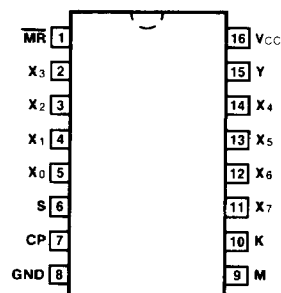
DESCRIPTION — The '384 is an 8-bit by 1-bit sequential logic element that multiplies two numbers represented in two's complement notation. The device implements Booth's algorithm internally to produce a two's complement product that needs no subsequent correction. Parallel inputs accept and store an 8-bit multiplicand ($X_0 - X_7$). The multiplier word is applied to the Y input in a serial bit stream, least significant bit first. The product is clocked out at the S output, least significant bit first.

The K input is used for expansion to longer X words, using two or more '384 packages. The Mode Control (M) input is used to establish the most significant package. An asynchronous Master Reset (\overline{MR}) input clears the internal flip-flops to the start condition and enables the X latches to accept new multiplicand data.

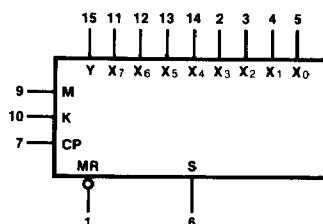
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		$V_{CC} = +5.0 V \pm 5\%$, $T_A = 0^\circ C \text{ to } +70^\circ C$	$V_{CC} = +5.0 V \pm 10\%$, $T_A = -55^\circ C \text{ to } +125^\circ C$	
Plastic DIP (P)	A	74LS384PC		9B
Ceramic DIP (D)	A	74LS384DC	54LS384DM	6B
Flatpak (F)	A	74LS384FC	54LS384FM	4L

CONNECTION DIAGRAM PINOUT A



LOGIC SYMBOL

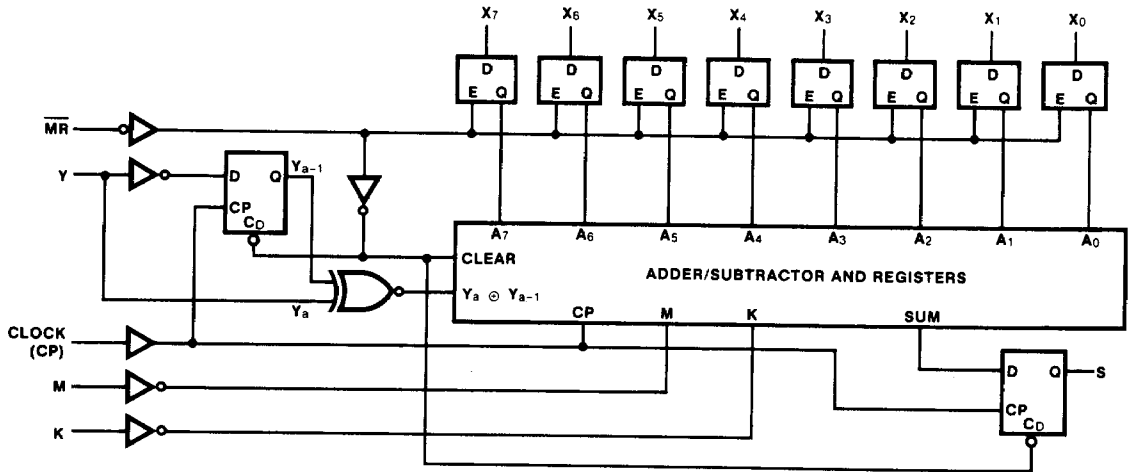


$V_{CC} = \text{Pin } 16$
 $GND = \text{Pin } 8$

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74LS (U.L.) HIGH/LOW
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0
K	Serial Expansion Input	0.75/0.75
M	Mode Control Input	0.5/0.3
\overline{MR}	Asynchronous Master Reset Input (Active LOW)	0.75/0.75
$X_0 - X_7$	Multiplicand Data Inputs	0.5/0.3
Y	Serial Multiplier Input	2.0/2.0
S	Serial Product Output	25/7.5 (5.0)

LOGIC DIAGRAM



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FUNCTION TABLE

INPUTS						INTERNAL	OUTPUT	FUNCTION
MR	CP	K	M	X _i	Y	Y _{a-1}	S	
-		L	L					Most Significant Multiplier Device
-		CS	H					Devices Cascaded in Multiplier String
L				OP		L	L	Load New Multiplicand and Clear Internal Sum and Carry Registers
H								Device Enabled
H	┐				L	L	AR	Shift Sum Register
H	┐				L	H	AR	Add Multiplicand to Sum Register and Shift
H	┐				H	L	AR	Subtract Multiplicand from Sum Register and Shift
H	┐				H	H	AR	Shift Sum Register

┐ = LOW-to-HIGH transition
 CS = Connected to S output of high order device
 OP = X_i latches open for new data (i = 0, 7)
 AR = Output as required per Booth's algorithm