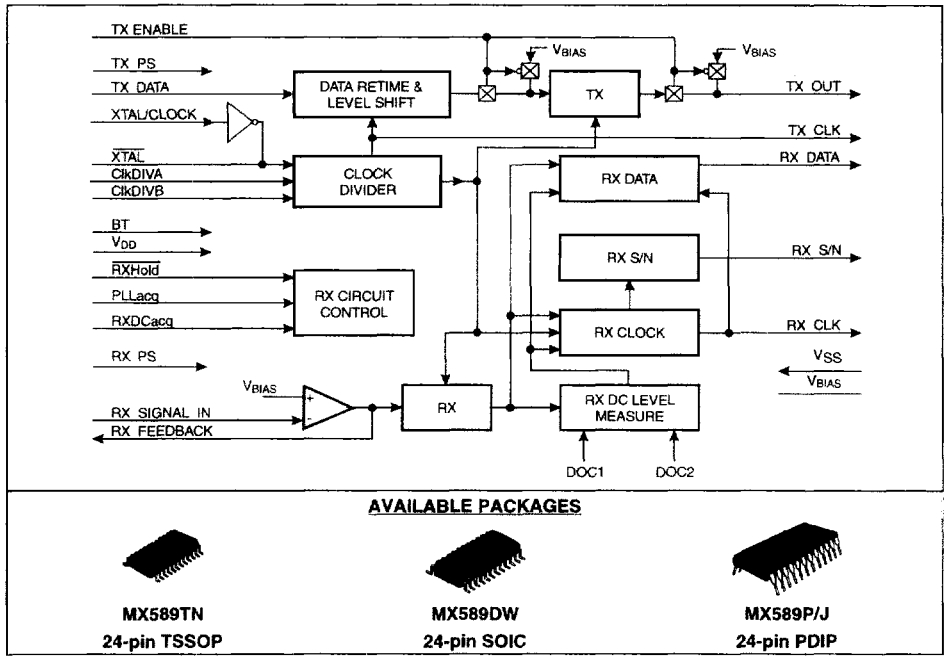
# MX•COM, INC. MiXed Signal ICs

DATA BULLETIN

# MX589 High Speed GMSK Modem

- **Data Rates from 4kbps to 64kbps**
- **Full or Half Duplex Gaussian Minimum Shift Keying (GMSK) Operation**
- **Selectable BT: (0.3 or 0.5)**
- **Low Power:**
  **3.0V, 32kbps, 1.5mA typ.**
  **5.0V, 64kbps, 4.0mA typ.**
- **Low Cost**
- **Point of Sale Terminals**
- **Low Power Wireless Data Link for PCs, Laptops, and Printers**
- **Data for GPS/Differential GPS**
- **Portable Wireless Data Applications:**
  **Cellular Digital Packet Data (CDPD)**
  **Mobitex™ Mobile Data System**
- **Low Current Non-DSP Solution**




**AVAILABLE PACKAGES**



**MX589TN**
**24-pin TSSOP**



**MX589DW**
**24-pin SOIC**



**MX589P/J**
**24-pin PDIP**

The MX589 is a single-chip synchronous modem designed for wireless data applications. Employing Gaussian Minimum Shift Keying (GMSK) baseband modulation, the MX589 features a wide range of available data rates: 4kbps to 64kbps.

Data rates and choice of BT (0.3 or 0.5) are pin-programmable to provide for different system requirements.

The Tx and Rx digital data interfaces are bit serial, synchronized to Tx and Rx data clocks generated by the modem. Separate Tx and Rx Powersave inputs allow full or half-duplex operation. Rx input levels can be set by a suitable AC and DC level adjusting circuit built with external components around an on-chip Rx Input Amplifier.

Acquisition, lock and hold of Rx data signals are made easier and faster by the use of Rx Control Inputs to clamp, detect and/or hold input data levels and can be set by the µProcessor as required. The Rx S/N output provides an indication of the quality of the received signal.

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Doc. # 20480103.009

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# 1. Block Diagram

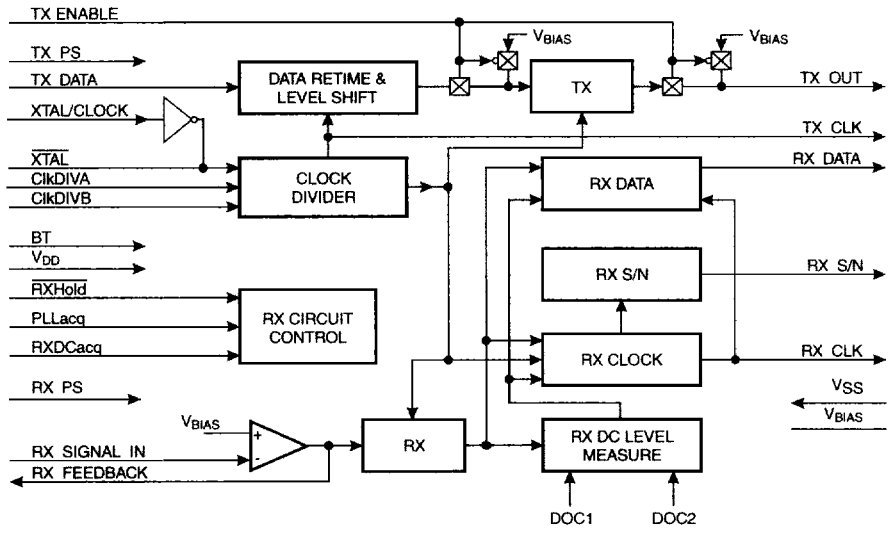


**Figure 1: Device Block Diagram**

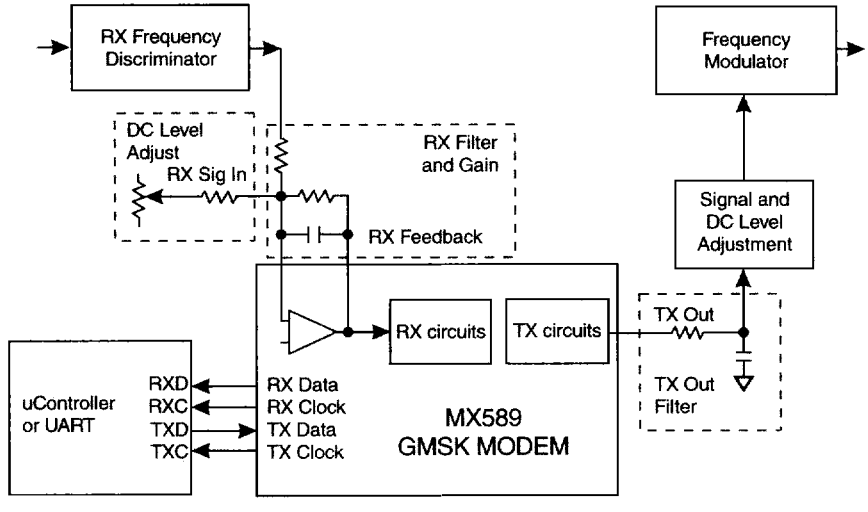


**Figure 2: System Block Diagram**


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## 2. Signal List

| Pin No. | Name | Type | Description |
|---|---|---|---|
| 1 | $\overline{\text{XTAL}}$ | | The output of the on-chip clock oscillator. |
| 2 | Xtal/Clock | | The input to the on-chip Xtal oscillator. A Xtal, or externally derived clock ($f_{XTAL}$) pulse input should be connected here. If an externally generated clock is to be used, it should be connected to this pin and the $\overline{\text{XTAL}}$ pin left unconnected |
| 3 | ClkDivA | | Logic level inputs control the internal clock divider and therefore the transmit and receive data rate. See Table 1 |
| 4 | ClkDivB | | Logic level inputs control the internal clock divider and therefore the transmit and receive data rate. See Table 1 |
| 5 | $\overline{\text{Rx HOLD}}$ | | A logic 0 applied to this input will freeze the Clock Extraction and Level Measurement circuits unless they are in Acquire mode. |
| 6 | RxDCacq | | A logic 1 applied to this input will set the RX Level Measurement circuitry to the Acquire mode. |
| 7 | PLLacq | | A logic 1 applied to this input will set the Rx Clock Extraction circuitry to Acquire mode (see Table 2). |
| 8 | Rx PSAVE | | A logic 1 applied to this input will powersave all receive circuits except for Rx CLK output (which will continue at the set bit-rate) and cause the Rx Data and Rx S/N outputs to go to a logic 0. |
| 9 | $V_{BIAS}$ | | The internal circuitry bias line, held at $V_{DD}/2$, this pin must be bypassed to $V_{SS}$ by a capacitor mounted close to the pin. |
| 10 | Rx FB | | Output of the Rx Input Amplifier. |
| 11 | Rx Signal In | | Input to Rx Input Amplifier. |
| 12 | $V_{SS}$ | | Negative supply. Signal ground. |
| 13 | Doc1 | | Connections to the Rx Level Measurement Circuitry. A capacitor should be connected from each pin to $V_{SS}$. See Figure 3. |
| 14 | Doc2 | | Connections to the Rx Level Measurement Circuitry. A capacitor should be connected from each pin to $V_{SS}$. See Figure 3. |
| 15 | BT | | A logic level to select the modem BT (the ratio of the Tx Filter's -3dB frequency to the Bit-Rate). A logic 1 = BT of 0.5, a logic 0 = BT of 0.3. |
| 16 | Tx Out | | Tx signal output from the MX589 GMSK Modem. |
| 17 | Tx Enable | | A logic 1 applied to this input enables the transmit data path through the Tx Filter to the Tx Out pin. A logic 0 will place the Tx Out pin at $V_{BIAS}$ via a high impedance. |
| 18 | Tx PSAVE | | A logic 1 applied to this input will powersave all transmit circuits except for the Tx Clock. |
| 19 | Tx Data | | The logic level input for the data to be transmitted. This data should be synchronous with Tx CLK. |
| 20 | Rx Data | | A logic level output carrying the received data, synchronous with Rx CLK. |
| 21 | Rx CLK | | A logic level clock output at the received data bit-rate. |
| 22 | Tx CLK | | A logic level clock output at the transmit-data rate. |
| 23 | Rx S/N | | A logic level output which may be used as an indication of the quality of the received signal. |
| 24 | $V_{DD}$ | | Positive supply. A single 5.0V power supply is required. Levels and voltages within this modem are dependent upon this supply. This pin should be bypassed to $V_{SS}$ by a capacitor mounted close to the pin. |


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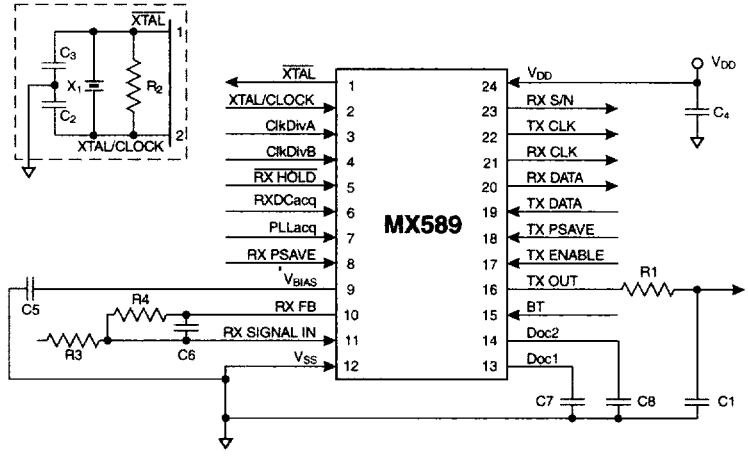
## 3. External Components




| | | |
|---|---|---|
| R1 | Note 1 | ±5% |
| R2 | 1.0MΩ | ±10% |
| R3 | Note 2 | ±10% |
| R4 | 100kΩ | ±10% |
| C1 | Note 1 | ±10% |
| C2 | Note 3 | |
| C3 | Note 3 | |

| | | |
|---|---|---|
| C4 | 0.1µF | ±20% |
| C5 | 1.0µF | ±20% |
| C6 | 22.0pF | ±20% |
| C7 | Note 4 | |
| C8 | Note 4 | |
| | | |
| X1 | Note 5 | |

**Figure 3: Recommended External Components**

**External Components Notes:**

1. The RC network formed by R1 and C1 is required between the Tx Out pin and the input to the modulator. This network, which can form part of any DC level shifting and gain adjustment circuitry, forms an important part of the transmit signal filtering. The ground connection to the capacitor C1 should be positioned to give maximum attenuation of high-frequency noise into the modulator.

   The component values should be chosen so that the product of the resistance and the capacitance is:

   BT of 0.3 = 0.34/bit rate (bps) BT of 0.5 = 0.22/bit rate (bps)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| Data Rate bps | BT = 0.3 | | BT = 0.5 | |
|---|---|---|---|---|
| | R1 | C1 | R1 | C1 |
| 4000 | 120kΩ | 680pF | 120kΩ | 470pF |
| 4800 | 100kΩ | 680pF | 100kΩ | 470pF |
| 8000 | 91kΩ | 470pF | 120kΩ | 220pF |
| 9600 | 91kΩ | 390pF | 47kΩ | 470pF |
| 16000 | 47kΩ | 470pF | 91kΩ | 150pF |
| 19200 | 100kΩ | 180pF | 91kΩ | 120pF |
| 32000 | 47kΩ | 220pF | 47kΩ | 150pF |
| 38400 * | 47kΩ | 180pF | 47kΩ | 120pF |
| 64000 * | 56kΩ | 100pF | 51kΩ | 68pF |
| * $V_{DD} \geq 4.5V$ | | | | |

**Note**: In all cases the value of R1 should not be less than 20.0 kΩ, and the calculated value of C1 includes calculated parasitic capacitance.

2. R3, R4 and C6 form the gain components for the Rx Input signal. R3 should be chosen as required by the signal input level.
3. The values chosen for C2 and C3 (including stray capacitance), should be suitable for the applied $V_{DD}$ and the frequency of X1.

   As a guide : C2 = C3 = 33pF at 1.0MHz falling to 18pF at the maximum frequency.

   At 3.0 volts, C2 = C3 = 33pF falling to 18pF at 5.0MHz. The equivalent series resistance of X1 should be less that 2.0kΩ falling to 150Ω at the maximum frequency. Stray capacitance on the Xtal/Clock circuit pins must be minimized.
4. C7 and C8 should both be .015µF for a data rate of 8kbps, and inversely proportional to the data rate for other data rates, e.g. .030µF at 4kbps, .0018µF at 64kbps.
5. The MX589 can operate correctly with Xtal/Clock frequencies between 1.0MHz and 8.2MHz ($V_{DD}$ = 5.0V) and 1.0MHz to 5.0MHz ($V_{DD}$ = 3.0V) see Table 1 for examples. For best results, a crystal oscillator design should drive the clock inverter input with signal levels of at least 40% of $V_{DD}$, peak to peak. Tuning fork crystals generally cannot meet this requirement. To obtain crystal oscillator design assistance, consult your crystal manufacturer. Operation of this device without a Xtal or Clock input may cause device damage.

# 4. General Description

## 4.1 Clock Oscillator Divider

The Tx and (nominal) Rx data rates are determined by division of the frequency present at the $\overline{Xtal}$ pin, which may be generated by the on-chip Xtal oscillator or derived from an external source. Any Xtal/clock frequency in the range 1.0MHz to 5.0MHz for $V_{DD}$ = 3.0V, or 1.0 MHz to 8.2MHz for $V_{DD}$ = 5.0V may be used, depending on the desired data rate.

The division ratio is controlled by the logic level inputs on ClkDivA and ClkDivB pins, as shown in Table 1, together with an indication of how various standard data rates may be derived from common µP Xtal frequencies.

$$\text{Data Rate} = \frac{\text{Xtal/Clock Frequency}}{\text{Division Ratio (Clk Div A/B)}}$$


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| Inputs | | Division Ratio | Xtal/Clock Frequency (MHz) | | | | |
|---|---|---|---|---|---|---|---|
| | | | 8.192 | 4.9152 | 4.096 | 2.4576 | 2.048 |
| | | | | | (12.288/3) | (12.288/5) | (6.144/3) |
| ClkDiv A | ClkDiv B | Xtal Freq. Data Rate | Data Rate (bps) | | | | |
| 0 | 0 | 128 | 64000* | 38400* | 32000 | 19200 | 16000 |
| 0 | 1 | 256 | 32000 | 19200 | 16000 | 9600 | 8000 |
| 1 | 0 | 512 | 16000 | 9600 | 8000 | 4800 | 4000 |
| 1 | 1 | 1024 | 8000 | 4800 | 4000 | | |

* $V_{DD}$ > = 4.5V

**Table 1: Clock/Data Rates**

**Note**: The device operation is not guaranteed above 64kbps or below 4kbps at the relevant supply voltage.

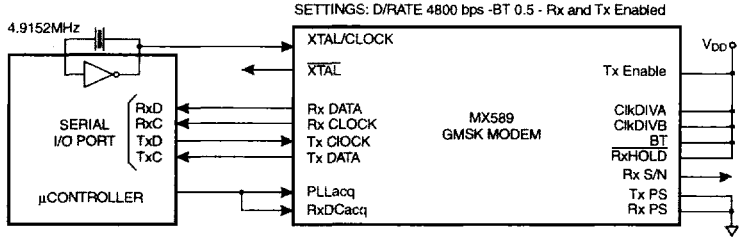


**Figure 4: Minimum µController System Connections**

## 4.2 Receive

### 4.2.1 Rx Signal Path Description

The function of the Rx circuitry is to:

1. Set the incoming signal to a usable level.
2. Clean the signal by filtering.
3. Provide DC level thresholds for clock and data extraction.
4. Provide clock timing information for data extraction and external circuits.
5. Provide Rx data in a binary form.
6. Assess signal quality and provide Signal-to-Noise information.

The output of the radio receiver's Frequency Discriminator should be fed to the MX589's Rx Filter by a suitable gain and DC level adjusting circuit. This circuit can be built with external components around the on-chip Rx Input Amplifier. The gain should be set so that the signal level at the Rx Feedback pin is nominally 1V peak to peak (for $V_{DD}$ = 5.0V) centered around $V_{BIAS}$ when receiving a continuous 1111000011110000.. data pattern.

Positive going signal excursions at Rx Feedback pin will produce a logic 0 at the Rx Data Output. Negative going excursions will produce a logic 1.

The received signal is fed through the lowpass Rx Filter, which has a -3dB corner frequency of 0.56 times the data bit-rate, before being applied to the Level Measure and Clock and Data extraction blocks.

The Level Measuring block consists of two voltage detectors, one of which measures the amplitude of the positive parts of the received signal. The other measures the amplitude of the negative portions. (Positive refers to signal levels higher than $V_{DD}$/2, and negative to levels lower than $V_{DD}$/2.) External capacitors are used by these detectors, via the Doc1 &

Doc2 pins, to form voltage hold or integrator circuits. These two levels are then used to establish the optimum DC level decision-thresholds for the Clock and Data extraction, depending upon the Rx signal amplitude and any DC offset.

### 4.2.2 Rx Circuit Control Modes

The operating characteristics of the Rx Level Measurement and Clock Extraction circuits are controlled, as shown in Table 2, by logic level inputs applied to the PLLacq, $\overline{\text{Rx HOLD}}$ and RxDCacq pins to suit a particular application, or to cope with changing reception conditions.

With reference to Figure 5, the Rx Mode Control diagram:

In general, a data transmission will begin with a preamble, for example, 1100110011001100, to allow the receive modem to establish timing and level-lock as quickly as possible. After the Rx carrier has been detected, and during the time that the preamble is expected, the RxDCacq and PLLacq Inputs should be switched from a logic 0 to a logic 1 so that the Level Measuring and Clock Extraction modes are operated and sequenced as shown.

The $\overline{\text{Rx HOLD}}$ input should normally be held at a logic 1 while data is being received, but may be driven to a logic 0 to freeze the Level Measuring Clock Extraction circuits during a fade. If the fade lasts for less than 200 bit periods, normal operation can be resumed by returning the $\overline{\text{Rx HOLD}}$ input to a logic 1 at the end of the fade. For longer fades , it may be better to reset the Level Measuring circuits by placing the RxDCacq to a logic 1 for 10 to 20 bit periods.

$\overline{\text{Rx HOLD}}$ has no effect on the level Measuring circuits while RxDCacq is at a logic 1, and has no effect on the PLL while PLLacq is at a logic 1.

A logic 0 on $\overline{\text{Rx HOLD}}$ does not disable the Rx Clock output, and the Rx Data Extraction and S/N Detector circuits will continue to operate.

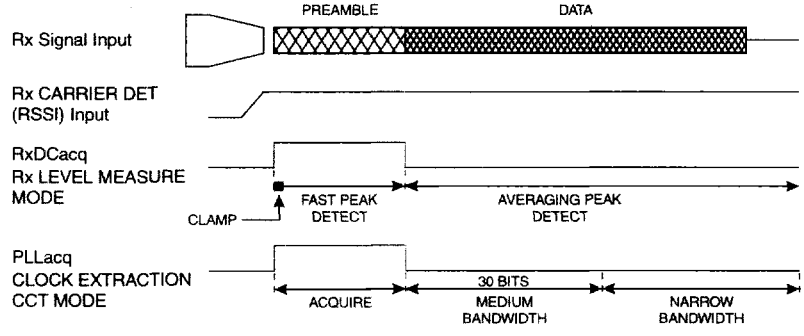


**Figure 5: Rx Mode Control Diagram**

| PLLacq | $\overline{\text{Rx HOLD}}$ | PLL Action | |
|---|---|---|---|
| 1 | 1 | Acquire | Sets the PLL bandwidth wide enough to allow a lock to the received signal in less than 8 zero crossings. This mode will operate as long as PLLacq is a logic 1 |
| 1 to 0 | 1 | Medium Bandwidth | The correction applied to the extracted clock is limited to a maximum of ± 1/16th bit-period for every two received zero crossings. The PLL operates in this mode for a period of about 30 bits immediately following a 1 to 0 transition of PLLacq input, provided that the $\overline{\text{Rx HOLD}}$ Input is a logic 1. |
| 0 | 1 | Narrow Bandwidth | The correction applied to the extracted clock is limited to a maximum of ± 1/64th bit-period for every two received zero crossings. The PLL operates in this mode whenever the $\overline{\text{Rx HOLD}}$ Input is a logic 1 and PLLacq has been a logic 0 for at least 30 bit periods (after Medium Bandwidth operation for instance) |
| 0 | 0 | Hold | The PLL feedback loop is broken, allowing the Rx Clock to freewheel during signal fade periods. |
| **RxDCacq** | **$\overline{\text{Rx HOLD}}$** | **Rx Level Measure Action** | |
| 0 to 1 | X | Clamp | Operates for one bit-time after a 0 to 1 transition of the RxDCacq input. The external capacitors are rapidly charged towards a voltage mid way between the received signal input level and $V_{BIAS}$ with the charge time-constant being of the order of 0.5 bit-time. |
| 1 | X | Fast Peak Detect | The voltage detectors act as peak detectors, one capacitor is used to capture the positive -going signal peaks of the Rx Filter output signal and the other capturing the negative-going peaks. The detectors operate in this mode whenever the RxDCacq input is at a logic 1 except for the initial 1-bit Clamp Mode time. |
| 0 | 1 | Averaging Peak Detect | Provides a slower but more accurate measurement of the signal peak amplitudes. |
| 0 | 0 | Hold | The capacitor charging circuits are disabled so that the outputs of the voltage detectors remain substantially at the last readings (discharging very slowly [time-constant approx. 2,000 bits] towards $V_{BIAS}$) |

X = Don't care

**Table 2: PLL and Rx Level Measurement Operational Modes**

#### 4.2.3 *Rx Clock Extraction*

Synchronized by a PLL circuit to zero-crossings of the incoming data, the Rx Clock Extraction circuitry controls the Rx Clock output. The Rx Clock is also used internally by the Data Extraction circuitry. The PLL parameters can be varied by the Rx Circuit Control inputs PLLacq and Rx HOLD to operated in one of four PLL modes as described in Table 2

#### 4.2.4 Rx Data Extraction

The Rx Data Extraction circuit decides whether each received bit is a 1 or 0 by sampling the received signal, after filtering, and comparing the sample values to an adaptive threshold derived from the Level Measuring circuit. This threshold is adapted from bit to bit to compensate for intersymbol interference caused by the bandlimiting of the overall transmission path and the Gaussian premodulation filter. The extracted data is output from the Rx Data pin, and should be sampled externally on the rising edge of the Rx CLK.

#### 4.2.5 Rx S/N Detection

The Rx S/N Detector system classifies the incoming zero-crossings as GOOD or BAD depending upon the time when each crossing actually occurs with respect to its expected time as determined by the Clock Extraction PLL. This information is then processed to provide a logic level output at the Rx S/N pin. A high level indicates a series of GOOD crossings; a low level indicates a BAD crossing.

By averaging this output it is possible to derive a measure of the Signal-to-Noise-Ratio and therefore the Bit-Error-Rate of the received signal.


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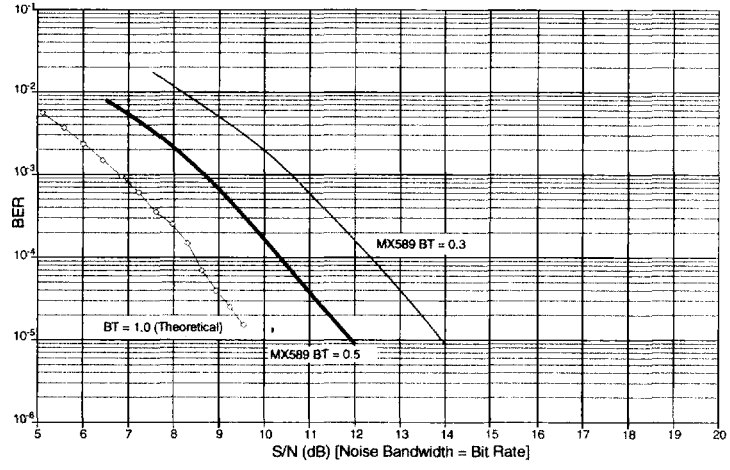


**Figure 6: Typical Bit-Error-Rate Performance**

### 4.2.6 Rx Signal Quality

The effect of input Rx signal quality on the Rx S/N output is shown in Figure 7.

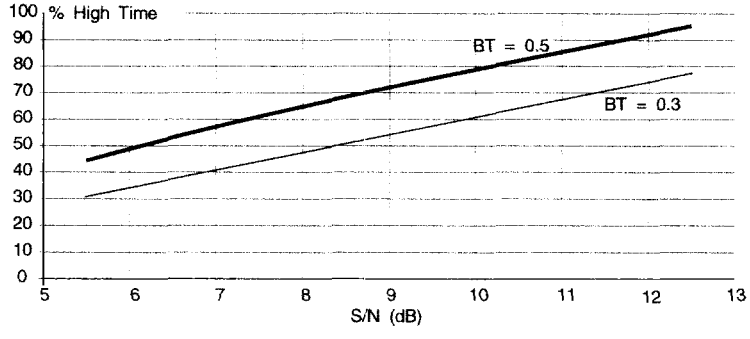


**Figure 7: Typical Rx S/N Output High time (%) vs Input S/N**


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## 4.3 Transmit

### 4.3.1 Tx Signal Path Description

The binary data applied to the Tx Data input is retimed within the chip on each rising edge of the Tx Clock and then converted to a 1-volt peak-to-peak binary signal centered about $V_{BIAS}$ (for $V_{DD}$ = 5.0V)

If the Tx Enable input is high, then this internal binary signal will be connected to the input of the lowpass Tx Filter, and the output of the filter connected to the Tx Out pin.

| Tx Enable | Tx Filter Input | Tx Out Pin |
|---|---|---|
| 1 | $V_{DD}/5$ $V_{P-P}$ Data | Filtered Data |
| 0 | $V_{BIAS}$ | $V_{BIAS}$ via 500kΩ |

A low input to the Tx Enable will connect the input of the Tx Filter to $V_{BIAS}$, and disconnect the Tx Out pin from the filter, connecting it instead to $V_{BIAS}$ through a high resistance (nominally 500kΩ).

The Tx Filter has a lowpass frequency response, which is approximately gaussian in shape as shown in Figure 9, to minimize amplitude and phase distortion of the binary signal while providing sufficient attenuation of the high frequency components which would otherwise cause interference into adjacent radio channels. The actual filter bandwidth to be used in any particular application will be determined by the overall system requirements. The attenuation-vs-frequency response of the transmit filtering provided by the MX589 have been designed to meet the specifications for most GMSK modem systems, having a -3dB bandwidth switchable between 0.3 and 0.5 times the data bit-rate (BT).

**Note**: An external RC network is required between the Tx Out pin and the input to the Frequency Modulator (see Figure 2 and Figure 3). This network, which can form part of any DC level shifting and gain adjustment circuitry, forms an important part of the transmit signal filtering. The ground connection to capacitor C1 should be positioned to give maximum attenuation of high-frequency noise into the modulator.

The signal at Tx Out is centered around $V_{BIAS}$, going positive for logic 1 (high) level inputs to the Tx Data input and negative for logic 0 (low) inputs.

When the transmit circuits are put into a powersave mode (by a logic 1 to the Tx PS pin) the output voltage of the Tx Filter will go to $V_{SS}$. When power is subsequently restored to the Tx Filter, its output will take several bit-times to settle. The Tx Enable input can be used to prevent these abnormal voltages from appearing at the Tx Out pin.

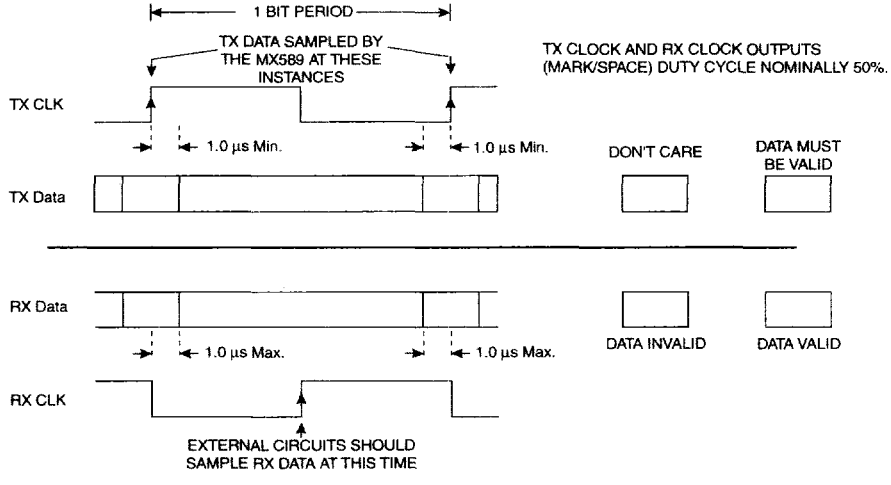


**Figure 8: Rx and Tx Clock Data Timings**

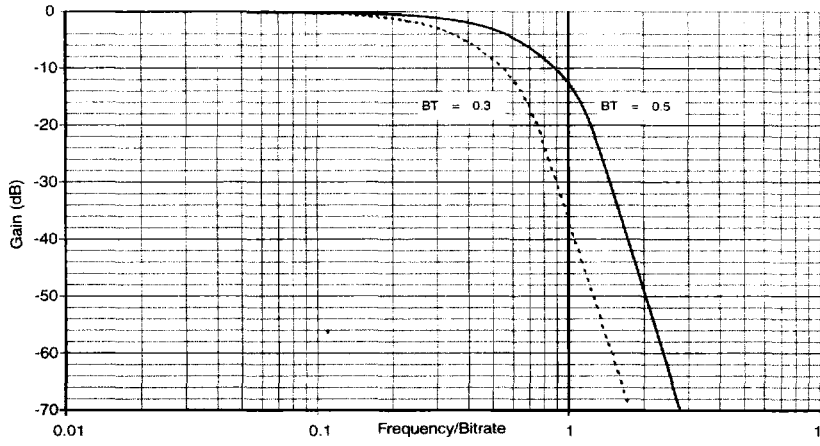


**Figure 9: Tx Filter Response**

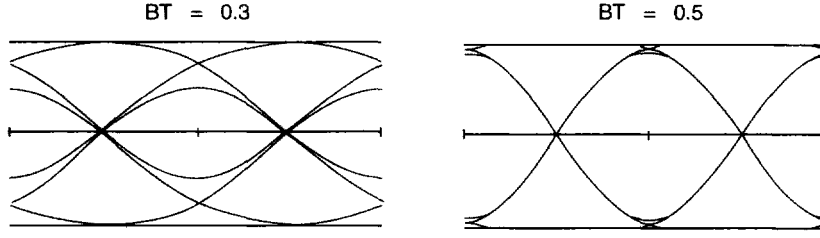


**Figure 10: Typical Transmit Eye Patterns**

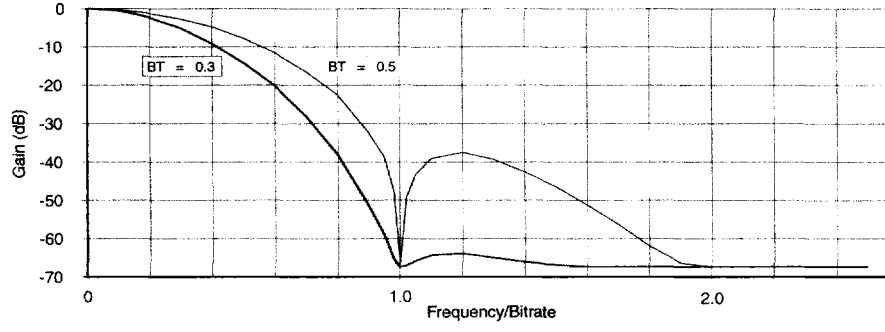


**Figure 11: Tx Output spectrum (Random Data)**

### 4.4 Data Formats

The receive section of the MX589 works best with data which has a reasonably random structure --the data should contain approximately the same number of ones as zeroes with no long sequences (>100 bits) of consecutive ones or zeroes. Also, long sequences (>100 bits) of 10101010 ... patterns should be avoided.

For this reason, it is recommended that data is made random in some manner before transmission, for example by exclusive-ORing it with the output of a binary pseudo-random pattern generator.

Where data is transmitted in bursts, each burst should be preceded by a preamble designed to allow the receive modem to establish timing and level lock as quickly as possible. This preamble for BT = 0.3 should be at least 16 bits long, and should preferably consist of alternating pairs of ones and zeroes i.e. 110011001100 .....; the eye of pattern 10101010 .... has the most gradual slope and will yield poor peak levels for the Rx circuits. For BT = 0.5 the eye pattern of 10101010... has reduced intersymbol interference and may be used as the preamble (DC Acq pin should be held high during preamble). See Fig. 6.

### 4.5 Acquisition and Hold Modes

The RxDCacq and PLLacq inputs must be pulsed High for about 16 bits at the start of reception to ensure that the DC measurement and timing extraction circuits lock-on to the received signal correctly. Once lock has been achieved, then the above inputs should be taken Low again.

In most applications, there will be a DC step in the output voltage from the receiver FM discriminator due to carrier frequency offsets as channels are changed or when the remote transmitter is turned on.

The MX589 can tolerate DC offsets in the received signal of at least ±0.5V with respect to $V_{BIAS}$, (measured at the Rx Feedback pin). However, to ensure that the DC offset compensation circuit operates correctly and with minimum delay, the Low to High transition of the RxDCacq and PLLacq inputs should occur after the mean input voltage to the MX589 has settled to within about 0.1V of its final value.

**Note**: This can place restrictions on the value of any series signal coupling capacitor.

As well as using the Rx Hold input to freeze the Level Measuring and Clock Extraction circuits during a signal fade, it may also be used in systems which use a continuously transmitting control channel to freeze the Rx circuitry during transmission of a data packet, allowing reception to resume afterwards without losing bit synchronization. To achieve this, the MX589 Xtal clock needs to be accurate enough that the derived RxClock output does not drift by more than about 0.1 bit time from the actual received data-rate during the time that the RxHold input is Low.

The RxDCacq input, however, may need to be pulsed high for 2 bit durations to re-establish the level measurements if the RxHold input is low for more that a few hundred bit-times (exact number depends on system crystal tolerances).

The voltages on the Doc1 and Doc2 pins reflect the average peak positive and negative excursions of the (filtered) receive signal, and could therefore be used to derive a measure of the data signal amplitude.

**Note**: These pins are driven from very high-impedance circuits, so that the DC load presented by any external circuitry should exceed 10MΩ to $V_{BIAS}$.

## 5. Application

### 5.1 Radio Channel Requirements

To achieve legal adjacent channel performance at high bit-rates, a radio with an accurate carrier frequency and an accurate modulation index is required. For optimum channel utilization, (e.g. low BER and high data-rates) attention must be paid to the phase and frequency response of both the IF and baseband circuitry.

#### 5.1.1 Bitrate, BT and Bandwidth

The maximum data rate that can be transmitted over a radio channel depends on the following:

Channel spacing

Allowable adjacent channel interference

Tx filter bandwidth

Peak carrier deviation (Modulation Index)

Tx and Rx carrier frequency accuracies

Modulator and Demodulator linearity

Rx IF filter frequency and phase characteristics

Use of error correction techniques

Acceptable error-rate

As a guide to MOBITEX operation, a raw data-rate of 8kbps at 12.5kHz channel spacing may be achievable -depending on local regulatory requirements- using a ±2kHz maximum deviation, a BT of 0.3, and no more than 1.5kHz discrepancy between Tx & Rx carrier frequencies. Forward error correction (FEC) could then be used with interleaving to reduce the effect of burst errors.

Reducing the data-rate to 4.8kbps would allow the BT to be increased to 0.5, improving the error-rate performance.

### 5.1.2 FM Modulator, Demodulator and IF

For optimum performance, the eye pattern of the received signal (when receiving random data) applied to the MX589 should be as close as possible to the Transmit eye pattern examples shown in Figure 11.

Of particular importance are general symmetry, cleanliness of the zero-crossings, and for a BT of 0.3, the relative amplitude of the inner eye opening.

To achieve this, attention must be paid to -

Linearity and frequency/phase response of the Tx frequency modulator. Unless the transmit data is especially encoded to remove low frequency components, the modulator frequency response should extend down to a few hertz. This is because two-point modulation is necessary for synthesized radios.

Bandwidth & phase response of the Rx IF filters.

Accuracy of the Tx and Rx carrier frequencies -any difference will shift the received signal towards one of the skirts of the IF filter response.

Ideally, the Rx demodulator should be DC coupled to the MX589 Rx Signal In pin (with a DC bias added to center the signal at the Rx Feedback pin around $V_{DD}/2$ [$V_{BIAS}$] ). However AC coupling can be used provided that:

The 3 dB cut-off frequency is 20Hz or below (i.e. a 0.1µF capacitor in series with 100kΩ).

The data does not contain long sequences of consecutive ones or zeroes.

Sufficient time is allowed after a step change at the discriminator output (resulting from channel changing or the appearance of an RF carrier) for the voltage into the MX589 to settle before the RxDCacq line is strobed.

### 5.1.3 Two Point Modulation

When designing the MX589 into a radio that uses a frequency synthesizer, a two-point modulation technique is recommended. This is both to prevent the radio's PLL circuitry from counteracting the modulation process, and to provide a clean flat modulation response down to DC

Figure 12 shows a suggested basic configuration to provide a two-point modulation drive from the MX589 Tx Output using MX•COM's MX019 Digitally Controlled Quad Amplifier Array. The MX019 elements provide individual set-up, calibration and dynamic control of modulation levels. Level setting control of the amplifiers/attenuators of the MX019 is via an 8-bit data word.

With reference to Figure 12:

The buffer amplifier is required to prevent loading of the MX589 external RC circuit.

Stage B, with R1/R2, provides suitable signal and DC levels for the VCO varactor; C1 is RF decoupling. The drive level should be adjusted (digitally) to provide the desired deviation.

Stage C, with R3/R4, provides the Reference Oscillator drive (application dependent). This parameter is set by adjusting for minimum AC signal on the PLL control voltage with a low-frequency modulating signal (inside the PLL bandwidth) applied.

Stage D could be used with the components shown if a negative reference drive is required.

Stage A provides buffering and overall level control.


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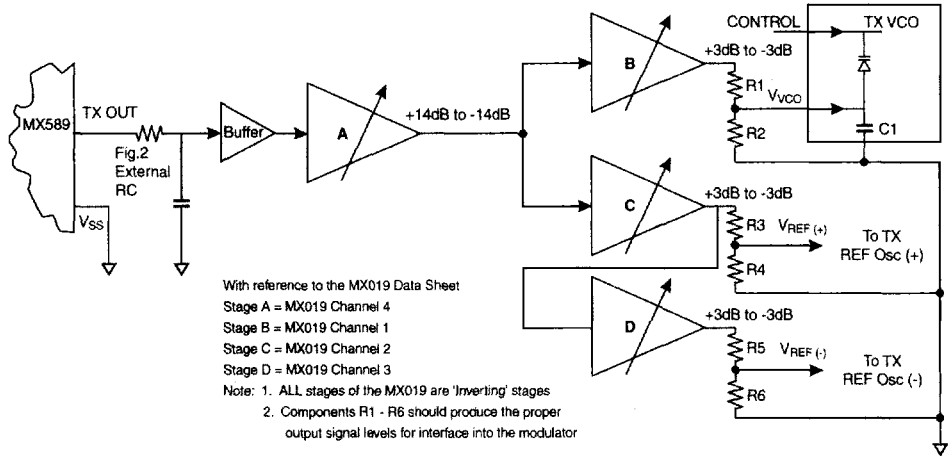


**Figure 12: An Example of Two-Point Modulation Drive with Individual Adjustment Using the MX019**

## 5.2 AC Coupling of Tx and Rx Signals

In practical applications, it will usually be possible to arrange for any AC coupling between the MX589 Tx Output and the frequency modulator to cut-off at a very low frequency such as 5.0Hz, but Ac coupling between the receive discriminator and the input of the MX589 may need to have a shorter time-constant to avoid problems from voltage steps at the output of the discriminator when changing channels or when the distant transmitter turns on.

For these reasons, as well as to maintain reasonable BER, the optimum -3dB cut-off frequencies are around 5.0Hz in the Tx path and 20.Hz in the Rx path.

Figure 13 shows the typical static Bit-Error-Rate performance of the MX589 operating under nominal conditions for various degrees of AC coupling at the Rx input and the Tx Output:

Data Rate = 8kbps $V_{DD}$ = 5.0V $T_{AMB}$ = 25°C Tx BT = 0.3

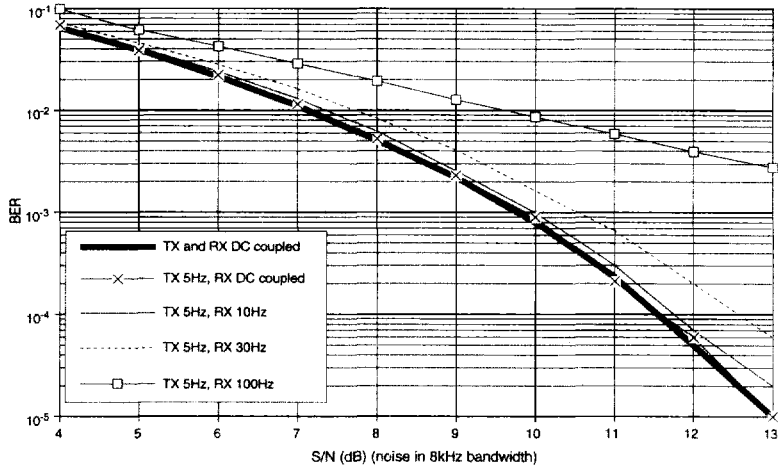


**Figure 13: Effect of AC Coupling on Typical Bit-Error Rate**

# 6. Performance Specification

## 6.1 Electrical Performance

### Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

| General | Min. | Max. | Units |
|---|---|---|---|
| Supply ($V_{DD}$ - $V_{SS}$) | -0.3 | 7.0 | V |
| Voltage on any pin to $V_{SS}$ | -0.3 | $V_{DD}$ + 0.3 | V |
| Current | | | |
| $V_{DD}$ | -30 | 30 | mA |
| $V_{SS}$ | -30 | 30 | mA |
| Any other pins | -20 | 20 | mA |
| **DW / PDIP Package** | | | |
| Total Allowable Power Dissipation at $T_{AMB}$ = 25°C | | 800 | mW |
| Derating above 25°C | | 13 | mW/°C above 25°C |
| Storage Temperature | -55 | 85 | °C |
| Operating Temperature | -40 | 85 | °C |
| **TN Package** | | | |
| Total Allowable Power Dissipation at $T_{AMB}$ = 25°C | | 550 | mW |
| Derating above 25°C | | 9 | mW/°C above 25°C |
| Storage Temperature | -55 | 85 | °C |
| Operating Temperature | -40 | 85 | °C |


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### Operating Limits

Correct operation of the device outside these limits is not implied.

| | Notes | Min. | Max. | Units |
|---|---|---|---|---|
| Supply ($V_{DD}$ - $V_{SS}$) | | 3.0 | 5.5 | V |
| Temperature | | -40 | 85 | °C |
| Rx and Tx Data Rate | | | | |
| $V_{DD} \geq 3.0V$ | | 4 | 32 | kbps |
| $V_{DD} \geq 4.5V$ | | 4 | 64 | kbps |
| Xtal/Clock Frequency | | | | |
| $V_{DD} \geq 3.0V$ | | 1.0 | 5.0 | MHz |
| $V_{DD} \geq 4.5V$ | | 1.0 | 10.3 | MHz |
| High Pulse Width | 1 | 40 | | ns |
| Low Pulse Width | 1 | 40 | | ns |

### Operating Limits Notes:

1. Timing for an external clock input to the Xtal/Clock pin.


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**Operating Characteristics**

For the following conditions unless otherwise specified:

$V_{DD}$ = 5.0V @ $T_{AMB}$ = 25°C

Xtal Frequency = 4.096mhz Data Rate = 8kbps Noise Bandwidth = Bit Rate

| | | | Notes | Min. | Typ. | Max | Units |
|---|---|---|---|---|---|---|---|
| **Static Values** | | | | | | | |
| Supply Current | Tx PS | Rx PS | 1 | | | | |
| $I_{DD}$ ($V_{DD}$ = 3.0V) | | | | | | | |
| | 1 | 1 | | | 0.5 | | mA |
| | 0 | 1 | | | 1.0 | | mA |
| | 1 | 0 | | | 1.0 | | mA |
| | 0 | 0 | | | 1.5 | | mA |
| $I_{DD}$ | | | | | | | |
| | 1 | 1 | | | 1.0 | | mA |
| | 0 | 1 | | | 2.0 | | mA |
| | 1 | 0 | | | 3.0 | | mA |
| | 0 | 0 | | | 4.0 | | mA |
| Input Logic Level | | | | | | | |
| Logic 1 Input Level | | | | 3.5 | | | V |
| Logic 0 Input Level | | | | | | 1.5 | V |
| Logic Input Current | | | 2 | -5.0 | | 5.0 | µA |
| Logic 1 Output Level ($I_{OH}$ = -120µA) | | | | 4.6 | | | V |
| Logic 0 Output Level ($I_{OL}$ = -120µA) | | | | | | 0.4 | V |
| **Transmit Parameters** | | | | | | | |
| Tx OUT, Output Impedance | | | 3 | | 1.0 | | kΩ |
| Tx OUT, Level | | | 4,10 | 0.8 | 1.0 | 1.2 | $V_{P-P}$ |
| Tx Data Delay | | | | | | | |
| BT = 0.3 | | | 5 | | 2.0 | 2.5 | bit-periods |
| BT = 0.5 | | | 5 | | 1.5 | 2.0 | bit-periods |
| Tx PS to Output-Stable time | | | 6 | | 4.0 | | |
| **Receive Parameters** | | | | | | | |
| Rx Amplifier- | | | | | | | |
| Input Impedance | | | | 1.0 | | | MΩ |
| Output Impedance | | | 7 | | 10.0 | | kΩ |
| Voltage Gain | | | | | 50.0 | | dB |
| Rx Filter Signal Input Level | | | 8, 10 | 0.7 | 1.0 | 1.3 | $V_{P-P}$ |
| Rx Time Delay | | | 9 | | | 3.0 | bit-periods |
| **On-Chip Xtal Oscillator** | | | | | | | |
| $R_{IN}$ | | | | 10.0 | | | MΩ |
| $R_{OUT}$ | | | 11 | | 50.0 | | kΩ |
| Voltage Gain | | | 11 | | 25.0 | | dB |


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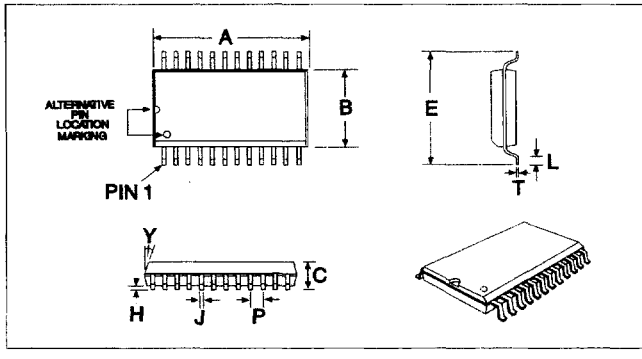
**Operating Characteristics Notes:**

1. Not including current drawn from the MX589 pins by external circuitry. See Absolute Maximum Ratings.
2. For $V_{IN}$ in the range $V_{SS}$ to $V_{DD}$.
3. For a load of 10kW or greater. Tx PS input at logic 0; Tx Enable = 1.
4. Data pattern of 1111000011110000 ..
5. Measured between the rising edge of Tx Clock and the center of the corresponding bit at Tx Out.
6. Time between the falling edge of Tx PS and the Tx Out voltage stabilizing to normal output levels.
7. For a load of 10kW or greater. Rx PS input at logic 0.
8. For optimum performance, Measured at the Rx Feedback pin for a 1111000011110000 ... pattern.
9. Measured between the center of bit at Rx Signal In and corresponding rising edge of the Rx Clock.
10. Levels are proportional to applied $V_{DD}$.
11. Small signal measurement at 1.0kHz with no load on Xtal output.

## 6.2 Packaging

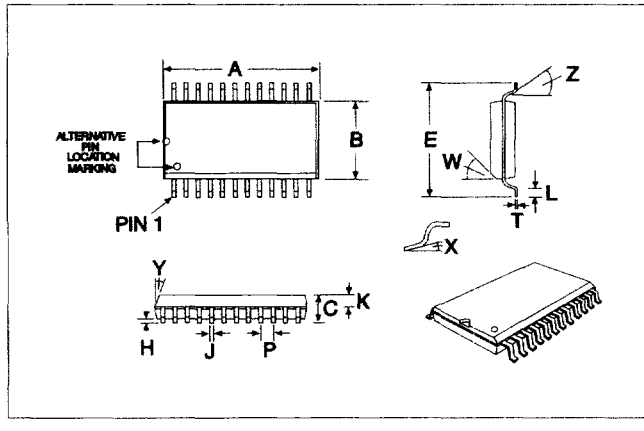



**Package Tolerances**

| DIM. | MIN. | TYP. | MAX. |
|---|---|---|---|
| A | 0.303 (7.70) | | 0.311 (7.90) |
| B | 0.169 (4.30) | | 0.177 (4.50) |
| C | ---------- | | 0.047 (1.20) |
| E | 0.248 (6.30) | | 0.256 (6.50) |
| H | 0.002 (0.05) | | 0.006 (0.15) |
| J | 0.007 (0.17) | | 0.012 (0.30) |
| L | 0.020 (0.50) | | 0.030 (0.75) |
| P | | 0.0256 (0.65) | |
| T | 0.003 (0.08) | | 0.008 (0.20) |
| Y | 0° | | 8° |

NOTE : All dimensions in inches (mm.)
Angles are in degrees

**Figure 14: 24-pin TSSOP Mechanical Outline: *Order as part no. MX589TN***




**Package Tolerances**

| DIM. | MIN. | TYP. | MAX. |
|---|---|---|---|
| A | 0.597 (15.16) | | 0.613 (15.57) |
| B | 0.286 (7.26) | | 0.299 (7.59) |
| C | 0.093 (2.36) | | 0.105 (2.67) |
| E | 0.390 (9.90) | | 0.419 (10.64) |
| H | 0.003 (0.08) | | 0.020 (0.51) |
| J | 0.013 (0.33) | | 0.020 (0.51) |
| K | 0.036 (0.91) | | 0.046 (1.17) |
| L | 0.016 (0.41) | | 0.050 (1.27) |
| P | | 0.050 (1.27) | |
| T | 0.009 (0.23) | | 0.0125 (0.32) |
| W | | 45° | |
| X | 0° | | 10° |
| Y | 5° | | 7° |
| Z | | 5° | |

NOTE : All dimensions in inches (mm.)
Angles are in degrees

**Figure 15: 24-pin SOIC Mechanical Outline: *Order as part no. MX589DW***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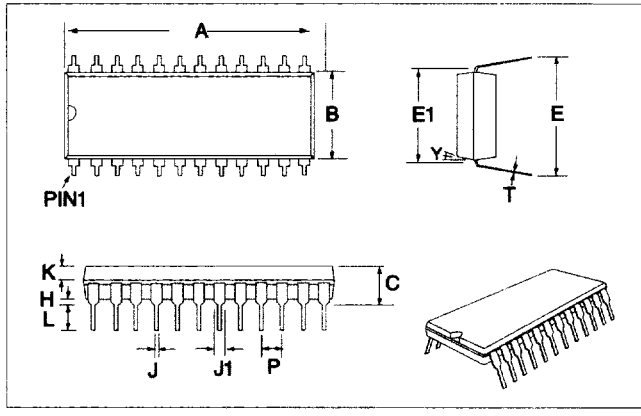


**Package Tolerances**

| DIM. | MIN. | TYP. | MAX. |
|---|---|---|---|
| A | 1.200 (30.48) | | 1.270 (32.26) |
| B | 0.500 (12.70) | | 0.555 (14.04) |
| C | 0.151 (3.84) | | 0.220 (5.59) |
| E | 0.600 (15.24) | | 0.670 (17.02) |
| E1 | 0.590 (14.99) | | 0.625 (15.88) |
| H | 0.015 (0.38) | | 0.045 (1.14) |
| J | 0.015 (0.38) | | 0.023 (0.58) |
| J1 | 0.040 (1.02) | | 0.065 (1.65) |
| K | 0.066 (1.67) | | 0.074 (1.88) |
| L | 0.121 (3.07) | | 0.160 (4.05) |
| P | | 0.100 (2.54) | |
| T | 0.008 (0.20) | | 0.015 (0.38) |
| Y | | 7° | |

NOTE : All dimensions in inches (mm.)
Angles are in degrees

**Figure 16: 24-pin PDIP Mechanical Outline: *Order as part no. MX589P***


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